

N-channel 950 V, 3 Ω typ., 4 A Zener-protected SuperMESH3™ Power MOSFET in I²PAKFP package

Datasheet – production data

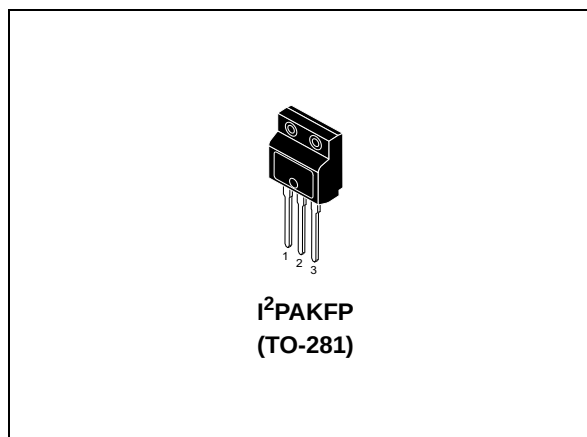
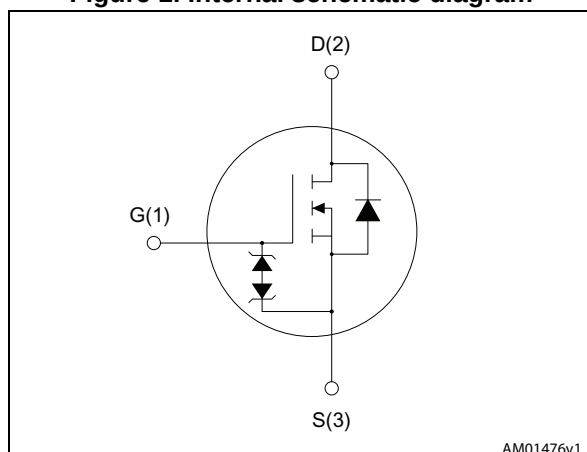


Figure 1. Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STFI5N95K3	950 V	3.5 Ω	4 A	25 W

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- 100% avalanche tested
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitances
- Zener-protected

Applications

- Switching applications

Description

This SuperMESH3™ Power MOSFET is the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Table 1. Device summary

Order code	Marking	Package	Packaging
STFI5N95K3	5N95K3	I ² PAKFP (TO-281)	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	4 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	3 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	16 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	25	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	100	mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	5	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ }^{\circ}\text{C}$)	2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^{\circ}\text{C}$

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 4\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, peak $V_{DS} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	5	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^{\circ}\text{C}/\text{W}$

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	950			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 950 \text{ V}$ $V_{DS} = 950 \text{ V}$, $T_C = 125 \text{ °C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100 \mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}$, $I_D = 2 \text{ A}$		3	3.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$	-	460	-	pF
C_{oss}	Output capacitance		-	38	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0 \text{ to } 760 \text{ V}$, $V_{GS} = 0$	-	970	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related	$V_{DS} = 0 \text{ to } 760 \text{ V}$, $V_{GS} = 0$	-	15	-	pF
R_g	Gate input resistance	$f = 1 \text{ MHz}$ open drain	-	5.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 760 \text{ V}$, $I_D = 4 \text{ A}$, $V_{GS} = 10 \text{ V}$ (see Figure 16)	-	19	-	nC
Q_{gs}	Gate-source charge		-	4.7	-	nC
Q_{gd}	Gate-drain charge		-	12	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}$, $I_D = 2\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15)	-	17	-	ns
t_r	Rise time		-	7	-	ns
$t_{d(off)}$	Turn-off delay time		-	32	-	ns
t_f	Fall time		-	18	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 17)	-	410		ns
Q_{rr}	Reverse recovery charge		-	3.5		μC
I_{RRM}	Reverse recovery current		-	17		A
t_{rr}	Reverse recovery time	$I_{SD} = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 17)	-	516		ns
Q_{rr}	Reverse recovery charge		-	4.1		μC
I_{RRM}	Reverse recovery current		-	16		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

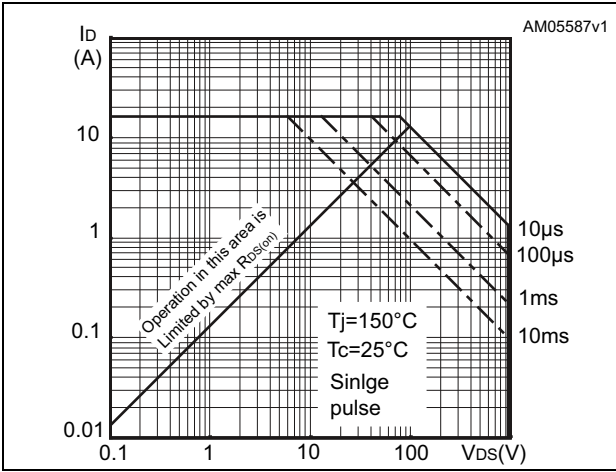


Figure 3. Thermal impedance

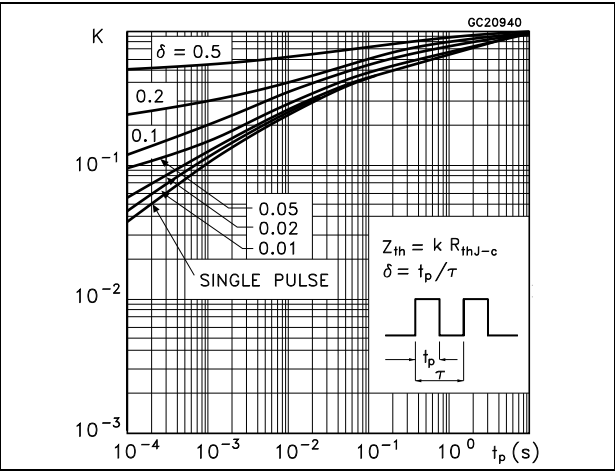


Figure 4. Output characteristics

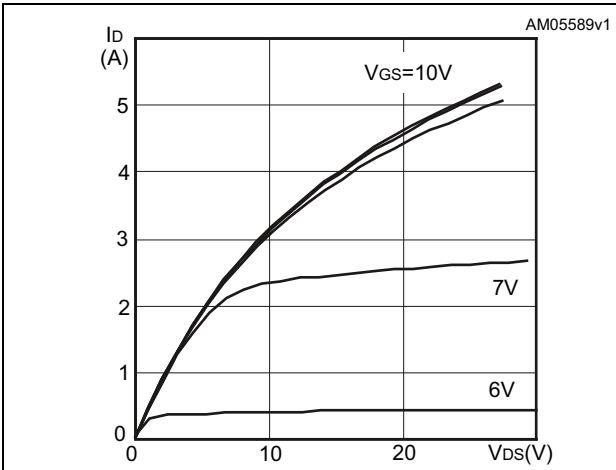


Figure 5. Transfer characteristics

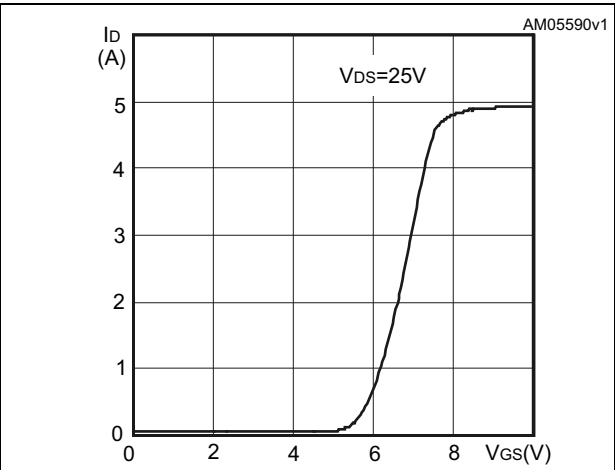


Figure 6. Gate charge vs gate-source voltage

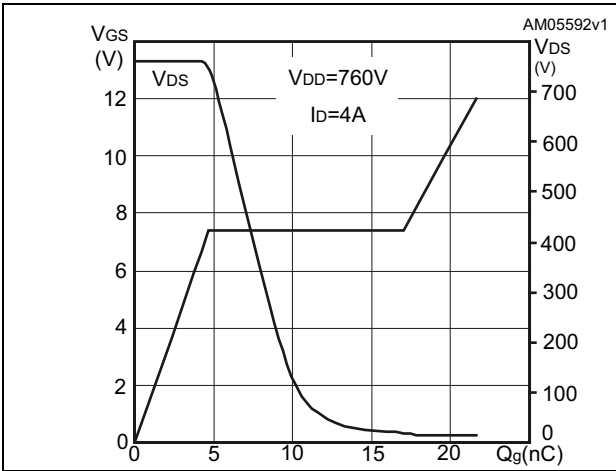


Figure 7. Static drain-source on-resistance

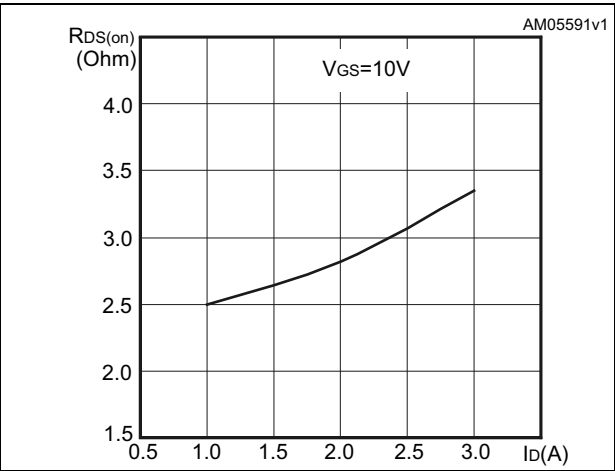


Figure 8. Capacitance variations

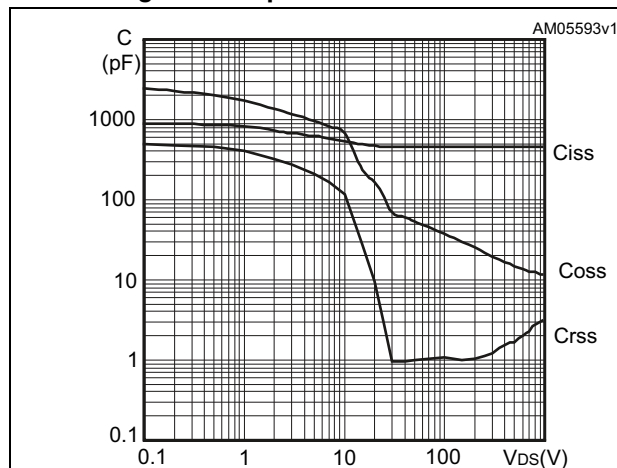


Figure 9. Output capacitance stored energy

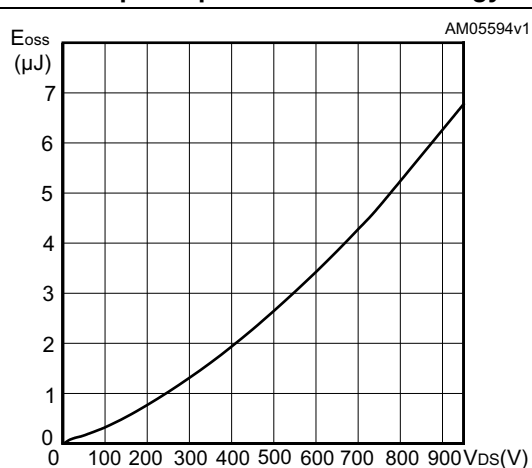


Figure 10. Normalized gate threshold voltage vs temperature

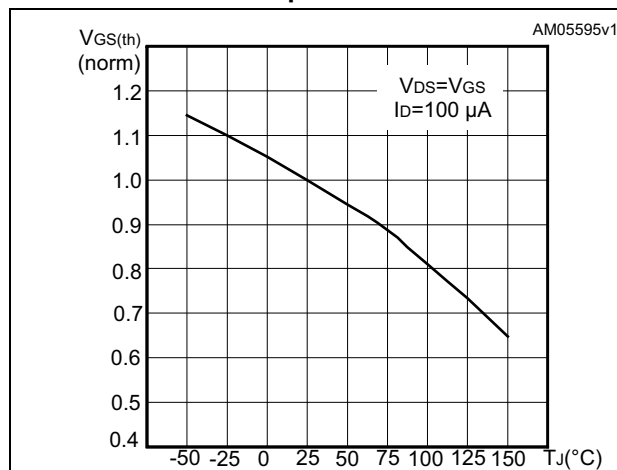


Figure 11. Normalized on-resistance vs temperature

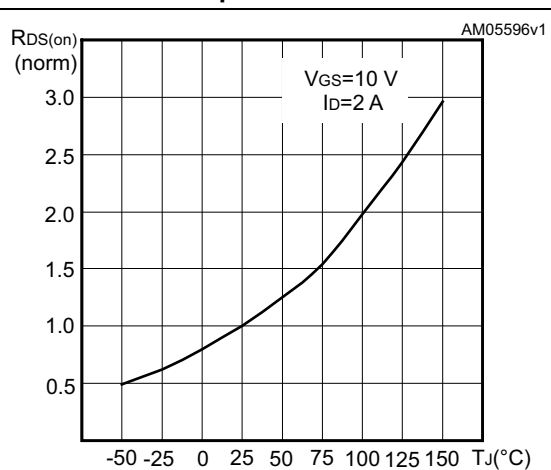


Figure 12. Source-drain diode forward characteristics

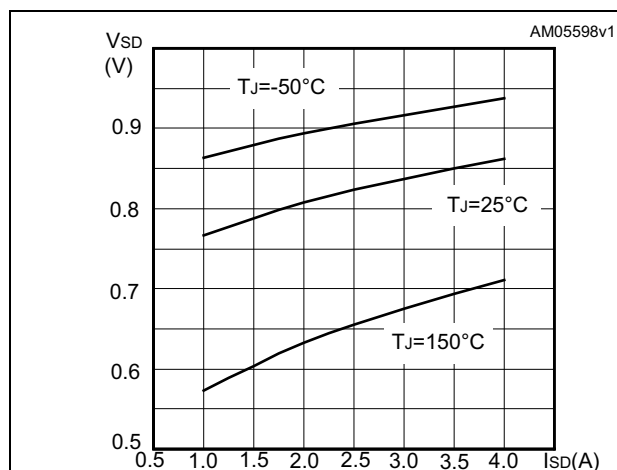
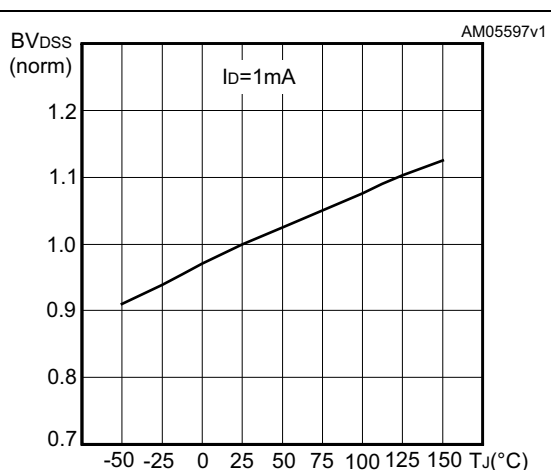
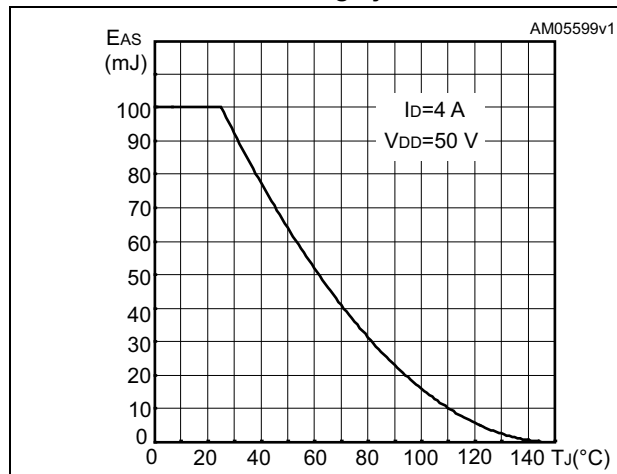
Figure 13. Normalized B_{VDS} vs temperature

Figure 14. Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 15. Switching times test circuit for resistive load



Figure 16. Gate charge test circuit

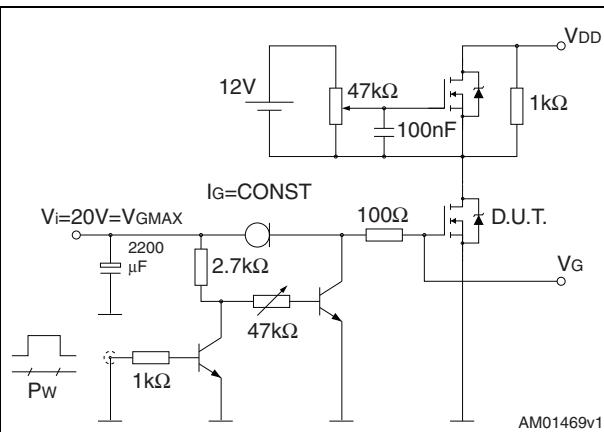


Figure 17. Test circuit for inductive load switching and diode recovery times

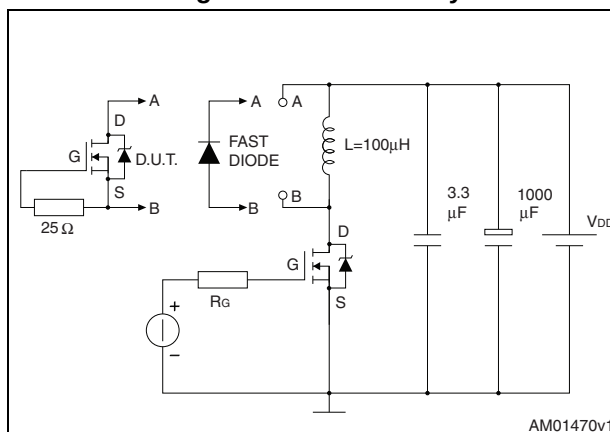


Figure 18. Unclamped inductive load test circuit

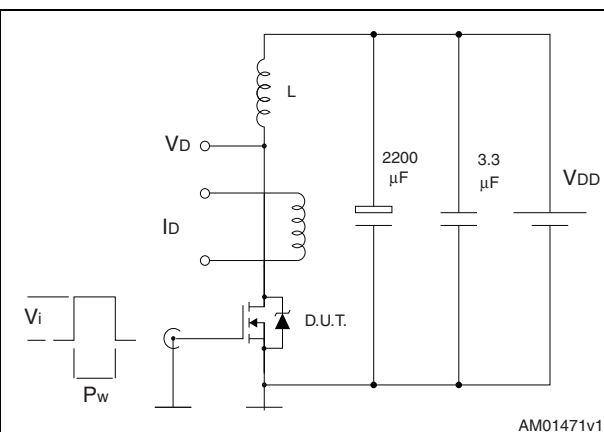


Figure 19. Unclamped inductive waveform

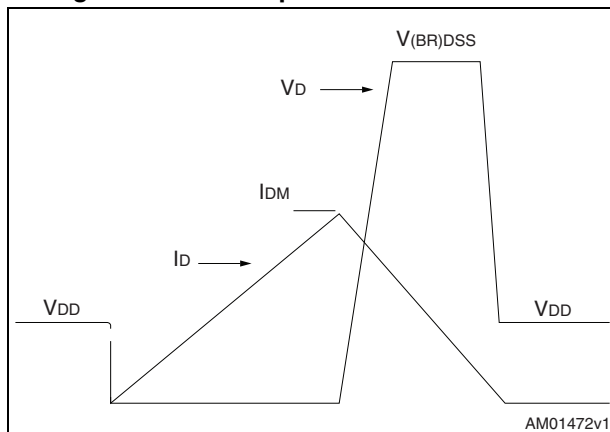


Figure 20. Switching time waveform



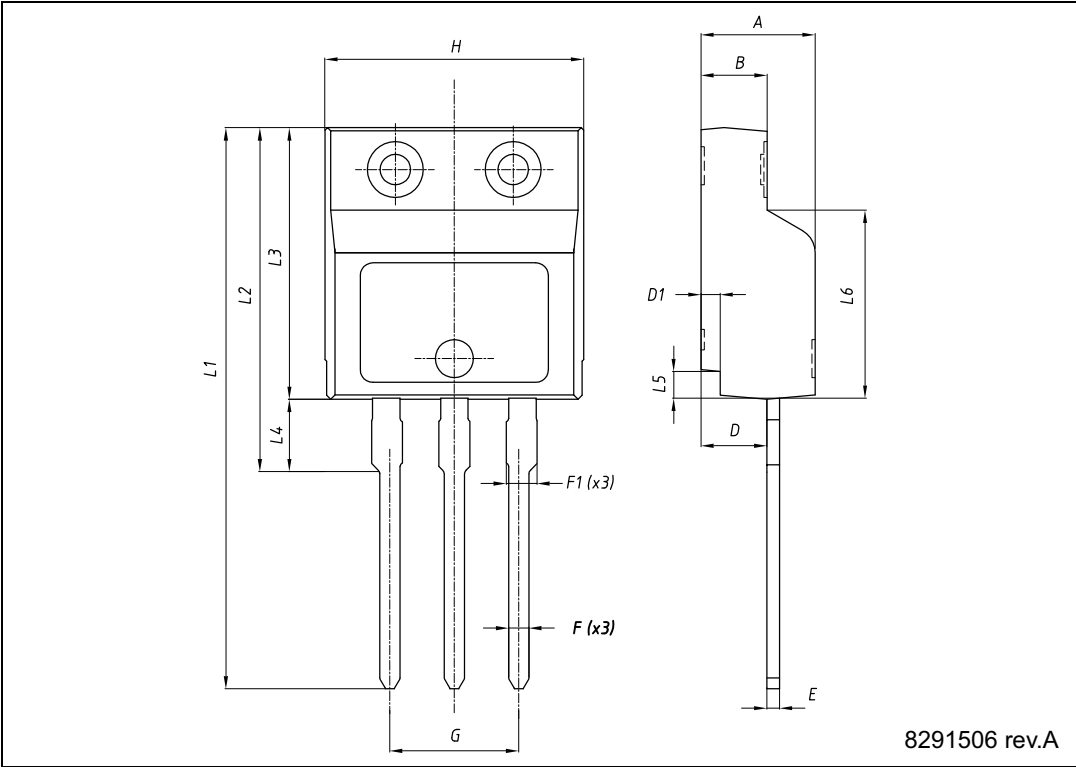
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 21. I²PAKFP (TO-281) drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
09-May-2013	1	First release

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