12-Bit, 20 MSPS/40 MSPS/65 MSPS 3 V Low Power A/D Converter

Data Sheet **AD9237**

FEATURES

- Ultralow power
  - 85 mW at 20 MSPS
  - 135 mW at 40 MSPS
  - 190 mW at 65 MSPS
- SNR = 66 dBc to Nyquist at 65 MSPS
- SFDR = 80 dBc to Nyquist at 65 MSPS
- DNL = ±0.7 LSB
- Differential input with 500 MHz bandwidth
- Flexible analog input: 1 V p-p to 4 V p-p range
- Offset binary, twos complement, or gray code data formats
- Output enable pin
- 2-step power-down
- Full power-down and sleep mode
- Clock duty cycle stabilizer

APPLICATIONS

- Ultrasound and medical imaging
- Battery-powered instruments
- Hand-held scope meters
- Low cost digital oscilloscopes
- Low power digital still cameras and copiers
- Low power communications

FUNCTIONAL BLOCK DIAGRAM

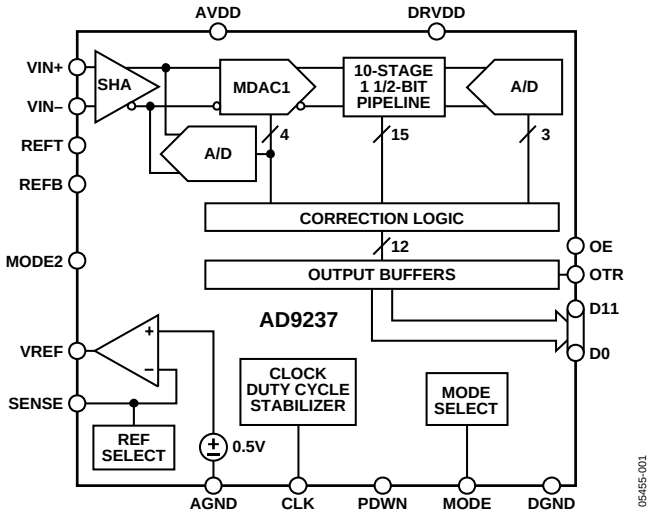

Figure 1.

GENERAL DESCRIPTION

The AD9237 is a family of monolithic, single 3 V supply, 12-bit, 20 MSPS/40 MSPS/65 MSPS analog-to-digital converters (ADC). This family features a high performance sample-and-hold amplifier (SHA) and voltage reference. The AD9237 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 20 MSPS/40 MSPS/65 MSPS data rates and guarantees no missing codes over the full operating temperature range.

With significant power savings over previously available ADCs, the AD9237 is suitable for applications in imaging and medical ultrasound.

Fabricated on an advanced CMOS process, the AD9237 is available in a 32-lead LFCSP and is specified over the industrial temperature range (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. Operating at 65 MSPS, the AD9237 consumes a low 190 mW at 65 MSPS, 135 mW at 40 MSPS, and 85 mW at 20 MSPS.
2. Power scaling reduces the operating power further when running at lower speeds.
3. The AD9237 operates from a single 3 V power supply and features a separate digital output driver supply to accommodate 2.5 V and 3.3 V logic families.
4. The patented SHA input maintains excellent performance for input frequencies beyond Nyquist and can be configured for single-ended or differential operation.
5. The AD9237 is optimized for selectable and flexible input ranges from 1 V p-p to 4 V p-p.
6. An output enable pin allows for multiplexing of the outputs.
7. Two-step power-down supports a standby mode in addition to a power-down mode.
8. The OTR output bit indicates when the signal is beyond the selected input range.
9. The clock duty cycle stabilizer (DCS) maintains converter performance over a wide range of clock pulse widths.

Rev. C

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AD9237* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-803: Pin Compatible High Speed ADCs Simplify Design Tasks
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9237: 12-Bit, 20 MSPS/40 MSPS/65 MSPS 3 V Low Power A/D Converter Data Sheet

TOOLS AND SIMULATIONS

- Visual Analog
- AD9237 IBIS Models
- AD9237LFCSP Analog Input S-Parameter Data

REFERENCE MATERIALS

Technical Articles

- Correlating High-Speed ADC Performance to Multicarrier 3G Requirements
- Matching An ADC To A Transformer
- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9237 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9237 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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10/05—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, maximum sample rate, 2 V p-p differential input, −0.5 dBFS input, 1.0 V internal reference, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	AD9237BCP-20			AD9237BCP-40			AD9237BCP-65			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	12			12			12			Bits
ACCURACY										
No Missing Codes Guaranteed	12			12			12			Bits
Offset Error		±1.30	±1.95		±1.30	±1.95		±1.30	±1.95	% FSR
Gain Error[1]		±0.70	±2.10		±0.75	±2.10		±1.05	±2.25	% FSR
Differential Nonlinearity (DNL)[2]		±0.70	±0.95		±0.70	±0.95	−1.00	±0.70	+1.25	LSB
Integral Nonlinearity (INL)[2]		±0.90	±1.35		±0.90	±1.35		±0.90	±2.00	LSB
TEMPERATURE DRIFT										
Offset Error		±2			±2			±2		ppm/°C
Gain Error[1]		±12			±12			±12		ppm/°C
INTERNAL VOLTAGE REFERENCE										
Output Voltage Error (1 V Mode)		±5	±25		±5	±25		±5	±25	mV
Load Regulation @ 1.0 mA		0.8			0.8			0.8		mV
Output Voltage Error (0.5 V Mode)		±2.5			±2.5			±2.5		mV
Load Regulation @ 0.5 mA		0.1			0.1			0.1		mV
Reference Input Resistance		7			7			7		kΩ
INPUT REFERRED NOISE										
VREF = 0.5 V		1.35			1.35			1.35		LSB rms
VREF = 1.0 V		0.70			0.70			0.70		LSB rms
ANALOG INPUT										
Input Span										
VREF = 0.5 V; MODE2 = 0 V			1			1			1	V p-p
VREF = 1.0 V; MODE2 = 0 V			2			2			2	V p-p
VREF = 0.5 V; MODE2 = AVDD			2			2			2	V p-p
VREF = 1.0 V; MODE2 = AVDD			4			4			4	V p-p
Input Capacitance[3]		7			7			7		pF
POWER SUPPLIES										
Supply Voltages										
AVDD	2.7	3.0	3.6	2.7	3.0	3.6	2.7	3.0	3.6	V
DRVDD	2.25	2.5	3.6	2.25	2.5	3.6	2.25	2.5	3.6	V
Supply Current										
IAVDD[2]		30.5			45.5			64.5		mA
IDRVDD[2]		3.0			4.5			5.5		mA
PSRR		±0.01			±0.01			±0.01		% FSR
POWER CONSUMPTION										
DC Input[4]		85			135			190		mW
Sine Wave Input[2]		100	120		150	180		210	270	mW
Power-Down Mode		1			1			1		mW
Standby Power		20			20			20		mW

[1] Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.0 V external reference).
[2] Measured at maximum clock rate, f_{IN} = 2.4 MHz, full-scale sine wave, with approximately 5 pF loading on each output bit.
[3] Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 4 for the equivalent analog input structure.
[4] Measured with dc input at maximum clock rate.

DIGITAL SPECIFICATIONS

Table 2.

Parameter	AD9237BCP-20 Min	AD9237BCP-20 Typ	AD9237BCP-20 Max	AD9237BCP-40 Min	AD9237BCP-40 Typ	AD9237BCP-40 Max	AD9237BCP-65 Min	AD9237BCP-65 Typ	AD9237BCP-65 Max	Unit
LOGIC INPUTS										
High Level Input Voltage	2.0			2.0			2.0			V
Low Level Input Voltage			0.8			0.8			0.8	V
High Level Input Current	−10		+10	−10		+10	−10		+10	µA
Low Level Input Current	−10		+10	−10		+10	−10		+10	µA
Input Capacitance		2			2			2		pF
LOGIC OUTPUTS[1]										
DRVDD = 3.3 V										
High-Level Output Voltage (IOH = 50 µA)	3.29			3.29			3.29			V
High-Level Output Voltage (IOH = 0.5 mA)	3.25			3.25			3.25			V
Low-Level Output Voltage (IOL = 1.6 mA)			0.2			0.2			0.2	V
Low-Level Output Voltage (IOL = 50 µA)			0.05			0.05			0.05	V
DRVDD = 2.5 V										
High-Level Output Voltage (IOH = 50 µA)	2.49			2.49			2.49			V
High-Level Output Voltage (IOH = 0.5 mA)	2.45			2.45			2.45			V
Low-Level Output Voltage (IOL = 1.6 mA)			0.2			0.2			0.2	V
Low-Level Output Voltage (IOL = 50 µA)			0.05			0.05			0.05	V

[1] Output voltage levels measured with 5 pF load on each output.

AC SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, maximum sample rate, 2 V p-p differential input, A_{IN} = –0.5 dBFS, 1.0 V internal reference, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	AD9237BCP-20 Min	AD9237BCP-20 Typ	AD9237BCP-20 Max	AD9237BCP-40 Min	AD9237BCP-40 Typ	AD9237BCP-40 Max	AD9237BCP-65 Min	AD9237BCP-65 Typ	AD9237BCP-65 Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)										
f_{INPUT} = 2.4 MHz		66.8			66.5			66.5		dBc
f_{INPUT} = 9.7 MHz	65.6	66.6								dBc
f_{INPUT} = 19.6 MHz				65.3	66.6					dBc
f_{INPUT} = 34.2 MHz							64.0	66.1		dBc
f_{INPUT} = 70 MHz		66.0			66.3			65.9		dBc
SIGNAL-TO-NOISE RATIO AND DISTORTION (SINAD)										
f_{INPUT} = 2.4 MHz		66.7			66.4			66.3		dBc
f_{INPUT} = 9.7 MHz	65.1	66.5								dBc
f_{INPUT} = 19.6 MHz				64.4	66.4					dBc
f_{INPUT} = 34.2 MHz							63.5	65.8		dBc
f_{INPUT} = 70 MHz		65.6			65.8			65.2		dBc
EFFECTIVE NUMBER OF BITS (ENOB)										
f_{INPUT} = 9.7 MHz		10.8								Bits
f_{INPUT} = 19.6 MHz					10.7					Bits
f_{INPUT} = 34.2 MHz								10.6		Bits

Parameter	AD9237BCP-20 Min	Typ	Max	AD9237BCP-40 Min	Typ	Max	AD9237BCP-65 Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)										
f_{INPUT} = 2.4 MHz		88.0			83.5			85.5		dBc
f_{INPUT} = 9.7 MHz	72.4	87.5								dBc
f_{INPUT} = 19.6 MHz				72.2	82.4					dBc
f_{INPUT} = 34.2 MHz							69.4	80.1		dBc
f_{INPUT} = 70 MHz		80.5			77.9			74.9		dBc
WORST HARMONIC (SECOND OR THIRD)										
f_{INPUT} = 2.4 MHz		−88.0			−83.5			−85.5		dBc
f_{INPUT} = 9.7 MHz	−72.4	−87.5								dBc
f_{INPUT} = 19.6 MHz				−72.2	−82.4					dBc
f_{INPUT} = 34.2 MHz							−69.4	−80.1		dBc
f_{INPUT} = 70 MHz		−80.5			−77.9			−74.9		dBc
WORST OTHER SPUR										
f_{INPUT} = 2.4 MHz		−90			−90			−90		dBc
f_{INPUT} = 9.7 MHz	−73.4	−90								dBc
f_{INPUT} = 19.6 MHz				−73.1	−90					dBc
f_{INPUT} = 34.2 MHz							−72.0	−90		dBc
f_{INPUT} = 70 MHz		−90			−90			−90		dBc

SWITCHING SPECIFICATIONS

Table 4.

Parameter	AD9237BCP-20 Min	Typ	Max	AD9237BCP-40 Min	Typ	Max	AD9237BCP-65 Min	Typ	Max	Unit
CLK INPUT PARAMETERS										
Maximum Conversion Rate	20			40			65			MSPS
Minimum Conversion Rate			1			1			1	MSPS
CLK Period	50.0			25.0			15.4			ns
CLK Pulse Width High[1]	15.0			8.8			6.2			ns
CLK Pulse Width Low[1]	15.0			8.8			6.2			ns
DATA OUTPUT PARAMETERS										
Output Delay (t_{PD})[2]		3.5			3.5			3.5		ns
Pipeline Delay (Latency)		9			9			9		Cycles
Output Enable Time		6			6			6		ns
Output Disable Time		3			3			3		ns
Aperture Delay (t_A)		1.0			1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)		0.5			0.5			0.5		ps rms
Wake-Up Time (Sleep Mode)[3]		3.0			3.0			3.0		ms
Wake-Up Time (Standby Mode)[3]		3.0			3.0			3.0		µs
OUT-OF-RANGE RECOVERY TIME		1			1			2		Cycles

[1] With duty cycle stabilizer enabled.
[2] Output delay is measured from CLK 50% transition to DATA 50% transition, with 5 pF load on each output.
[3] Wake-up time is dependent on value of decoupling capacitors; typical values shown with 0.1 µF and 10 µF capacitors on REFT and REFB.

TIMING DIAGRAM

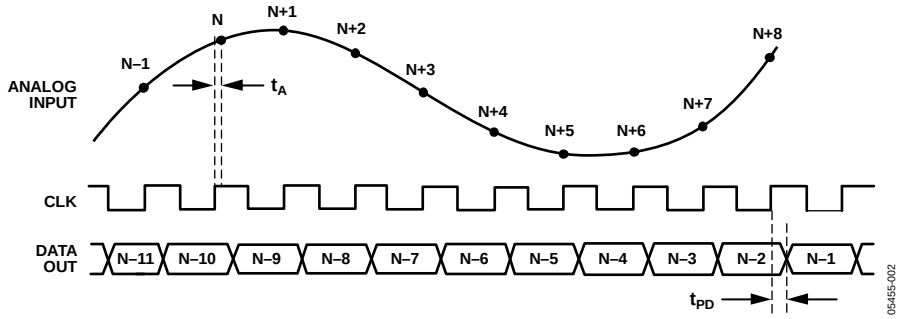

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Pin Name	With Respect to	Min	Max	Unit
ELECTRICAL				
AVDD	AGND	−0.3	+3.9	V
DRVDD	DGND	−0.3	+3.9	V
AGND	DGND	−0.3	+0.3	V
AVDD	DRVDD	−3.9	+3.9	V
Digital Outputs, OE	DGND	−0.3	DRVDD + 0.3	V
CLK, MODE, MODE2	AGND	−0.3	AVDD + 0.3	V
VIN+, VIN−	AGND	−0.3	AVDD + 0.3	V
VREF	AGND	−0.3	AVDD + 0.3	V
SENSE	AGND	−0.3	AVDD + 0.3	V
REFB, REFT	AGND	−0.3	AVDD + 0.3	V
PDWN	AGND	−0.3	AVDD + 0.3	V
ENVIRONMENTAL[1]				
Operating Temperature		−40	+85	°C
Junction Temperature			150	°C
Lead Temperature (10 sec)			300	°C
Storage Temperature		−65	+150	°C

[1] Typical thermal impedances (32-lead LFCSP), θ_{JA} = 32.5°C/W, θ_{JC} = 32.71°C/W. These measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-1.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

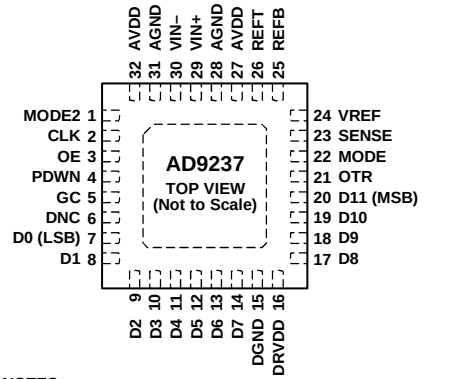

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	MODE2	SHA Gain Select and Power Scaling Control (see Table 8).
2	CLK	Clock Input Pin.
3	OE	Output Enable Pin (Active Low).
4	PDWN	Power-Down Function Selection (see Table 9).
5	GC	Gray Code Control (Active High).
6	DNC	Do Not Connect.
7 to 14, 17 to 20	D0 (LSB) to D11 (MSB)	Data Output Bits.
15	DGND	Digital Output Ground.
16	DRVDD	Digital Output Driver Supply. Must be decoupled to DGND with a minimum 0.1 µF capacitor. Recommended decoupling is 0.1 µF in parallel with 10 µF.
21	OTR	Out-of-Range Indicator.
22	MODE	Data Format and Clock Duty Cycle Stabilizer (DCS) Mode Selection (see Table 10).
23	SENSE	Reference Mode Selection (see Table 7).
24	VREF	Voltage Reference Input/Output (see Table 7).
25	REFB	Differential Reference (–). Must be decoupled to REFT with a minimum 10 µF capacitor.
26	REFT	Differential Reference (+).
27, 32	AVDD	Analog Power Supply. Must be decoupled to AGND with a minimum 0.1 µF capacitor. Recommended decoupling is 0.1 µF in parallel with 10 µF.
28, 31	AGND	Analog Ground.
29	VIN+	Analog Input Pin (+).
30	VIN–	Analog Input Pin (–).
EP		It is recommended that the exposed paddle be soldered to the ground plane. There is an increased reliability of the solder joints and maximum thermal capability of the package is achieved with exposed paddle soldered to the customer board.

TERMINOLOGY

Analog Bandwidth (Full Power Bandwidth)
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay (t_A)
The delay between the 50% point of the rising edge of the clock and the instant at which the analog input is sampled.

Aperture Jitter (t_J)
The sample-to-sample variation in aperture delay.

Integral Nonlinearity (INL)
The deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSBs beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes must be present over all operating ranges.

Offset Error
The major carry transition should occur for an analog value ½ LSB below VIN+ = VIN−. Offset error is defined as the deviation of the actual transition from that point.

Gain Error
The first code transition should occur at an analog value ½ LSB above negative full scale. The last transition should occur at an analog value 1½ LSB below the positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Temperature Drift
The temperature drift for offset error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection Ratio
The change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Total Harmonic Distortion (THD)[1]
The ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal.

Signal-To-Noise and Distortion (SINAD)[1]
The ratio of the rms signal amplitude to the rms value of the sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

Effective Number of Bits (ENOB)
The effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD using the following formula:

$$ENOB = (SINAD_{dBFS} - 1.76)/6.02$$

Signal-to-Noise Ratio (SNR)[1]
The ratio of the rms signal to the rms value of the sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc.

Spurious-Free Dynamic Range (SFDR)[1]
SFDR is the difference in dB between the rms amplitude of the input signal and the rms value of the peak spurious signal. The peak spurious signal may not be an harmonic.

Two-Tone SFDR[1]
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product.

Clock Pulse Width and Duty Cycle
Pulse width high is the minimum amount of time that the clock pulse should be left in the Logic 1 state to achieve rated performance. Pulse width low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

Minimum Conversion Rate
The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The clock rate at which parametric testing is performed.

Output Propagation Delay (t_{PD})
The delay between the clock logic threshold and the time when all bits are within valid logic levels.

Out-of-Range Recovery Time
The time it takes the ADC to reacquire the analog input after a transition from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

[1] AC specifications may be reported in dBc (degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).

EQUIVALENT CIRCUITS

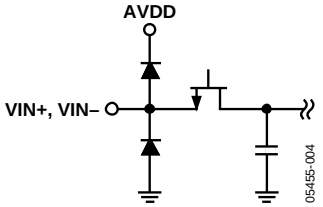

Figure 4. Equivalent Analog Input Circuit

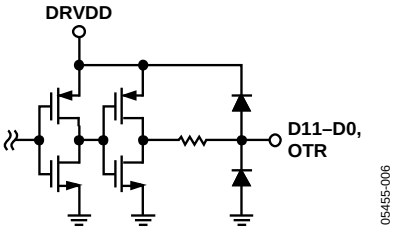

Figure 6. Equivalent Digital Output Circuit

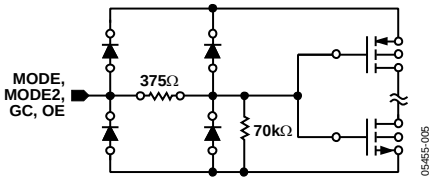

Figure 5. Equivalent MODE, MODE2, GC, OE Input Circuit

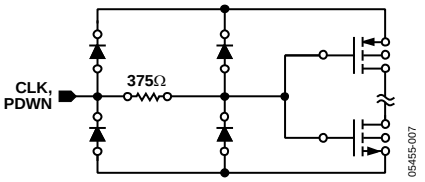

Figure 7. Equivalent CLK, PDWN Input Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 3.0 V, DRVDD = 2.5 V, maximum sample rate with DCS disabled, T_A = 25°C, 2 V p-p differential input, A_{IN} = −0.5 dBFS, VREF = 1.0 V internal, FFT length 16 K, unless otherwise noted.

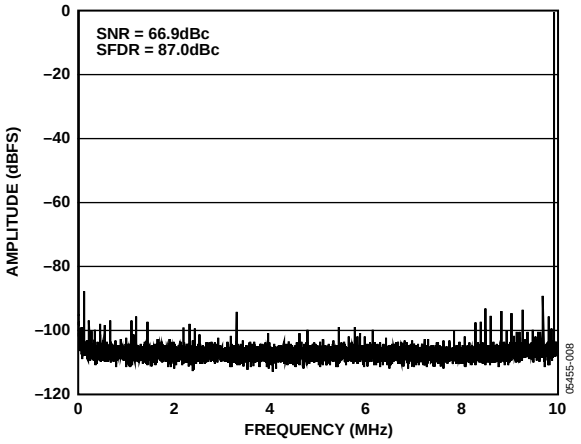

Figure 8. AD9237-20 10 MHz FFT

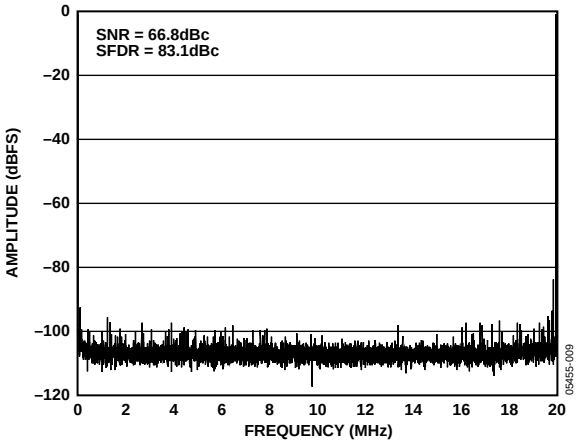

Figure 9. AD9237-40 20 MHz FFT

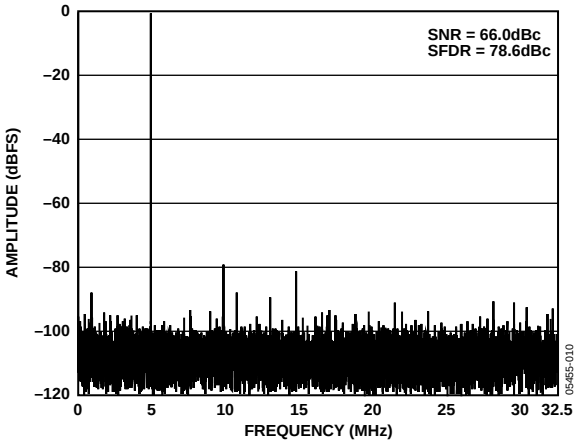

Figure 10. AD9237-65 70 MHz FFT

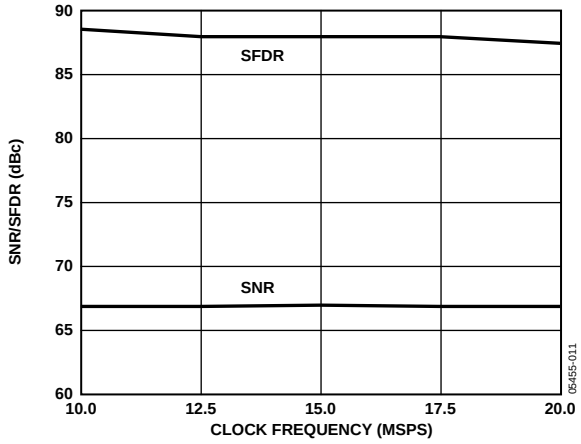

Figure 11. AD9237-20 SNR/SFDR vs. Clock Frequency with f_{IN} = 10 MHz

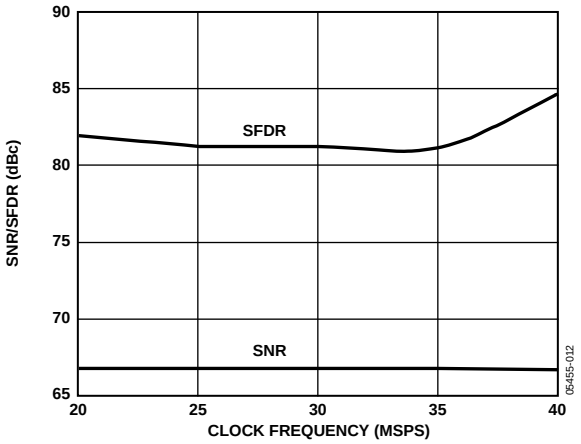

Figure 12. AD9237-40 SNR/SFDR vs. Clock Frequency with f_{IN} = 20 MHz

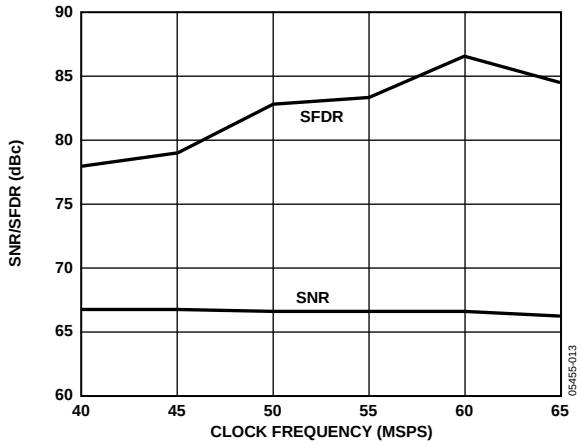

Figure 13. AD9237-65 SNR/SFDR vs. Clock Frequency with f_{IN} = 35 MHz

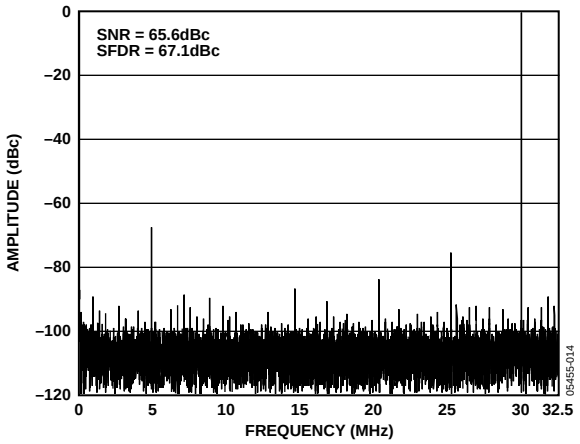

Figure 14. AD9237-65 100 MHz FFT

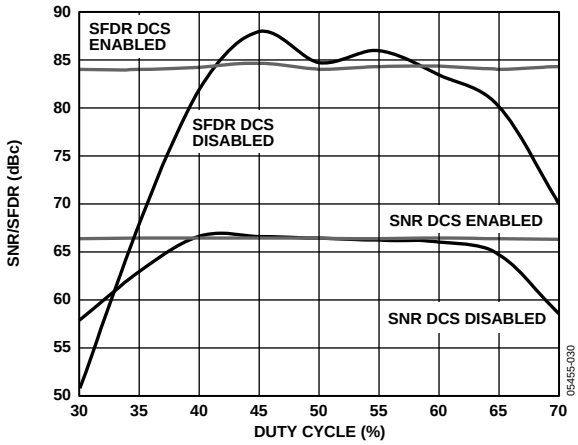

Figure 17. SNR/SFDR vs. Clock Duty Cycle

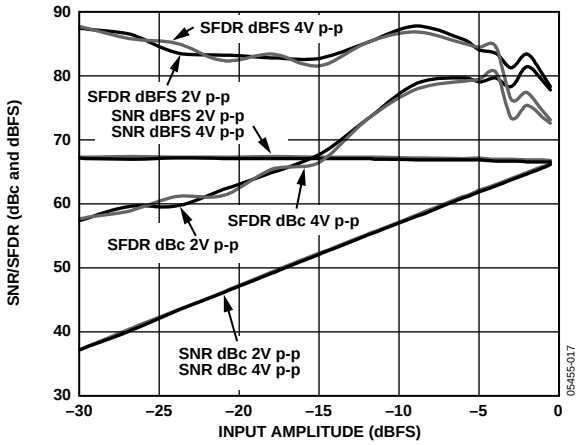

Figure 15. AD9237-65 SNR/SFDR vs. Input Amplitude with f_{IN} = 35 MHz

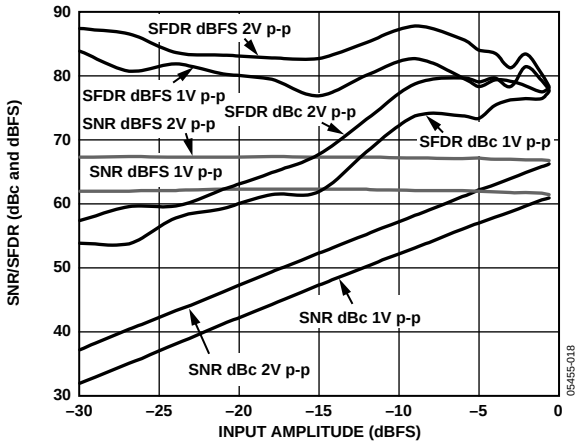

Figure 18. AD9237-65 SNR/SFDR vs. Input Amplitude with f_{IN} = 35 MHz

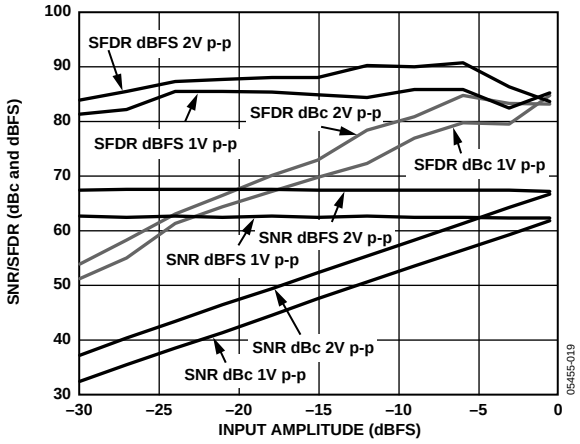

Figure 16. AD9237-40 SNR/SFDR vs. Input Amplitude with f_{IN} = 20 MHz

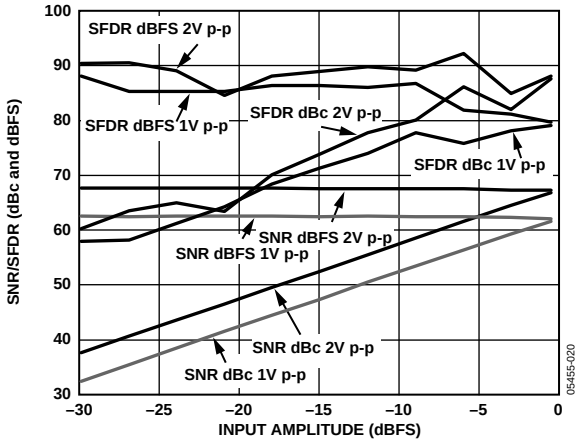

Figure 19. AD9237-20 SNR/SFDR vs. Input Amplitude with f_{IN} = 10 MHz

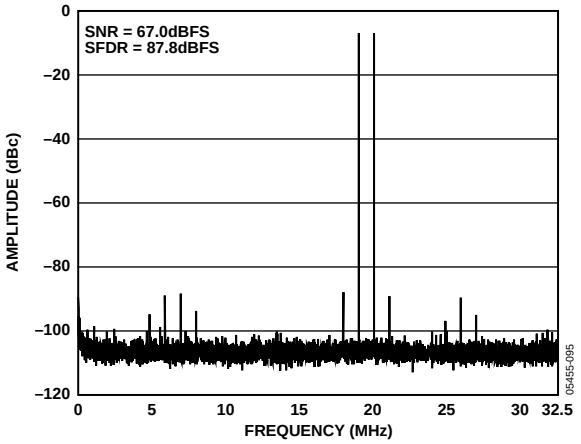

Figure 20. AD9237-65 Two-Tone FFT, f_{IN1} = 45 MHz, f_{IN2} = 46 MHz

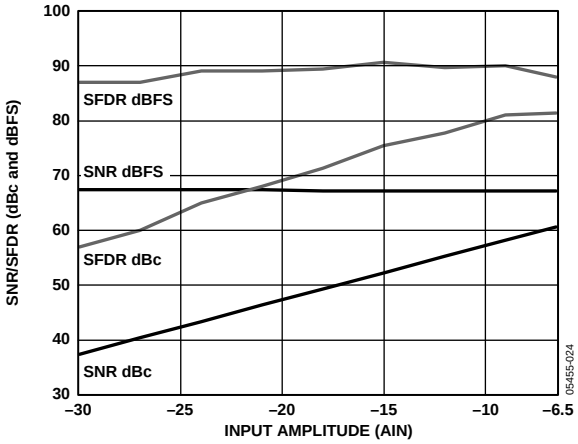

Figure 23. AD9237-65 Two-Tone SNR/SFDR , vs. Analog Input with f_{IN1} = 45 MHz, f_{IN2} = 46 MHz

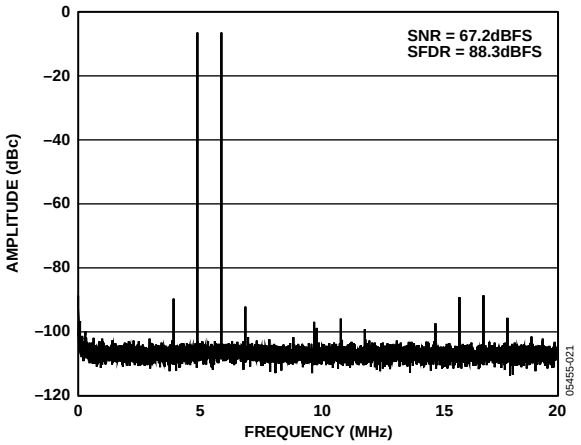

Figure 21. AD9237-40 Two-Tone FFT
f_{IN1} = 45 MHz, f_{IN2} = 46 MHz

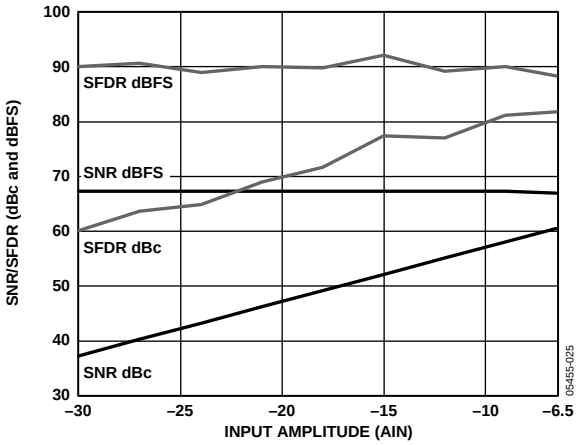

Figure 24. AD9237-40 Two-Tone SNR/SFDR , vs. Analog Input with f_{IN1} = 45 MHz, f_{IN2} = 46 MHz

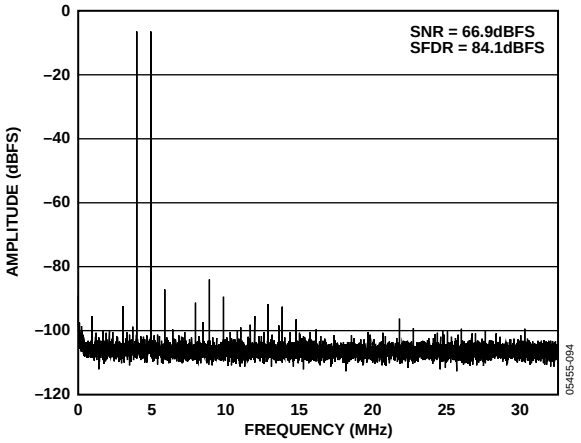

Figure 22. AD9237-65 Two-Tone FFT, f_{IN1} = 69 MHz, f_{IN2} = 70 MHz

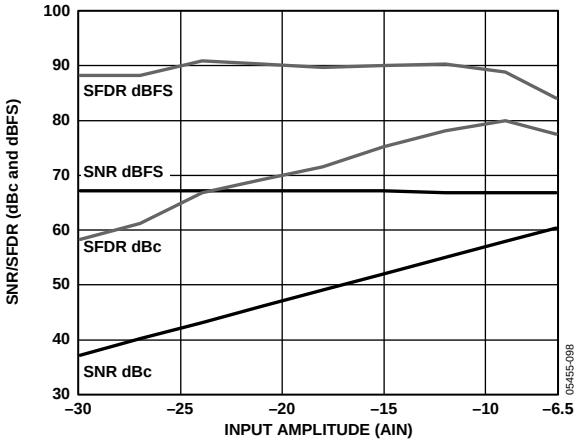

Figure 25. AD9237-65 Two-Tone SNR/SFDR vs. Analog Input with f_{IN1} = 69 MHz, f_{IN2} = 70 MHz

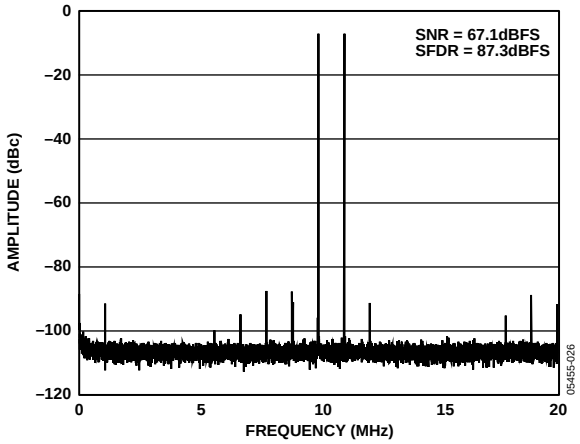

Figure 26. AD9237-40 Two-Tone FFT
f_{IN1} = 69 MHz, f_{IN2} = 70 MHz

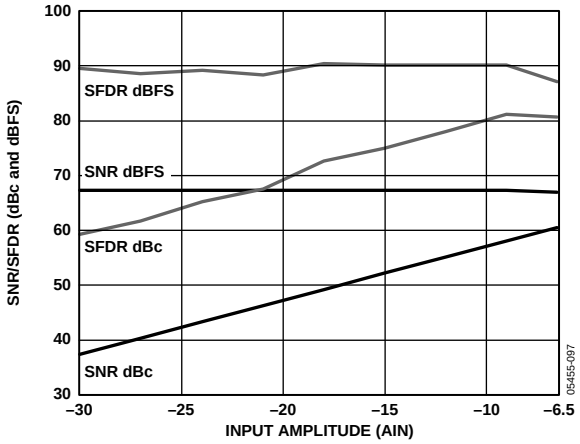

Figure 29. AD9237-40 Two-Tone SNR/SFDR vs. Analog Input with
f_{IN1} = 69 MHz, f_{IN2} = 70 MHz

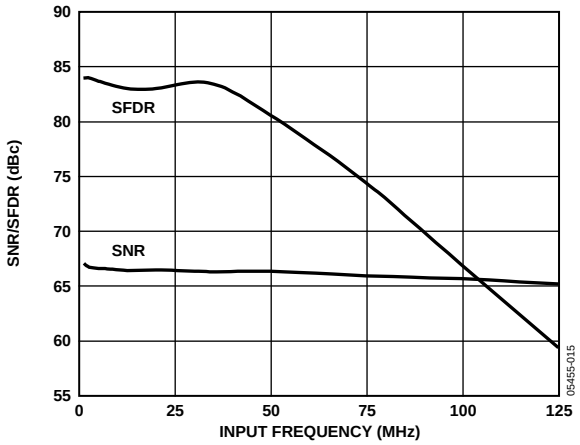

Figure 27. AD9237-65 SNR/SFDR vs. Input Frequency

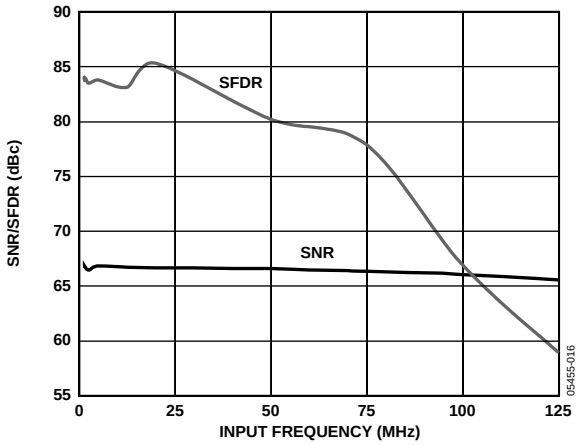

Figure 30. AD9237-40 SNR/SFDR vs. Input Frequency

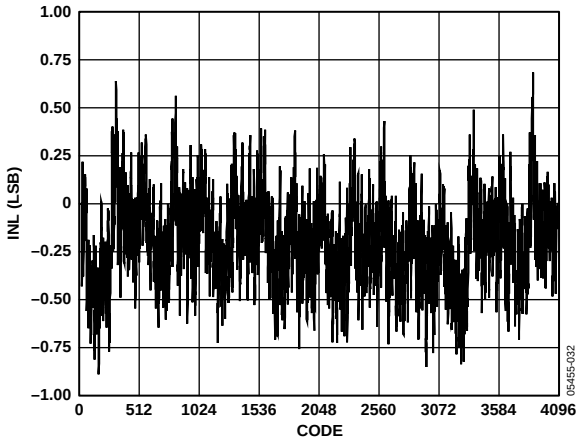

Figure 28. Typical INL

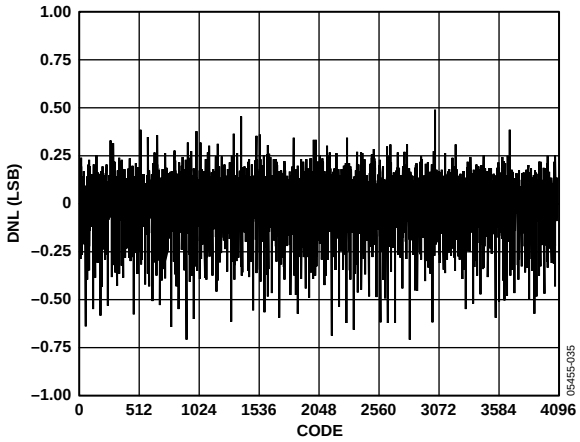

Figure 31. Typical DNL

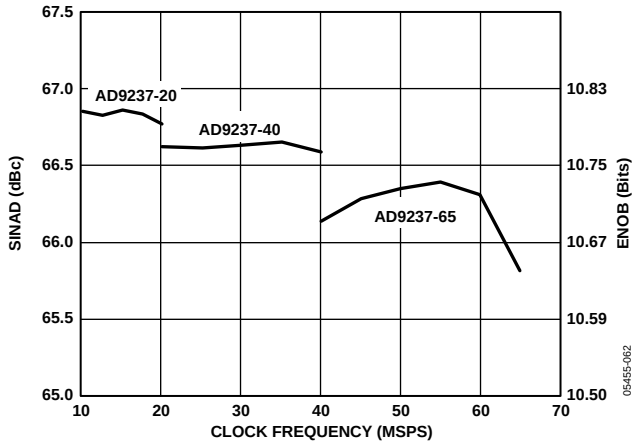

Figure 32. AD9237 SINAD/ENOB vs. Clock Frequency with f_{IN} = Nyquist

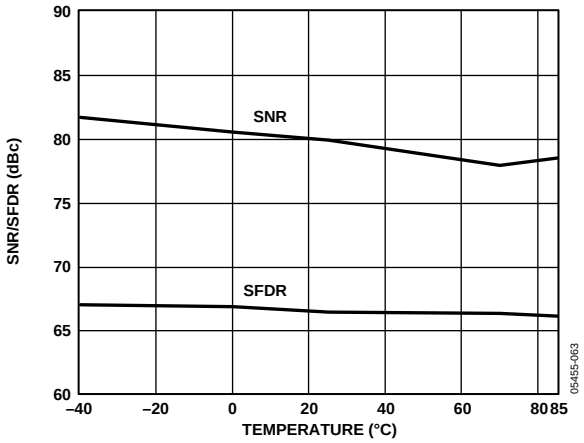

Figure 33. AD9237-65 SNR/SFDR vs. Temperature with f_{IN} = 32.5MHz

APPLYING THE AD9237

THEORY OF OPERATION

The AD9237 uses a calibrated, 11-stage pipeline architecture with a patented input SHA implemented. Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage consists of a flash ADC.

The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. While the converter captures a new input sample every clock cycle, it takes eight clock cycles for the conversion to be fully processed and to appear at the output, as shown in Figure 2.

The input stage contains a differential SHA that can be ac- or dc-coupled in differential or single-ended modes. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down and stand-by operation, the output buffers go into a high impedance state.

The ADC samples the analog input on the rising edge of the clock. System disturbances just prior to, or immediately following, the rising edge of the clock and/or excessive clock jitter can cause the SHA to acquire the wrong input value and should be minimized.

ANALOG INPUT AND REFERENCE OVERVIEW

The analog input to the AD9237 is a differential switched capacitor SHA that has been designed for optimum performance while processing a differential input signal. The SHA input can support a wide common-mode range and maintain excellent performance, as shown in Figure 34. An input common-mode voltage of midsupply minimizes signal-dependant errors and provides optimum performance.

Figure 35 shows the clock signal alternately switching the SHA between sample mode and hold mode. When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source.

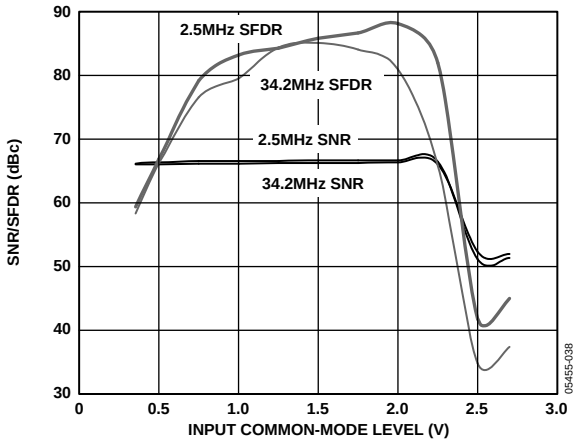

Figure 34. AD9237-65 SNR/SFDR vs. Input Common-Mode Level

In addition, a small shunt capacitor placed across the inputs provides dynamic charging currents. This passive network creates a low-pass filter at the ADC's input; therefore, the precise values are dependent on the application. In IF under-sampling applications, the shunt capacitor(s) should be reduced or removed depending on the input frequency. In combination with the driving source impedance, the capacitors limit the input bandwidth.

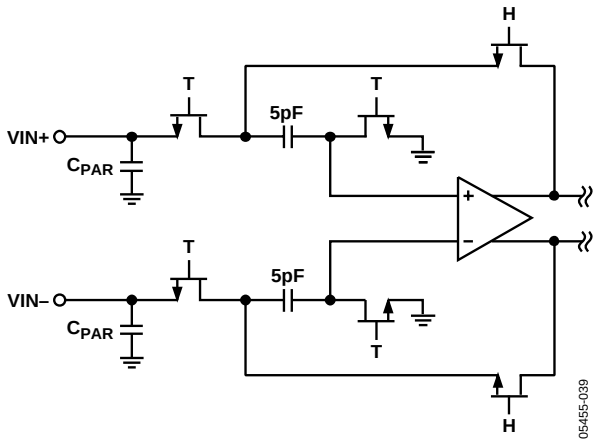

Figure 35. Switched-Capacitor SHA Input

For best dynamic performance, the source impedances driving VIN+ and VIN– should be matched so that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

An internal differential reference buffer creates positive and negative reference voltages, REFT and REFB, that define the span of the ADC core.

The output common mode of the reference buffer is set to mid-supply, and the REFT and REFB voltages and input span are defined as:

$$REFT = ½(AVDD + VREF)$$

$$REFB = ½(AVDD - VREF)$$

$$Span = \frac{4 \times (REFT - REFB)}{Span\_Factor} = \frac{4 \times VREF}{Span\_Factor}$$

The previous equations show that the REFT and REFB voltages are symmetrical about the midsupply voltage, and the input span is proportional to the value of the VREF voltage, see Table 7 for more details.

The internal voltage reference can be pin strapped to fixed values of 0.5 V or 1.0 V, or adjusted within this range as discussed in the Internal Reference Connection section. Maximum SNR performance is achieved with the AD9237 set to an input span of 2 V p-p or greater. The relative SNR degradation is 3 dB when changing from 2 V p-p mode to 1 V p-p mode.

The SHA must be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined as:

$$VCM_{MIN} = VREF/2$$

$$VCM_{MAX} = (AVDD + VREF)/2$$

The minimum common-mode input level allows the AD9237 to accommodate ground-referenced inputs.

Although optimum performance is achieved with a differential input, a single-ended source can be driven into VIN+ or VIN–. In this configuration, one input accepts the signal while the opposite input should be set to midscale by connecting it to an appropriate reference. For example, a 2 V p-p signal can be applied to VIN+ while a 1 V reference is applied to VIN–. The AD9237 then accepts an input signal varying between 2 V and 0 V. In the single-ended configuration, distortion performance may degrade significantly as compared to the differential case. However, the effect is less noticeable at lower input frequencies and in the lower speed grade models (AD9237-40 and AD9237-20).

Differential Input Configurations

As previously detailed, optimum performance is achieved while driving the AD9237 in a differential input configuration. For baseband applications, the AD8351 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8351 is easily set to AVDD/2, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal. Figure 36 details a typical configuration using the AD8351.

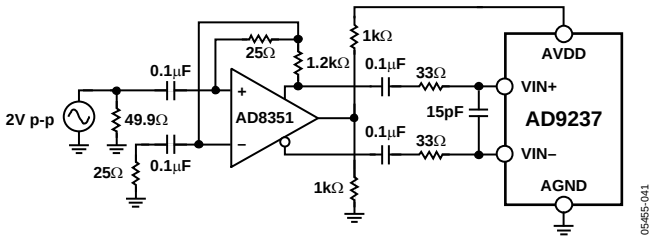

Figure 36. Differential Input Configuration Using the AD8351

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers is not adequate to achieve the true performance of the AD9237. This is especially true in IF undersampling applications where frequencies in the 70 MHz to 100 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration, as shown in Figure 37.

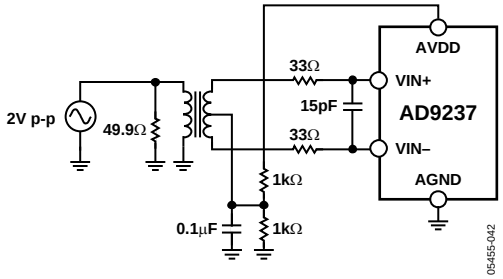

Figure 37. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can cause core saturation, which leads to distortion.

Single-Ended Input Configuration

A single-ended input can provide adequate performance in cost-sensitive applications. In this configuration, there is degradation in SFDR and distortion performance due to the large input common-mode swing. However, if the source impedances on each input are matched, there should be little effect on SNR performance. Figure 38 details a typical single-ended input configuration.

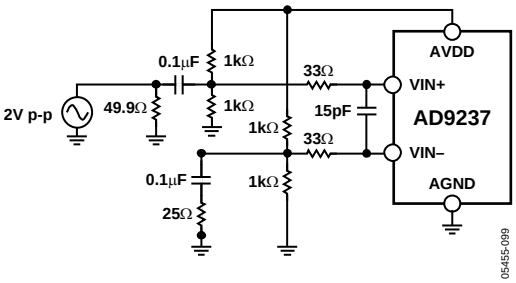

Figure 38. Single-Ended Input Configuration

Table 7. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting VREF (V)	Span Factor	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 1	$\frac{4 \times External\ Reference}{Span\_Factor}$
Internal Fixed Reference	VREF	0.5	2 1	1.0 V 2.0 V
Programmable Reference	0.2 V to VREF	0.5 × (1 + R2/R1) (See Figure 40)	2 1	$\frac{4 \times VREF}{Span\_Factor}$
Internal Fixed Reference	AGND to 0.2 V	1.0	2 1	2.0 V 4.0 V

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9237. The input range can be adjusted by varying the reference voltage applied to the AD9237, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly.

In all reference configurations, REFT and REFB drive the A/D conversion core and, in conjunction with the span factor, establish its input span. The input range of the ADC always equals four times the voltage at the reference pin divided by the span factor for either an internal or an external reference. It is required to decouple REFT to REFB with 0.1 µF and 10 µF decoupling capacitors, as shown in Figure 39.

Internal Reference Connection

A comparator within the AD9237 detects the potential at the SENSE pin and configures the reference into one of four possible states, which are summarized in Table 7. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider, setting VREF to 1 V (see Figure 39). Connecting the SENSE pin to VREF switches the reference amplifier output to the SENSE pin, completing the loop and providing a 0.5 V reference output. If a resistor divider is connected, as shown in Figure 40, then the switch is again set to the SENSE pin. This puts the reference amplifier in a non-inverting mode with the VREF output defined as

$$VREF = 0.5 \times \left(1 + \frac{R2}{R1}\right)$$

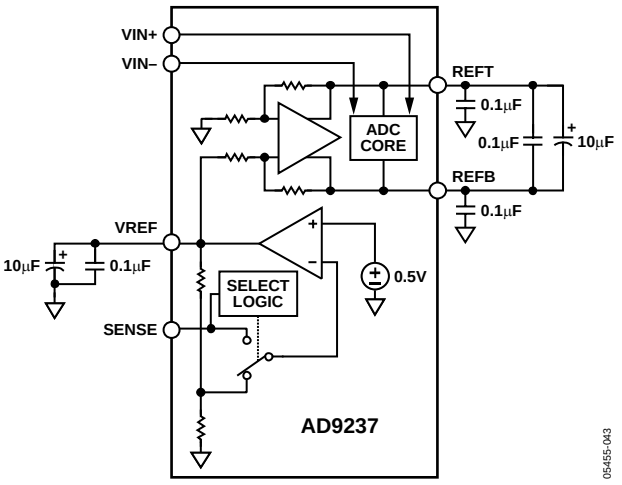

Figure 39. Internal Reference Configuration

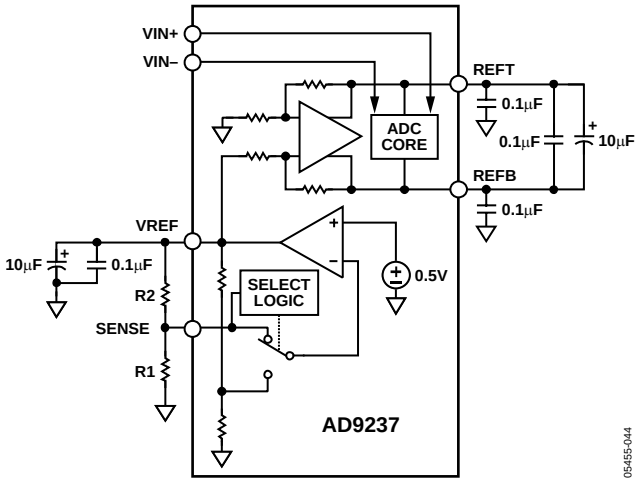

Figure 40. Programmable Reference Configuration

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or to improve thermal drift characteristics. Figure 41 shows the typical drift characteristics of the internal reference in both 1 V and 0.5 V modes. When multiple ADCs track one another, a single reference (internal or external) reduces gain matching errors.

When the SENSE pin is connected to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7 kΩ load. The internal buffer still generates the positive and negative full-scale references, REFT and REFB, for the ADC core. The input span is always four times the value of the reference voltage divided by the span factor; therefore, the external reference must be limited to a maximum of 1 V.

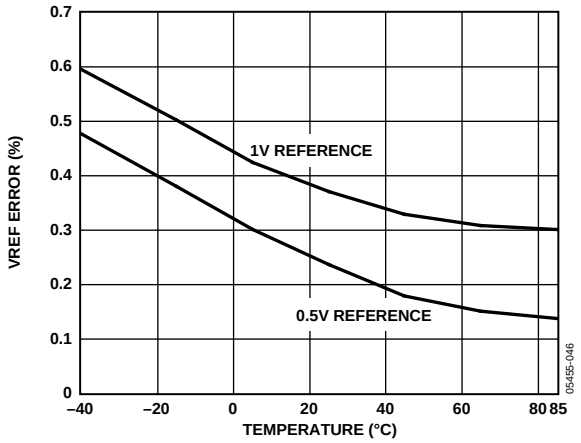

Figure 41. Typical VREF Drift

If the internal reference of the AD9237 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 42 shows how the internal reference voltage is affected by loading. A 2 mA load is the maximum recommended load.

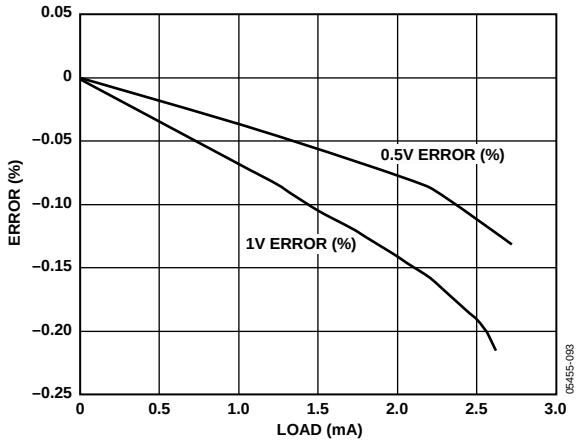

Figure 42. VREF Accuracy vs. Load

CLOCK INPUT CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, can be sensitive to clock duty cycle. Commonly a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9237 contains a clock duty cycle stabilizer (DCS) that retimes the nonsampling, or falling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9237. As shown in Figure 17, noise and distortion performance are nearly flat over a 30% range of duty cycle with the DCS enabled.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately 100 clock cycles to allow the DLL to acquire and lock to the new rate.

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{INPUT}) due only to rms aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = 20\log_{10}\left[\frac{1}{2\pi f_{INPUT} t_J}\right]$$

In this equation, the rms aperture jitter represents the root-sum-square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. Undersampling applications are particularly sensitive to jitter.

The clock input should be treated as an analog signal in cases where aperture jitter can affect the dynamic range of the AD9237. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (such as gating, dividing, or other methods), then it should be retimed by the original clock at the last step.

The lowest typical conversion rate of the AD9237 is 1 MSPS. At clock rates below 1 MSPS, dynamic performance may degrade.

POWER DISSIPATION, POWER SCALING, AND STANDBY MODE

As shown in Figure 43, the power dissipated by the AD9237 is proportional to its sample rate. The digital power dissipation does not vary substantially between the three speed grades because it is determined primarily by the strength of the digital drivers and the load on each output bit. The maximum DRVDD current can be calculated as

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLK} \times N$$

where N is 12, the number of output bits.

This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency, $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which is determined by the encode rate and the characteristics of the analog input signal.

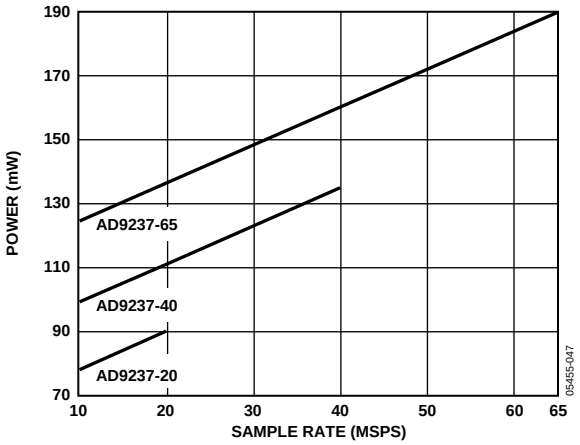

Figure 43. Total Power vs. Sample Rate with f_{IN} = 10 MHz

For the AD9237-20 speed grade, the digital power consumption can represent as much as 10% of the total dissipation. Digital power consumption can be minimized by reducing the capacitive load presented to the output drivers. The data in Figure 43 was taken with a 5 pF load on each output driver.

The AD9237 is designed to provide excellent performance with minimum power. The analog circuitry is optimally biased so that each speed grade provides excellent performance while affording reduced power consumption. Each speed grade dissipates a baseline power at low sample rates that increases linearly with the clock frequency, as shown in Figure 43.

The power scaling feature provides an additional power savings when enabled, as shown in Figure 44. The power scaling mode cannot be enabled if the clock is varied during operation. This is because the internal circuitry cannot quickly track a changing clock, and the part does not have enough power to operate properly.

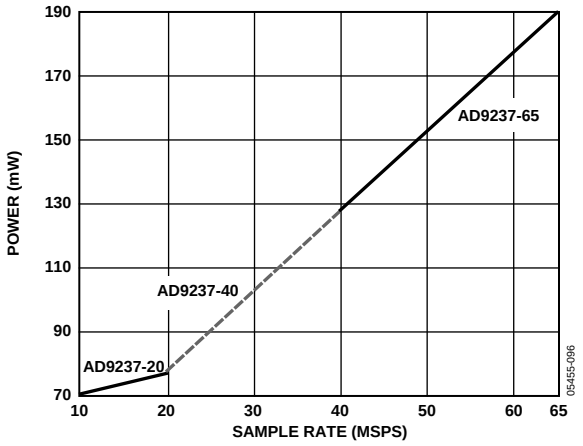

Figure 44. Total Power vs. Sample Rate with Power Scaling Enabled

The MODE2 pin is a multilevel input that controls the span factor and power scaling modes. The MODE2 pin is internally pulled down to AGND by a 70 kΩ resistor. The input threshold and corresponding mode selections are outlined in Table 8.

Table 8. MODE2 Selection

MODE2 Voltage	Span Factor	Power Scaling
AVDD	1	Disabled
2/3 AVDD	1	Enabled
1/3 AVDD	2	Enabled
AGND (Default)	2	Disabled

The PDWN pin is a multilevel input that controls the power states. The input threshold values and corresponding power states are outlined in Table 9.

Table 9. PDWN Selection

PDWN Voltage	Power State	Power (mW)
AVDD	Power-Down Mode	1
1/3 AVDD	Standby Mode	20
AGND (Default)	Normal Operation	Based on speed grade

By asserting the PDWN pin high, the AD9237 is placed in power-down mode. In this state, the ADC typically dissipates 1 mW. During power-down, the output drivers are placed in a high impedance state. Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, clock, and duty cycle stabilizer circuitry. The decoupling capacitors on REFT and REFB are discharged when entering power-down mode and then must be recharged when returning to normal operation.

As a result, the wake-up time is related to the time spent in power-down mode and shorter standby cycles result in proportionally shorter wake-up times. With the recommended 0.1 µF and 10 µF decoupling capacitors on REFT and REFB, it takes approximately 1 sec to fully discharge the reference buffer decoupling capacitors and 3 ms to restore full operation.

By asserting the PDWN pin to AVDD/3, the AD9237 is placed in standby mode. In this state, the ADC typically dissipates 20 mW. The output drivers are placed in a high impedance state. The reference circuitry is enabled, allowing for a quick start upon bringing the ADC into normal operating mode.

DIGITAL OUTPUTS

The AD9237 output drivers can be configured to interface with 2.5 V or 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies that can affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9237; these transients can detract from the converter's dynamic performance.

As detailed in Table 10, the data format can be selected for either offset binary, twos complement, or gray code.

Operational Mode Selection

The AD9237 can output data in either offset binary, twos complement, or gray code format. There is also a provision for enabling or disabling the duty cycle stabilizer (DCS). The MODE pin is a multilevel input that controls the data format (except for gray code) and DCS state. The MODE pin is internally pulled down to AGND by a 70 kΩ resistor. The input threshold values and corresponding mode selections are outlined in Table 10.

The gray code output format is obtained by connecting GC to AVDD. When the part is in gray code mode, the MODE pin controls the DCS function only. The GC pin is internally pulled down to AGND by a 70 kΩ resistor.

Table 10. MODE Selection

MODE Voltage	Data Format	Duty Cycle Stabilizer
AVDD	Twos Complement	Disabled
2/3 AVDD	Twos Complement	Enabled
1/3 AVDD	Offset Binary	Enabled
AGND (Default)	Offset Binary	Disabled

Out of Range (OTR)

An out-of-range condition exists when the analog input voltage is beyond the input range of the ADC. The OTR pin is a digital output that is updated along with the data output corresponding to the particular sampled input voltage. Therefore, the OTR pin has the same pipeline latency as the digital data. OTR is low when the analog input voltage is within the analog input range, and high when the analog input voltage exceeds the input range, as shown in Figure 45. OTR remains high until the analog input returns to within the input range and another conversion is completed. By logically AND-ing OTR with the MSB and its complement, overrange high or underrange low conditions can be detected. Table 11 is a truth table for the overrange/ underrange circuit in Figure 46, which uses NAND gates. Systems requiring programmable gain condition of the AD9237 can, after eight clock cycles, detect an out-of-range condition; therefore, eliminating gain selection iterations. In addition, OTR can be used for digital offset and gain calculation.

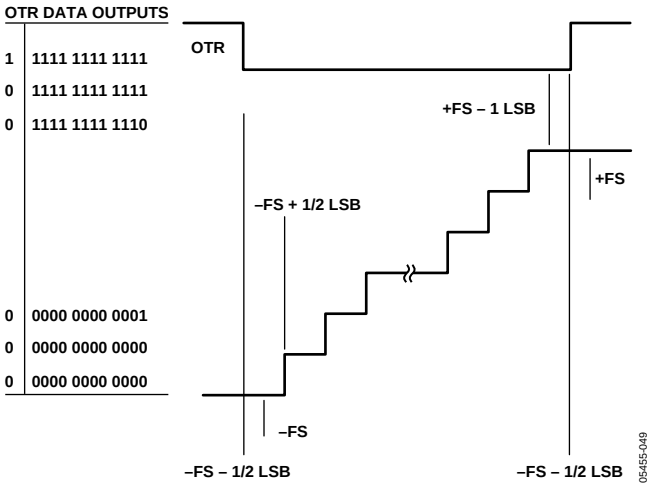

Figure 45. OTR Relation to Input Voltage and Output Data

Table 11. Output Data Format

OTR	MSB	Analog Input Is
0	0	Within range
0	1	Within range
1	0	Underrange
1	1	Overrange

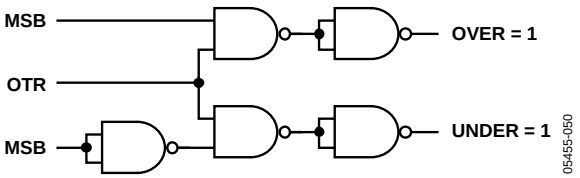

Figure 46. Overrange/Underrange Logic

Digital Output Enable Function (OE)

The AD9237 has three-state ability. The OE pin is internally pulled down to AGND by a 70 kΩ resistor. If the OE pin is low, the output data drivers are enabled. If the OE pin is high, the output data drivers are placed in a high impedance state. It is not intended for rapid access to the data bus. Note that the OE pin is referenced to the digital supplies (DRVDD) and should not exceed that voltage.

Timing

The AD9237 provides latched data outputs with a pipeline delay of eight clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal. Refer to Figure 2 for a detailed timing diagram.

OUTLINE DIMENSIONS

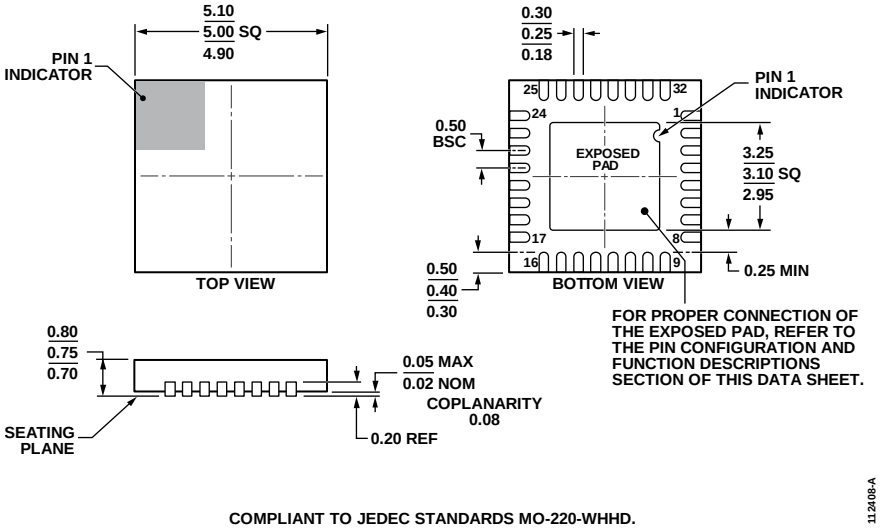

Figure 47. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AD9237BCPZ-40	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-7
AD9237BCPZRL7-40	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-7

[1] Z = RoHS-Compliant Part.
[2] Formerly CP-32-2 package.

NOTES

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D05455–0–8/14(C)