PIC18F47J53 Family
Silicon Errata and Data Sheet Clarification

The PIC18F47J53 Family devices that you have received conform functionally to the current Device Data Sheet (DS39964**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F47J53 Family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F47J53 Family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A1
PIC18F47J53	2C7h	01h
PIC18F46J53	2C5h	
PIC18F27J53	2C3h	
PIC18F26J53	2C1h	
PIC18LF47J53	2D7h	
PIC18LF46J53	2D5h	
PIC18LF27J53	2D3h	
PIC18LF26J53	2D1h	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC18F2XJXX/4XJXX Family Flash Microcontroller Programming Specification"* (DS39687) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A1
CTMU	Constant Current Source	1.	Band gap must be manually enabled before using the CTMU.	X
Oscillator Configurations	PLL	2.	PLL can not be enabled unless the 8 or 4 MHz INTOSC option is set.	X
ADC	A/D	3.	ANx pin may output a pull-up pulse during acquisition.	X
EUSART	Receive Baud Rate	4.	Receive and transmit baud rates differ due to different clock sources.	X
MSSP	I^2C™ Mode	5.	If a Stop condition occurs in the middle of an address or data reception, there will be issues with the SCL clock stream and RCEN bit.	X
MSSP	I^2C Slave Reception	6.	In I^2C slave reception, the module may have problems receiving correct data.	X
EUSART	Enable/ Disable	7.	If interrupts are enabled, disabling and re-enabling the module requires a 2 TCY delay.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: Charge Time Measurement Unit (CTMU)

When using the CTMU, the constant current source may not output if the internal band gap reference is not enabled.

Work around

Before using the CTMU, the internal band gap reference module should be manually enabled by setting the VBGEN bit to '1' (ANCON1<7> = 1).

Affected Silicon Revisions

A1							
X							

2. Module: Phase Locked Loop (PLL)

When OSCCON<6:4> are configured to settings other than a 4 MHz or 8 MHz INTOSC postscaler, the PLLEN bit (OSCTUNE<6>) is forced to '0', even if firmware tries to set the PLLEN bit. This may prevent firmware from enabling the PLL.

Work around

Before attempting to set the PLLEN bit, configure OSCCON<6:4> to '0b110' or '0b111' to select the 4 MHz or 8 MHz INTOSC postscaler.

Affected Silicon Revisions

A1							
X							

3. Module: Analog-to-Digital Converter (ADC)

At the beginning of sample acquisition, one or more small pull-up pulses (approximately 25 ns long) may output to the currently selected ANx analog channel. These pulses can lead to a positive offset error when the analog signal voltage is near VSS and the external analog signal driver is unable to dissipate the added pull-up voltage before the A/D conversion occurs.

Work around

Do one or more of the following:

- Use the "0 TAD" A/D acquisition time setting to start the next sample acquisition period immediately following an A/D conversion completion.

  This allows the external analog signal driver more time to dissipate the pull-up pulses that occur when the sample acquisition is started.
- Use a longer A/D acquisition time setting to provide time for the external analog signal driver to dissipate the pull-up pulse voltage.
- Use low-impedance, active analog signal drivers to reduce the time needed to dissipate the pull-up pulse voltage.
- Experiment with external filter capacitor values to avoid allowing the pull-up voltage offset to affect the final voltage that gets converted.

Small filter capacitor values (or none at all) will allow time for the external analog signal driver to dissipate the pull-up voltage quickly. Alternately, large filter capacitor values will prevent the short pull-up pulses from increasing the final voltage enough to cause an A/D conversion error.

Affected Silicon Revisions

A1							
X							

4. Module: EUSART (Receive Baud Rate)

The EUSART may transmit and receive at different baud rates under the following circumstances:

- a system clock source other than the Secondary Oscillator has been selected, and
- a CPU clock divider (CPDIV<1:0>, CONFIG1H<1:0>) other than 1:1 has been programmed.

This is because the receive baud rate clock source is generated from a point prior to the CPU prescaler, while the rest of the logic is clocked at the system clock frequency (following the prescaler).

Work around

Several work arounds are presented; others may be available.

- If possible, use only a CPU divider of 1:1 (CPDIV<1:0> = 11).
- If the EUSART is being used to receive data only, calculate the baud rate on the predivided clock frequency. For example, if the system clock frequency is 8 MHz and a CPU divider setting of 2 is being used, use a clock frequency of 16 MHz to calculate baud rate.
- Use two USART modules for communication: one to transmit data, and one to receive. Calculate the baud rate for the receive USART as described in the previous work around. Calculate the transmit baud rate normally using the actual (post-divider) clock speed.

Affected Silicon Revisions

A1							
X							

5. Module: Master Synchronous Serial Port

In Master I^2C Receive mode, if a Stop condition occurs in the middle of an address or data reception, the SCL clock stream will continue endlessly and the RCEN bit of the SSPxCON2 register will remain set improperly. When a Start condition occurs after the improper Stop condition, nine additional clocks will be generated followed by the RCEN bit going low.

Work around

Use low-impedance pull-ups on the SDA line to reduce the possibility of noise glitches that may trigger an improper Stop event. Use a time-out event timer to detect the unexpected Stop condition, and subsequently, the stuck RCEN bit. Clear the stuck RCEN bit by clearing the SSPEN bit of SSPxCON1.

Affected Silicon Revisions

A1							
X							

6. Module: Master Synchronous Serial Port (MSSP)

When configured for I^2C™ slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer register (SSPxBUF) is not read after the SSP1IF interrupt (PIR1<3>) has occurred, but before the first rising clock edge of the next byte being received.

Work around

The issue can be resolved in either of these ways:

- Prior to the I^2C slave reception, enable the clock stretching feature. This is done by setting the SEN bit (SSPxCON2<0>).
- Each time the SSPxIF is set, read the SSPxBUF before the first rising clock edge of the next byte being received.

A1							
X							

7. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (SPEN bit (RCSTAx<7>) = 0)
- The EUSART is re-enabled (RCSTAx<7> = 1)
- A two-cycle instruction is executed immediately after setting SPEN, CREN or TXEN = 1

Work around

Add a 2 TCY delay after any instruction that re-enables the EUSART module (sets SPEN, CREN or TXEN = 1).

See Example 1.

Affected Silicon Revisions

A1							
X							

EXAMPLE 1: RE-ENABLING AN EUSART MODULE

```
;Initial conditions: SPEN = 0 (module disabled)
;To re-enable the module:
;Re-Initialize TXSTAx, BAUDCONx, SPBRGx, SPBRGHx registers (if needed)
;Re-Initialize RCSTAx register (if needed), but do not set SPEN = 1 yet

;Now enable the module, but add a 2-Tcy delay before executing any two-cycle
;instructions
bsf    RCSTA1, SPEN        ;or RCSTA2 if EUSART2
nop                        ;1 Tcy delay
nop                        ;1 Tcy delay (two total)
```

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39964**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Guidelines for Getting Started with PIC18FJ Microcontrollers

Section 2.4 "Voltage Regulator Pins (VCAP/VDDCORE)" has been replaced with a new and more detailed section. The entire text follows:

2.4 Voltage Regulator Pins (VCAP/VDDCORE)

On "F" devices, a low-ESR (< 5Ω) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specification can be used.

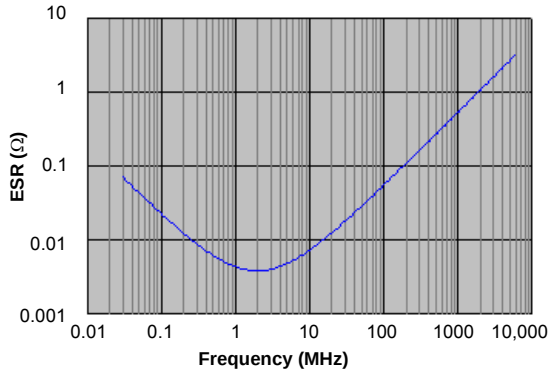
Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 31.0 "Electrical Characteristics"** for additional information.

On "LF" devices, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 31.0 "Electrical Characteristics"** for information on VDD and VDDCORE.

Note that the "LF" versions of these devices are provided with the voltage regulator permanently disabled; they must always be provided with a supply voltage on the VDDCORE pin.

FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at 25°C, 0V DC bias.

TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to 125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to 85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to 125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to 85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to 125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to 85ºC

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

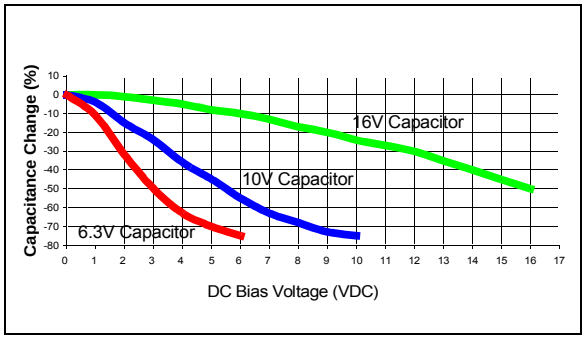
Typical low-cost, 10 µF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R), or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 µF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal voltage regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for 16V, 10V and 6.3V rated capacitors is shown in Figure 2-4.

FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V core voltage. Suggested capacitors are shown in Table 2-1.

2. Module: Reset

Table 5-2 incorrectly defines the SSP2STAT Reset state as '1111 1111'. The correct Reset state of the SSP2STAT is '0000 0000'.

This correction also applies to all other occurrences of this value throughout the device data sheet, including:

- Table 6-4: Register File Summary (PIC18F47J53)
- Register 20-1: SSPxSTAT: MSSPx Status Register (SPI Mode) (Access 1, FC7h; 2, F73h; 2 F73h)
- Register 20-5: SSPxSTAT: MSSPx Status Register (I^2C™ Mode) (1, Access FC7h; 2, F73h)

3. Module: Device Overview

Figures 1-1 and 1-2 incorrectly denote the program memory size as being 16 Kbytes to 64 Kbytes. The correct program memory size is 64 Kbytes to 128 Kbytes.

4. Module: Electrical Characteristics

The D060, D061 and D063 rows in **Section 31.3 DC Characteristics: PIC18F47J53 Family (Industrial)**, on page 527, have been pulled out of the table and placed into Table 31-1. The new table, with updated content, is shown below:

TABLE 31-1 DC CHARACTERISTICS:PIC18F47J53 FAMILY (INDUSTRIAL)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Symbol**	**Characteristic**	**Typ**	**Max**	**Units**	**Temp.**	**Conditions**
	IIL	**Input Leakage Current)(1,2)**					
D060		I/O Ports without 5.5V Tolerance	±5	±200	nA	±25ºC	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
			±15	±500	nA	+85ºC	
		I/O Ports with 5.5V Tolerance	±5	±200	nA	±25ºC	VSS ≤ VPIN ≤ 5.5V, Pin at high-impedance
			±15	±500	nA	+85ºC	
D061		$\overline{\text{MCLR}}$	±5	±200	nA	±25ºC	VSS ≤ VPIN ≤ VDD
			±15	±500	nA	+85ºC	
D062		D+/D-	±75	±500	nA	±25ºC	VSS ≤ VPIN ≤ VUSB
			±75	±500	nA	+85ºC	
D063		OSC1	±5	±200	nA	±25ºC	VSS ≤ VPIN ≤ VDD
			±15	±500	nA	+85ºC	

Note 1: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

5. Module: Electrical Characteristics

Table 31-7 has been corrected and changes are shown in bold below:

TABLE 31-7 USB MODULE SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	Sym	Characteristics	Min	Typ	Max	Units	Comments
D313	VUSB	USB Voltage	3.0	—	3.6	V	Voltage on VUSB pin must be in this range for proper USB operation
D314	IIL	Input Leakage on D+ or D-	—	**±.075**	**±0.5**	µA	VSS ≤ VPIN ≤ VUSB
D315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	For VUSB range
D316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	For VUSB range
D318	VDIFS	Differential Input Sensitivity	—	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
D319	VCM	Differential Common Mode Range	0.8	—	2.5	V	
D320	ZOUT	Driver Output Impedance(1)	28	—	44	Ω	
D321	VOL	Voltage Output Low	0.0	—	0.3	V	1.5 kΩ load connected to 3.6V
D322	VOH	Voltage Output High	2.8	—	3.6	V	1.5 kΩ load connected to ground

Note 1: The D+ and D- signal lines have built-in impedance matching resistors. No external resistors, capacitors or magnetic components are necessary on the D+/D- signal paths between the PIC18F47J53 family device and a USB cable.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2010)

Initial release of this document, issued for revision A1 silicon. Added silicon issues 1 (Charge Time Measurement Unit – CTMU), 2 (Phase Locked Loop – PLL), 3 (Analog-to-Digital Converter – ADC), 4 (EUSART – Receive Baud Rate), 5 (MSSP – I^2C Modes), 6 (I^2C Slave Reception) and 7 (EUSART – Enable/Disable). No data sheet clarifications.

Rev B Document 10/2010)

Added data sheet clarification issues 1 (Guidelines For Getting Started with PIC18FJ Microcontrollers), 2 (Reset) and 3 (Device Overview).

Rev C Document 12/2010)

Added data sheet clarification issues 4-5 (Electrical Characteristics).

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