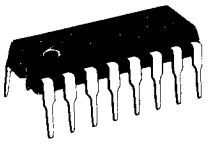
MN74HC175/MN74HC175S

Quad D-Type Flip-Flops with Clear

■ Description

MN74HC175/MN74HC175S contain four quad D-type flip-flop circuits with clear, and this circuit has common clock and clear, and complementary outputs Q and $\overline{Q}$. D-input data is transferred to outputs Q and $\overline{Q}$ at the rising edge of the clock pulse. The output from each flip-flop circuit is a reversed phase output of the other. All flip-flops are controlled by a common clock and clear; the clear function operates when the clear input is "L", and all Q and $\overline{Q}$ outputs become "L" and "H" respectively. Adoption of the silicon gate CMOS process makes possible low power consumption and a high noise allowance; LS TTL 10-inputs can be directly driven. Resistors and diodes are used in the V_{DD} and V_{SS} to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.

P-3



16-pin plastic DIL package

P-4

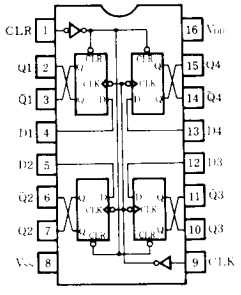
16-pin Panaflat package (SO-16D)

■ Truth table

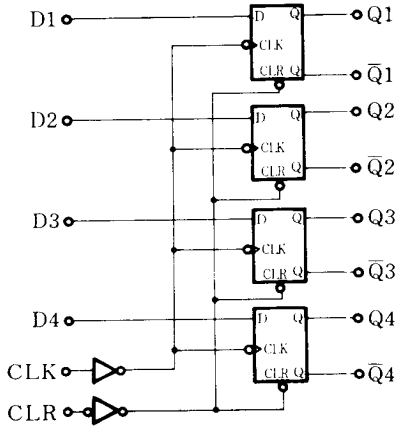
Input			Output	
CLR	CLK	D	Q	$\overline{Q}$
L	×	×	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	×	Q_0	$\overline{Q}_0$

Notes:
1. ↑: Data input is transferred to output when clock rises from LOW to HIGH
2. ×: Either HIGH or LOW; it doesn't matter
3. $Q_0(\overline{Q}_0)$: Q($\overline{Q}$) level prior to determination of input conditions shown in the tables

Pin configuration (top view)



■ Logic diagram



■ Absolute maximum ratings

Item			Sym.	Rating	Unit
Supply voltage			V_{DD}	−0.5～7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{DD}+0.5	V
Input current			I_I	±20	mA
Output current			I_O	±25	mA
Power dissipation	MN74HC175	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/℃	
	MN74HC175S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/℃	
Storage temperature range			T_{stg}	−65～+150	℃
Supply current			I_{DD}, I_{SS}	±50	mA

■ Recommended operating conditions

Item	Sym.	Rating	Unit
Operating supply voltage	V_{DD}	1.4～6.0	V
Input voltage	V_I	0～V_{DD}	V
Operating temperature range	T_{opr}	−40～+85	℃
Input rise and fall time	t_r, t_f	0～500	ns

■ DC characteristics (V_{DD}=5V±10%, V_{SS}=0V)

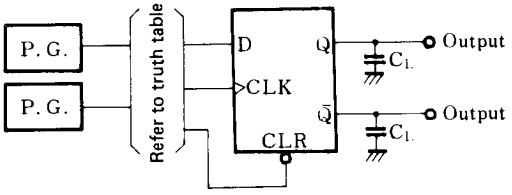
Item	Sym.	Test conditions		Ta=−40℃ Min.	Ta=−40℃ Max.	Ta=+25℃ Min.	Ta=+25℃ Max.	Ta=+85℃ Min.	Ta=+85℃ Max.	Unit
Quiescent supply current	I_{DD}	V_I=V_{DD} or V_{SS}			8		8		80	μA
High level input voltage	V_{IH}	V_O=V_{DD}−1.0V or 0.5V, $\|I_O\|$≦1μA	V_{DD}=4.5V	3.15		3.15		3.15		V
			V_{DD}=5.0V	3.50		3.50		3.50		
			V_{DD}=5.5V	3.85		3.85		3.85		
Low level input voltage	V_{IL}	V_O=V_{DD}−1.0V or 0.5V, $\|I_O\|$≦1μA	V_{DD}=4.5V		0.9		0.9		0.9	V
			V_{DD}=5.0V		1.0		1.0		1.0	
			V_{DD}=5.5V		1.1		1.1		1.1	
Input current	±I_I	V_I=V_{DD} or V_{SS}			0.3		0.3		1	μA
High level output voltage	V_{OH}	V_I=V_{DD} or V_{SS}, $\|I_O\|$≦1μA		V_{DD}−0.05		V_{DD}−0.05		V_{DD}−0.05		V
Low level output voltage	V_{OL}	V_I=V_{DD} or V_{SS}, $\|I_O\|$≦1μA			0.05		0.05		0.05	V
High level output current	I_{OH}	V_I=V_{DD} or V_{SS}, V_O=V_{DD}−0.8V		−6		−5		−4		mA
Low level output current	I_{OL}	V_I=V_{DD} or V_{SS}, V_O=0.4V		6		5		4		mA

■ AC characteristics (V_{DD}=5V, V_{SS}=0V, Ta=25℃, Input transition time ≦6ns, C_L=50pF)

Item	Sym.	Test conditions	Min.	Typ.	Max.	Unit
Output rise time	t_{TLH}			8	15	ns
Output fall time	t_{THL}			6	15	ns
Minimum data set-up time	t_{su}				20	ns
Maximum clock frequency	f_{max}		30			MHz
Propagation time (L→H) CLK→Q,$\bar{Q}$	t_{PLH}				25	ns
Propagation time (H→L) CLK→Q,$\bar{Q}$	t_{PHL}				25	ns
Propagation time (L→H) PR,CLR→Q,$\bar{Q}$	t_{PLH}				25	ns
Propagation time (H→L) PR,CLR→Q,$\bar{Q}$	t_{PHL}				25	ns
Minimum clear pulse width	t_{WCD}				25	ns

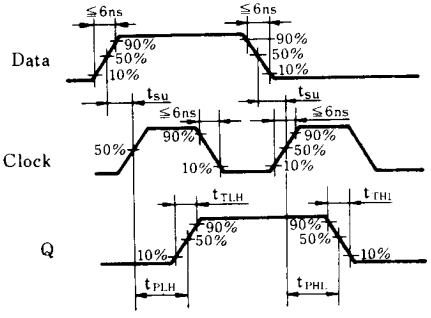
※ Switching time measurement circuit and waveform

1. Measurement circuit



2. Waveforms

Waveforms–1 (t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL}(CLK→Q, $\bar{Q}$))



Waveforms–2 (t_{PLH}/t_{PHL}(CLR→Q, $\bar{Q}$), t_{WCD})