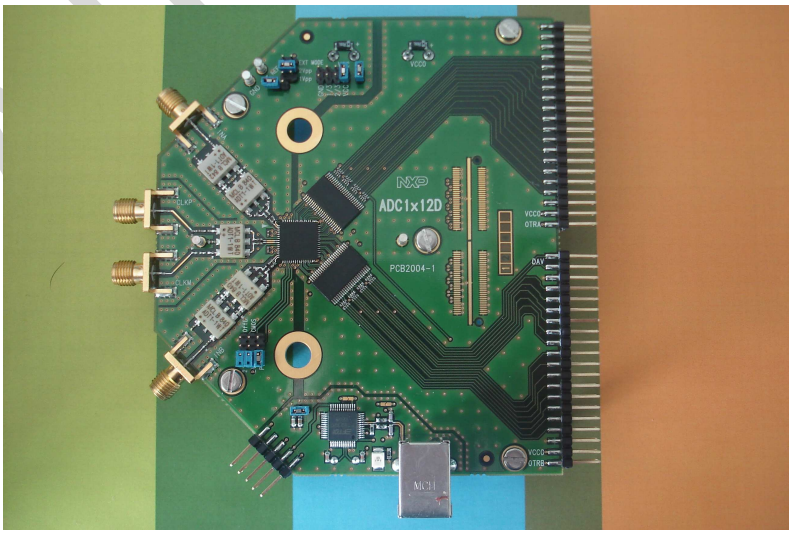
Quick start ADC1412D, ADC1212D, ADC1112D series

Demonstration board for ADC1412D, ADC1212D, ADC1112D series

Rev. 10 — 17 December 2010 **Quick start**

Document information

Info	Content
Keywords	PCB2004-1, Demonstration board, ADC, Converter, ADC1412D, ADC1212D and ADC1112D series.
Abstract	This document describes how to use the demonstration board for the analog-to-digital converter ADC1412D, ADC1212D and ADC1112D series.
Overview	

Revision history

Rev	Date	Description
1	20081001	Initial version.
2	20090518	Update to PCB2004-1.2.
3	20090610	Add SPI software description.
4	20100518	Update to latest release of SPI software. Add HSDC extension module acquisition system description.
5	20100601	Correction added.
6	20100730	Update for LVDS acquisition mode.
7	20100806	Update to latest acquisition software tool.
8	20100820	Update for web release.
9	20100924	Update with latest board reference.
10	20101217	Update with latest software tool.

1. Overview of the ADC1412D, ADC1212D, ADC1112D demo board

1.1 ADC1412D series

Figure 1 presents the connections to measure the ADC1412D series:

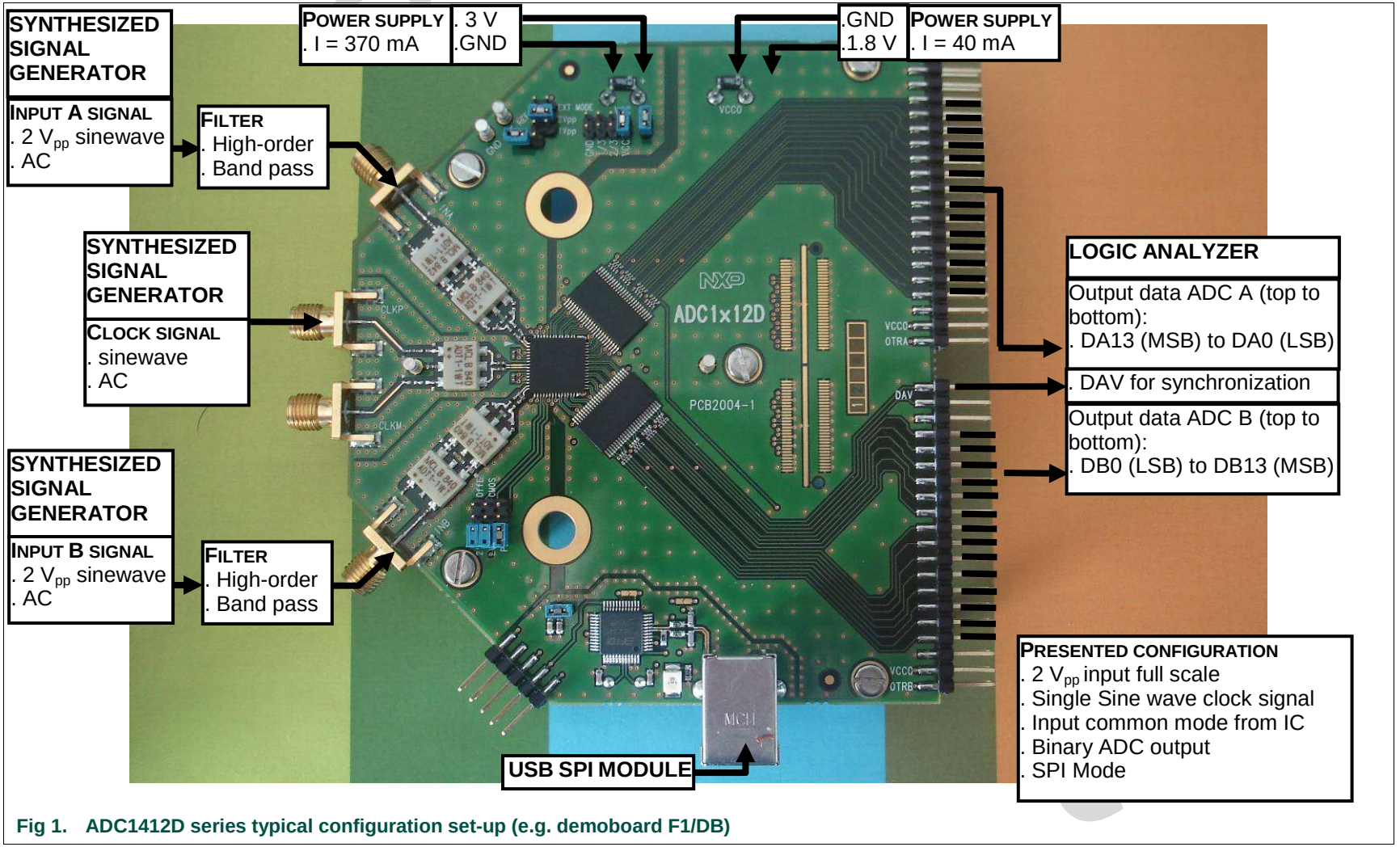


Fig 1. ADC1412D series typical configuration set-up (e.g. demoboard F1/DB)

1.2 ADC1212D series

Figure 2 presents the connections to measure the ADC1212D series:

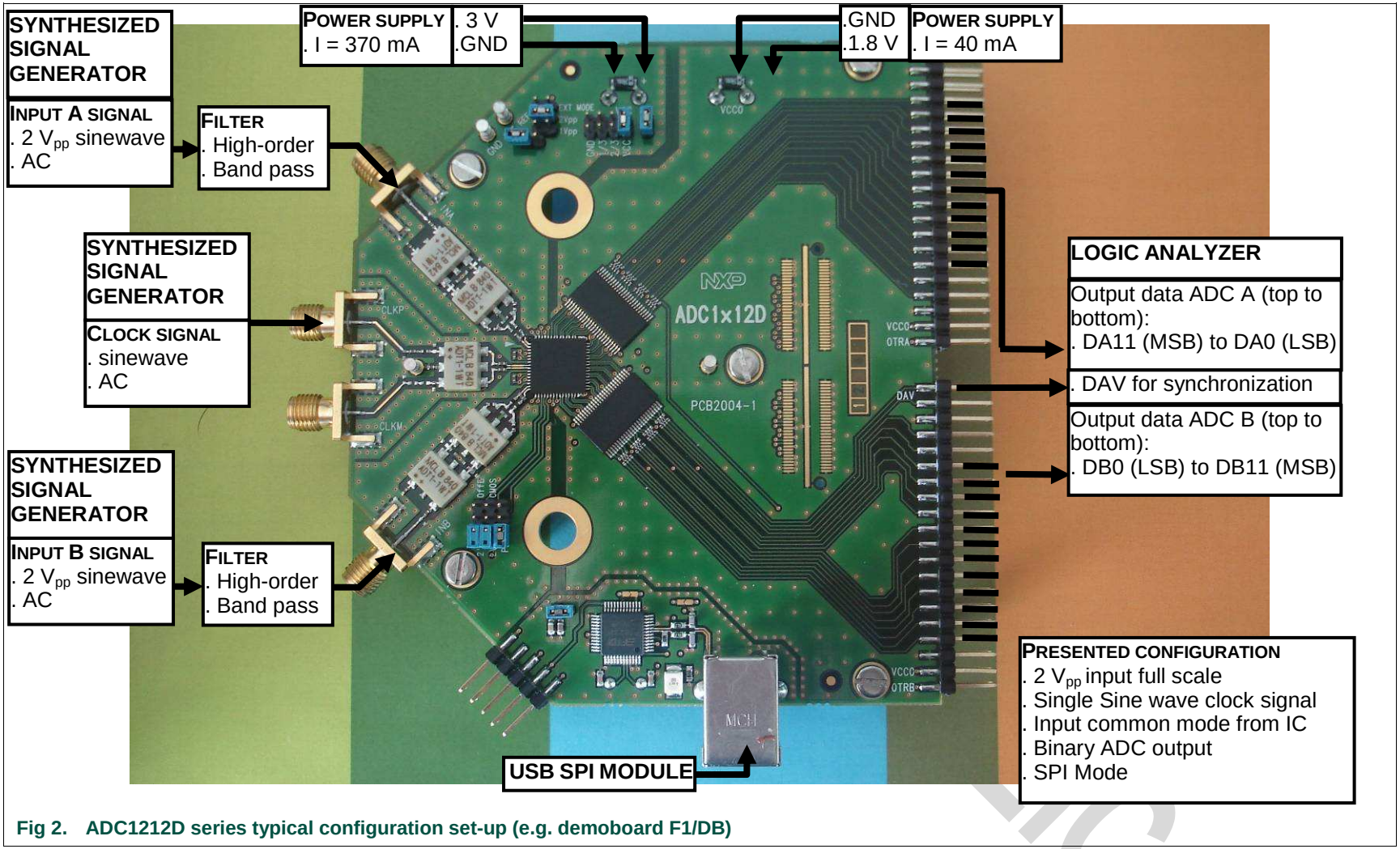


Fig 2. ADC1212D series typical configuration set-up (e.g. demoboard F1/DB)

1.3 ADC1112D series

Figure 3 presents the connections to measure the ADC1112D series:

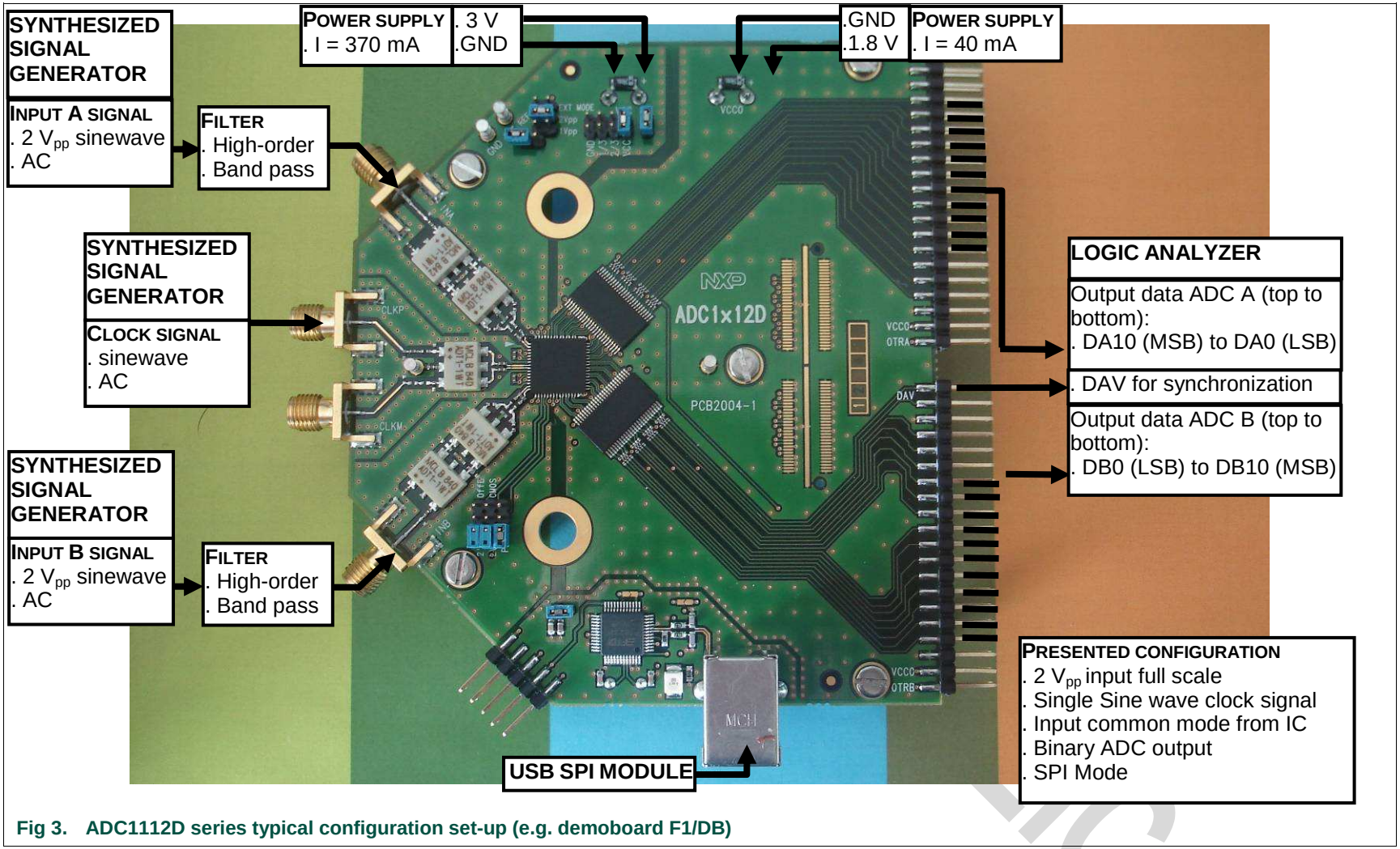
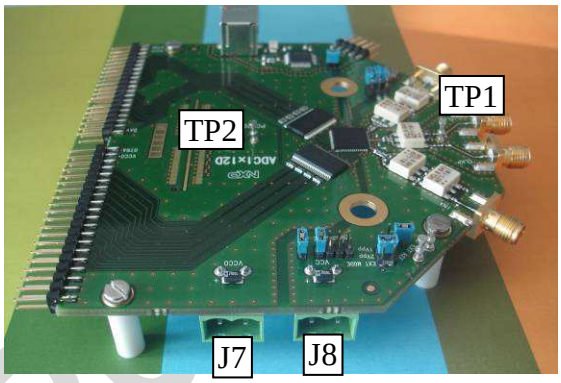


Fig 3. ADC1112D series typical configuration set-up (e.g. demoboard F1/DB)

1.4 Power supply

The board is powered with a 3 V_{DC} and 1.8/3 V_{DC} power supplies. A power supply regulator is used to supply all the circuitry on the board.

Table 1. General power supply

Name	Function	View
J8	+3 V green connector – Power supply 3 V_{DC} / 400 mA.	
J7	+1.8 V green connector – Power supply 1.8 V_{DC} / 100 mA	
TP1	AGND test point – Digital ground	
TP2	DGND test point – Analog ground	

1.5 Input signals (IN, CLK)

The input clock signal can be either a sinewave or a LVCMOS signal.

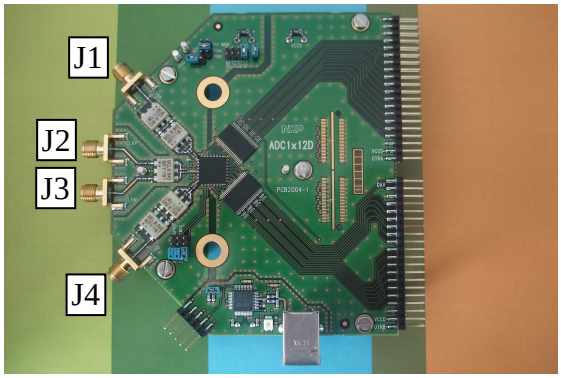
To ensure a good evaluation of the device, the input signal and the input clock must be synchronized together.

Moreover, the input frequency (Fi, MHz) and the clock frequency (Fclk, Msps) should follow the formula, known as coherency criteria for FFT processing (see section 3.3.6 and appendix A.1):

$$\frac{F_{in}}{F_s} = \frac{M}{N}$$

where M is an odd number of period and N is the number of samples.

Table 2. Input signals

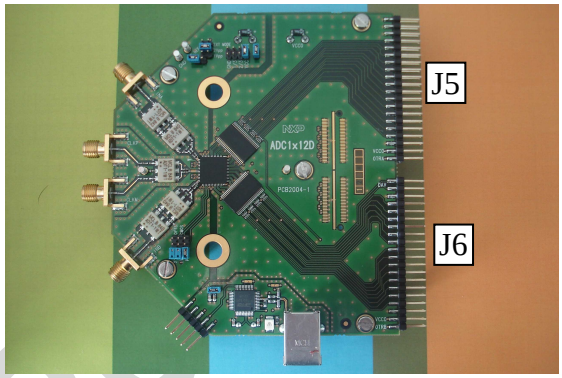
Name	Function	View
J1	IN A connector – Analog input signal (50 Ω matching)	
J2	CLKP connector – Single ended clock input signal (50 Ω matching), with a transformer.	
J3	CLKN connector – Grounded on that demoboard	
J4	IN B connector – Analog input signal (50 Ω matching)	

1.6 Output signals (DA0 to DA13, DB0 to DB13, OTRA, DAV)

The digital output signal is available in binary, 2's complement or gray format.

A Data Valid Output clock (DAV) is provided by the device for the data acquisition.

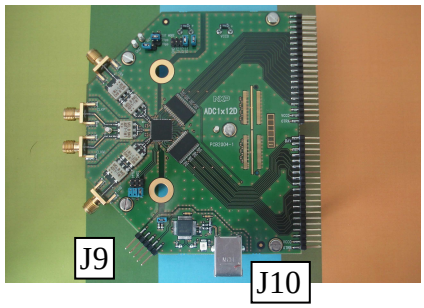
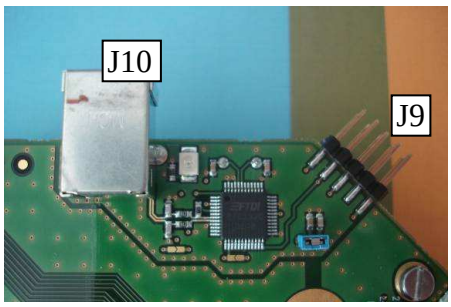
Table 3. Output signals

Name	Function	View
J5	Array connector – ADC A digital output(DA0 to DA13), Out of range signal (OTRA)	
J6	Array connector – ADC B digital output(DB0 to DB13) and Data Valid (DAV)	

1.7 SPI Mode

The ADC1412D can be controlled either by a Serial Peripheral Interface (SPI) or by PIN.

Table 4. SPI Interface

Name	Function	View
J9	Array connector – SPI daughter board interface (for debug only)	
J10	USB connector – SPI daughter board interface	

1.8 SPI program

For more details on how to control device with SPI, refer to section 3.3.

2. HSDC extension module: acquisition board

The figure 4 shows an overview of the extension module HSDC-EXTMOD01/DB acquisition board:

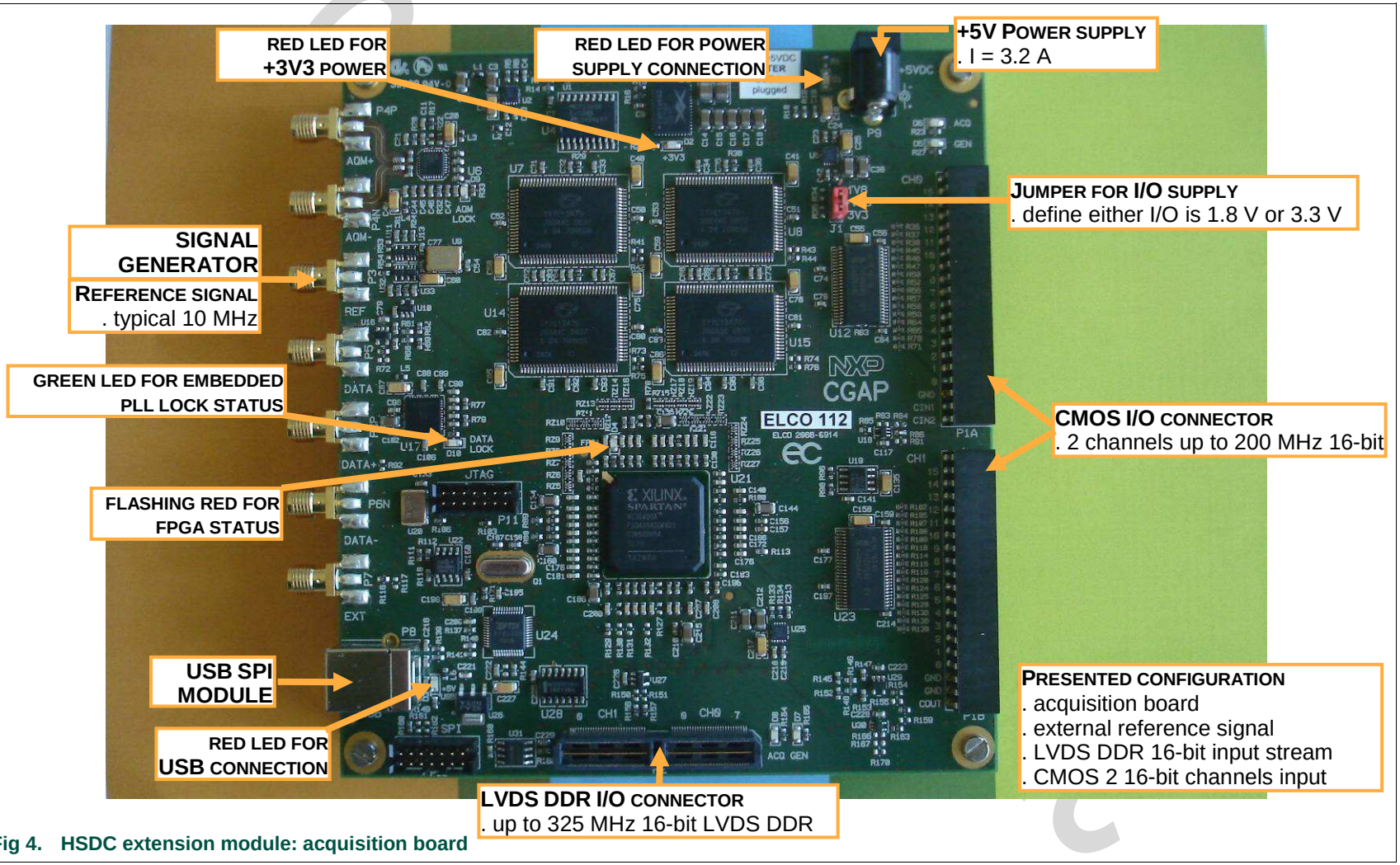


Fig 4. HSDC extension module: acquisition board

The HSDC extension module is intended for acquisition/generation and clock generation purpose. When connected to an ADC demo-board it is intended as an acquisition system for digital output bits delivered by ADC, either CMOS (HE14 P1 connector) or LVDS DDR (SAMTEC QTH_060_02 P2 connector).

The board brief specification is shown below:

- 32 MB memory size for acquisition pattern;
- 2 16-bit channels CMOS up to 200 MHz;
- 16-bit LVDS DDR input data stream up to 320 MHz;
- On-board or external reference for signal generation.

In this section the specific requirement for the use with ADC1412D demo-board will be shown.

For more details on the HSDC-EXTMOD01/DB, please contact dataconverter-support@nxp.com.

2.1 HSDC extension module: hardware initialization

Before using the generation board, make sure that you connect the USB cable **prior to** the supply.

When USB and power cable are connected, the HSDC-EXTMOD will light 3 red LEDs.

The green LED close to the PLL is only when it is locked (see section 3.3).

The red LED close to FPGA reports normal behavior when flashing ¼ on, ¾ off. Any other flashing behavior reports a failure at initialization (see section 3.3).

2.2 HSDC extension module: CMOS connector description

The figure 5 shows a brief description of the hardware connection on the HE14 connector.

For proper use of the acquisition board, make sure that resistor R86 (0 Ω) is connected while R84 is removed.

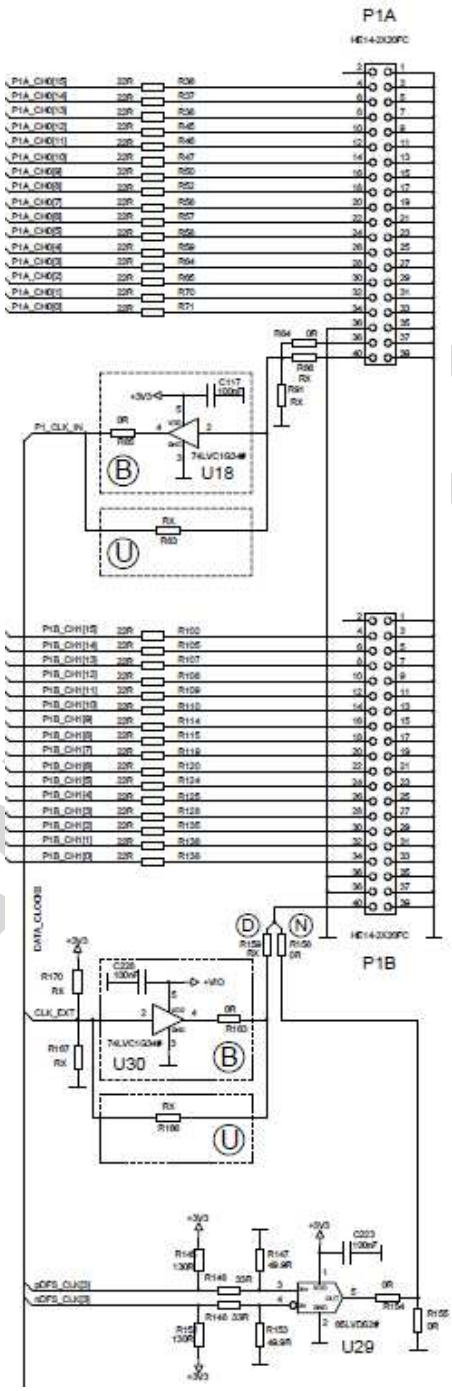


Fig 5. HSDC extension module: HE14 CMOS hardware schematic overview

3. Combo ADC1412D and HSDC extension module

3.1 ADC1412D CMOS outputs (demoboard F1/DB)

The figure 6 below shows an overview of the whole system ADC1412D+HSDC extension module with CMOS outputs configuration (e.g. ADC1412D125F1/DB) for which connection is straightforward, together with a supply extension module (HSDC-ACC09/DB release A) for the ADC1412D demo-board:

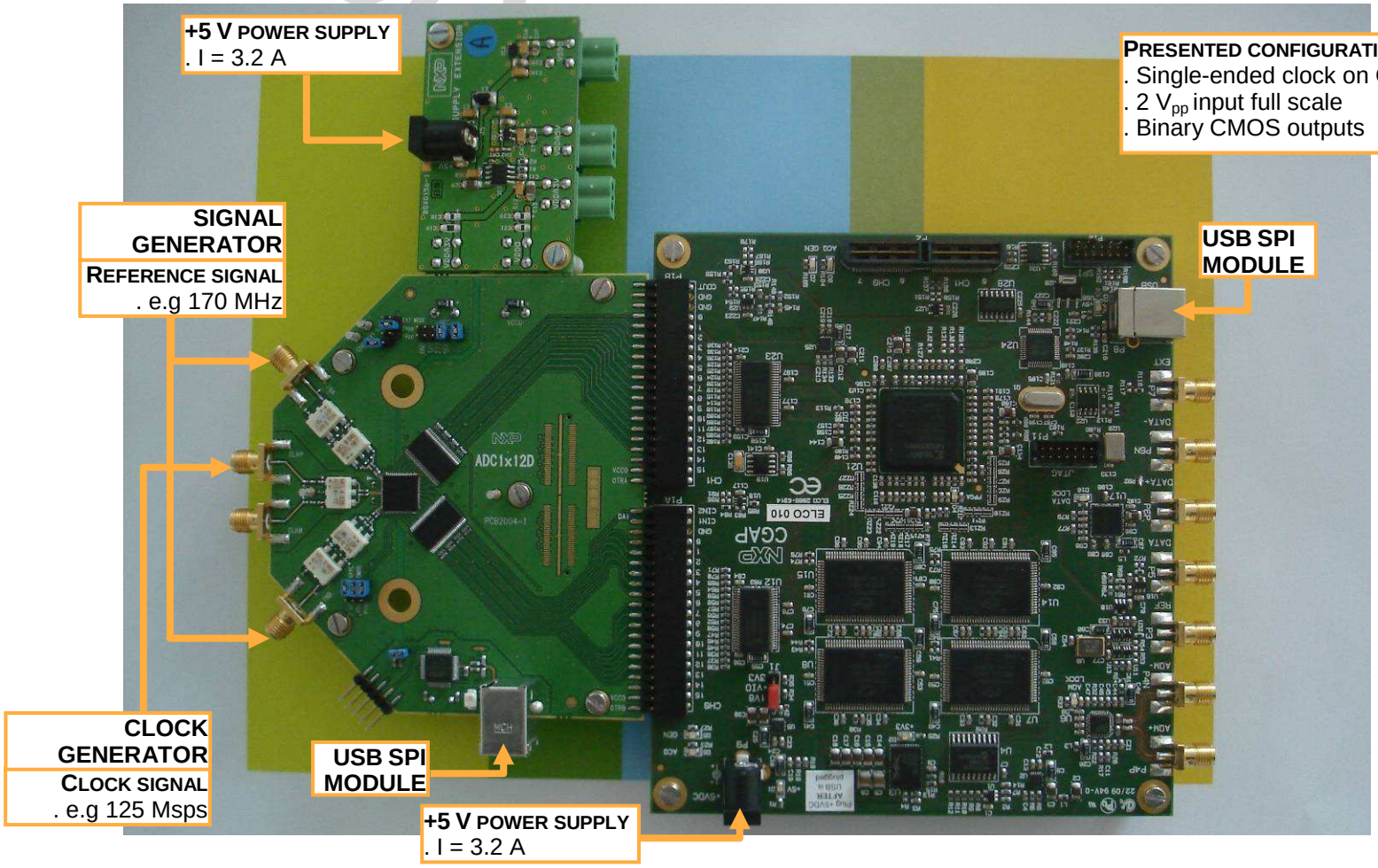


Fig 6. Evaluation set-up measurement with ADC1412D125F1/DB and HSDC-EXTMOD01/DB

3.2 ADC1412D LVDS outputs (demoboard F2/DB)

The figure 7 below shows an overview of the whole system ADC1412D+HSDC extension module with LVDS outputs configuration (e.g. ADC1412D125F1/DB) for which connection is done with a bridge SAMTEC (HSDC-ACC05/DB), together with a supply extension module (HSDC-ACC09/DB release B) for the ADC1412D demo-board:

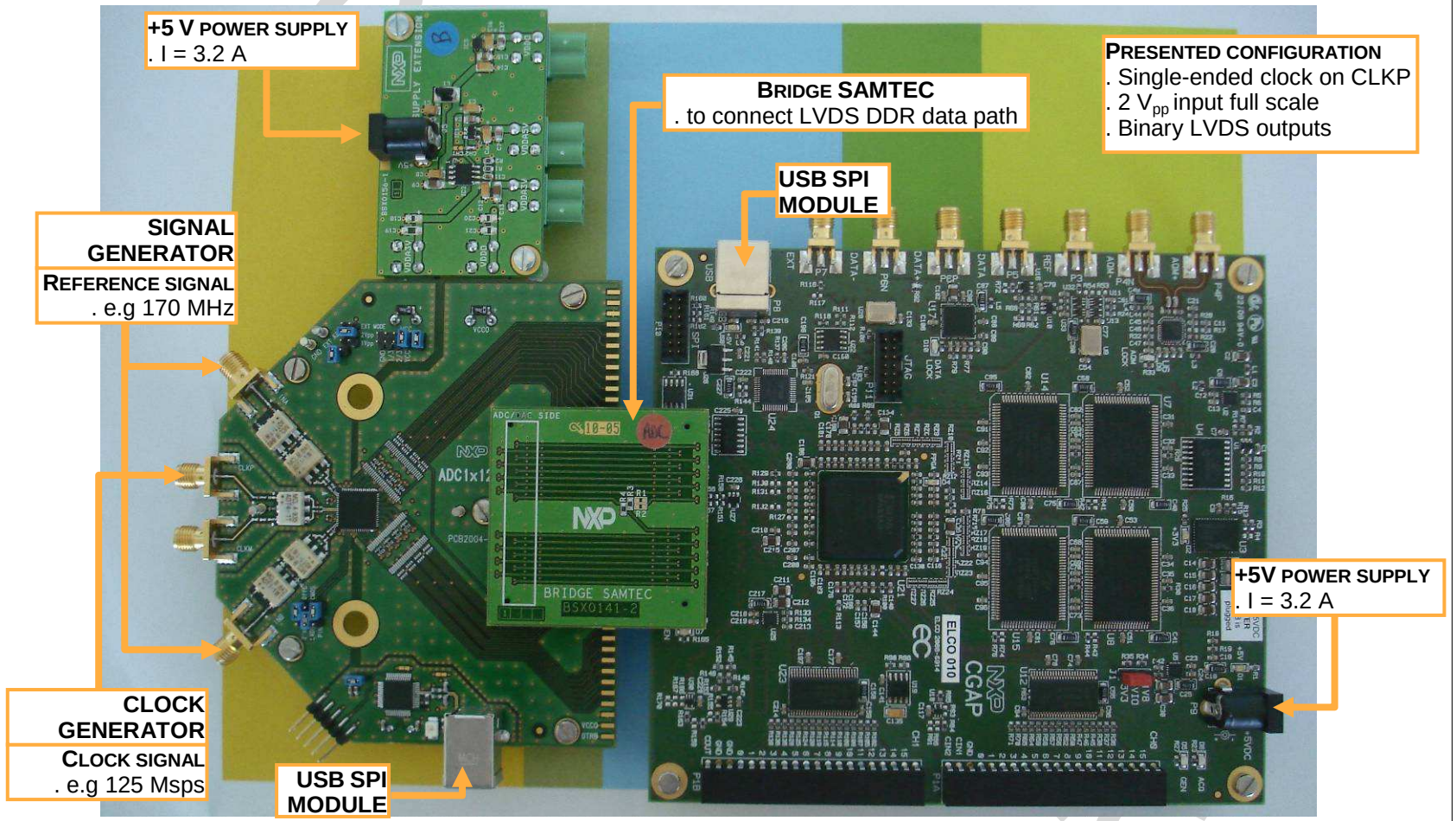


Fig 7. Evaluation set-up measurement with ADC1412D125F2/DB and HSDC-EXTMOD01/DB

Note 1: make sure that supply extension release B is used: it delivers the 3 V supply for LVDS output path for the ADC.

Note 2: make sure that LVDS connection is done as shown.

3.3 ADC Software tool

Run the application “SW_ADC_1_r02.exe”. This application will allow:

- the user to control features on our high speed ADC through the SPI interface available on any ADC1412D, ADC1212D and ADC1112D series;
- as well as performing any online data acquisition to evaluate the performances of the ADC1412D, ADC1212D and ADC1112D series.

At start-up, the program will detect any board connected to your system and display information as can be seen on following window:

Fig 8. SW_ADC_1_r02: start-up screen

①: “NXP Banner Button” will display your default internet browser to the NXP data converter home page;

②: “REFRESH” allows you to poll your system for any hardware change. It will reset any board connected to your system;

③: “QUIT” allows you quit the application;

④: “INITIALIZATION” allows you to initialize the HSDC-EXTMOD board prior to any acquisition task.

In the example above, the HSDC-EXTMOD has been detected, as well as ADC1412D080.

At this moment, make sure that 4 LEDs are visible on the HSDC-EXTMOD (2 close to power plug, 1 for USB and 1 close to FPGA).

The “Info” page gives more details on the current hardware configuration for the HSDC-EXTMOD board:

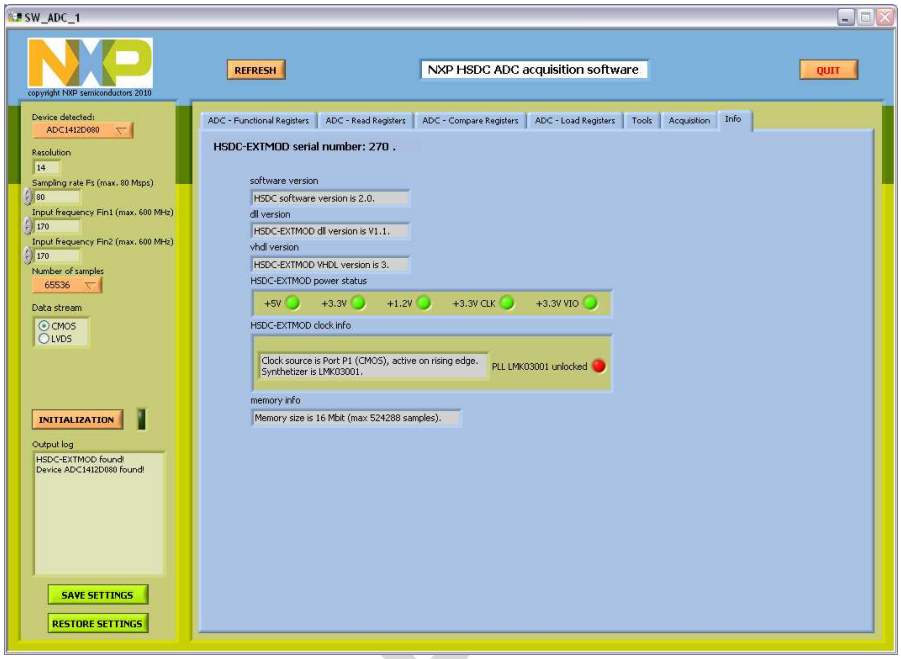


Fig 9. SW_ADC_1_r02: “Info” page

The HSDC-EXTMOD is not yet initialized, so the embedded PLL (LMK03001 in this example) is not locked. Initialization is only required for acquisition purpose.

3.3.1 ADC SPI programming Functional Registers page

The page displays all SPI registers for ADC1412D, ADC1212D and ADC1112D series:

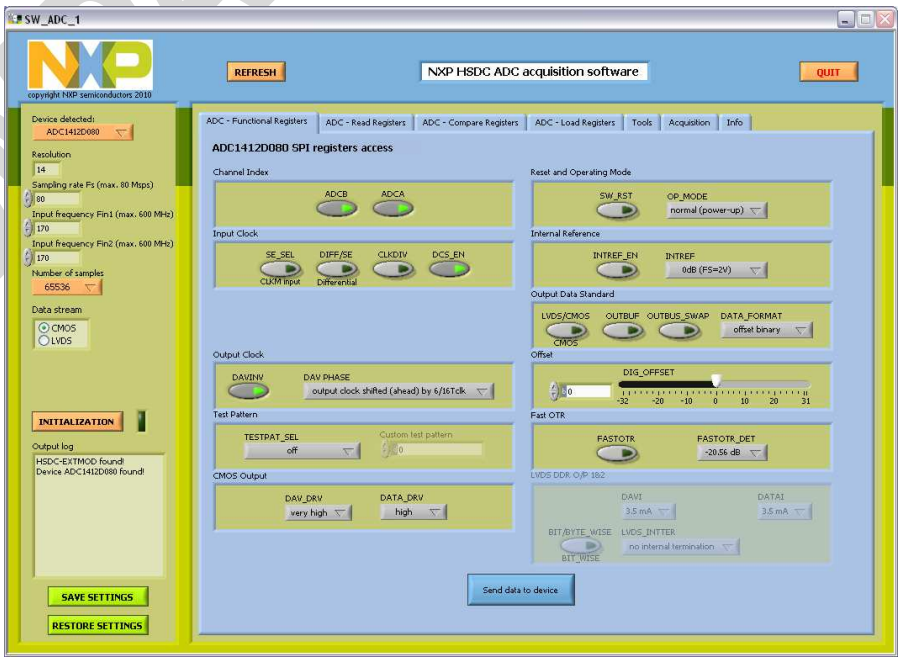


Fig 10. SW_ADC_1_r02: “ADC - Functional Registers” page

Perform any settings and then click on the “Send data to device” button to update the device registers.

3.3.2 ADC SPI programming Read Registers page

This page can be used to read all registers by clicking on the “Read all registers” button and will display the result in the table below:

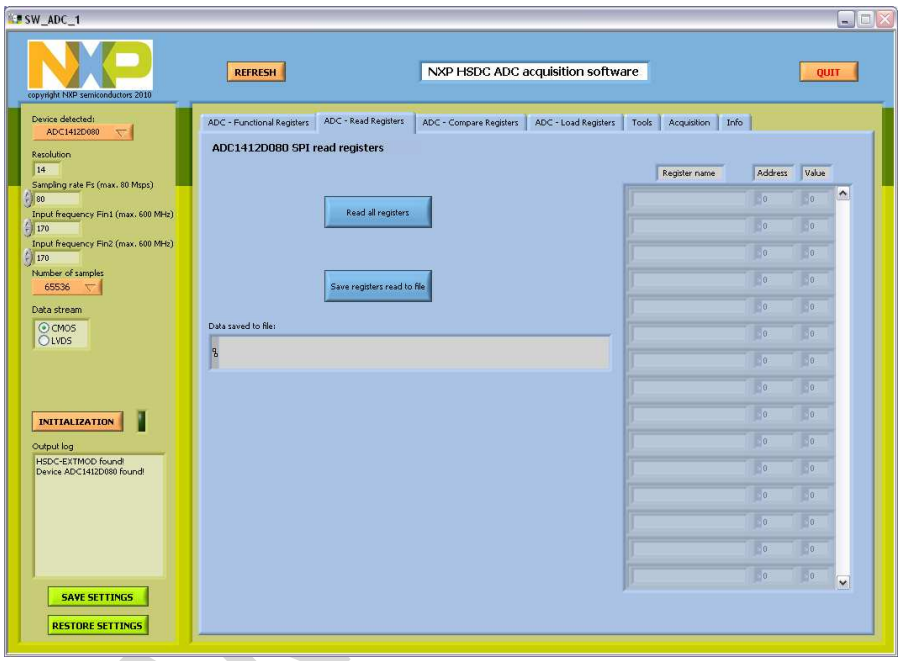


Fig 11. SW_ADC_1_r02: “ADC - Read Registers” page

When all registers have been read, it is possible to save the data to a text file. The settings are saved in a table-like format as shown below:

Table 5. Typical saving on text file

Content of file is shown as table format

Column 1	Column 2
Address	Value
3	ff
5	00
6	01
8	00
11	00
12	08
13	00
14	00

Column 1	Column 2
15	00
16	00
17	00
20	0e
21	00
22	00

Note that all data are saved in hexadecimal format.

Click on the “Save registers read to file” button to select the file to store data to. Make sure that you store your file with “.txt” extension, this will allow you to re-use the file on the “ADC - Load Registers” page.

3.3.3 ADC SPI programming Compare Registers page

This page can be used to compare the registers value from the 2 channels:

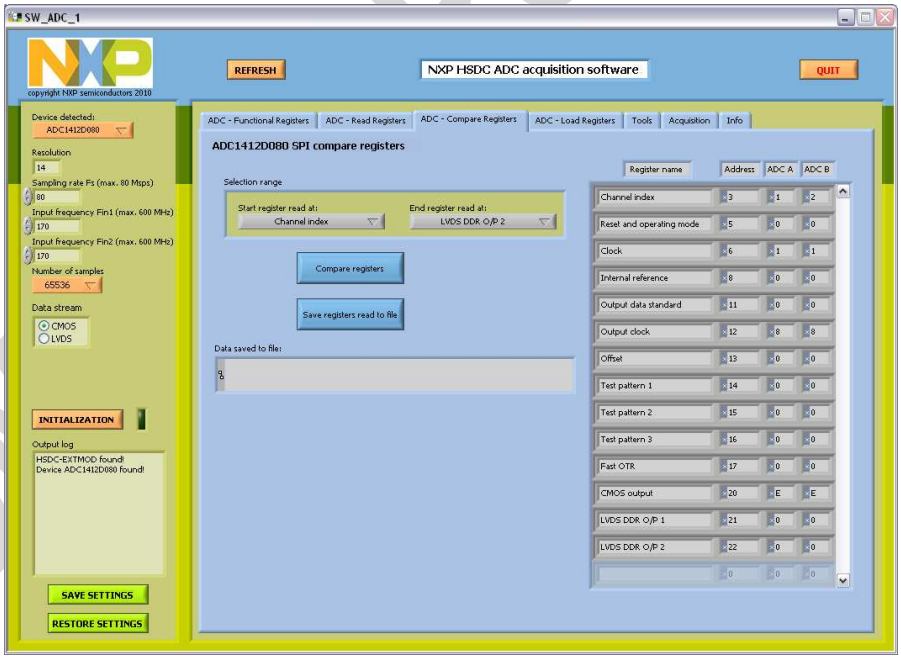


Fig 12. SW_ADC_1_r02: “ADC - Read Registers” page

To do the comparison, follow the procedure below:

- Select the first and last register to be compared in the “Selection range” field;
- Click on “Compare registers” button, this will show the values of all registers in the field of comparison for both ADC A and B.

Click on the “Save registers read to file” button to save the result of the comparison. The format of the text file is equivalent to the previous section and is given below:

Table 6. Typical saving for comparison on text file
Content of file is shown as table format

Column 1	Column 2	Column 3	Column 4
Register Name	Address	ADC A	ADC B
Channel index	3	1	2
Reset and operating mode	5	0	0
Clock	6	1	1
Internal reference	8	0	0
Output data standard	11	0	0
Output clock	12	8	8
Offset	13	0	0
Test pattern 1	14	0	0
Test pattern 2	15	0	0
Test pattern 3	16	0	0
Fast OTR	17	0	0
CMOS output	20	E	E
LVDS DDR O/P 1	21	0	0
LVDS DDR O/P 2	22	0	0

Note that all data are saved in hexadecimal format.

3.3.4 ADC SPI programming Load Registers page

This page allows downloading configuration data to the device registers:

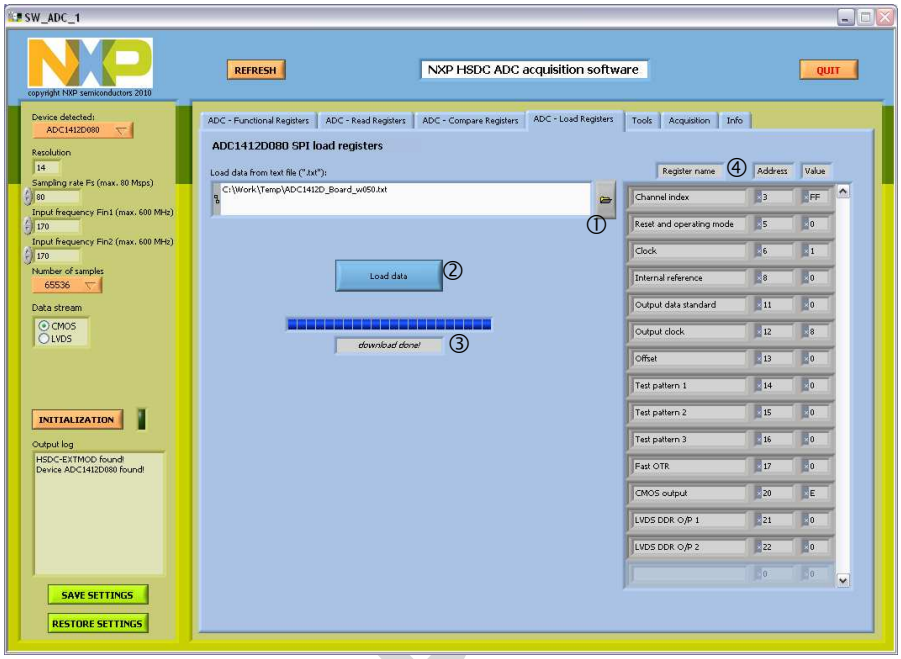


Fig 13. SW_ADC_1_r02: "ADC - Load Registers" page

It is not necessary to have a file that has the whole set of registers listed. The only restriction is regarding the formatting of the file as given in section 3.3.2.

Note: this page can not be used to download data saved during the comparison process.

To download settings onto device registers, follow the procedure below:

- Browse to select your file (button ①);
- Click on "Load data" button ②.

A message on field ③ and a progress bar will inform about the status of the operation until message "download done!" is seen. The table ④ is updated with the current values downloaded at the fly as can be seen on figure 13.

3.3.5 Tools page

This page allows the user to calculate the coherent frequencies values involved of the acquisition process. It gives an indication where the 6 first harmonics are located in the Nyquist zone.

Enter your analog and sampling frequencies in field ①**.** Indicate the number of samples to be acquired ②, as well as the fixed parameter for the coherency calculation (Fs in our example above ③). Press "UPDATE GRAPH" to look at the frequency plan, it gives also the real Fin frequency (Refer to appendix A.1 for more details on coherency calculation):

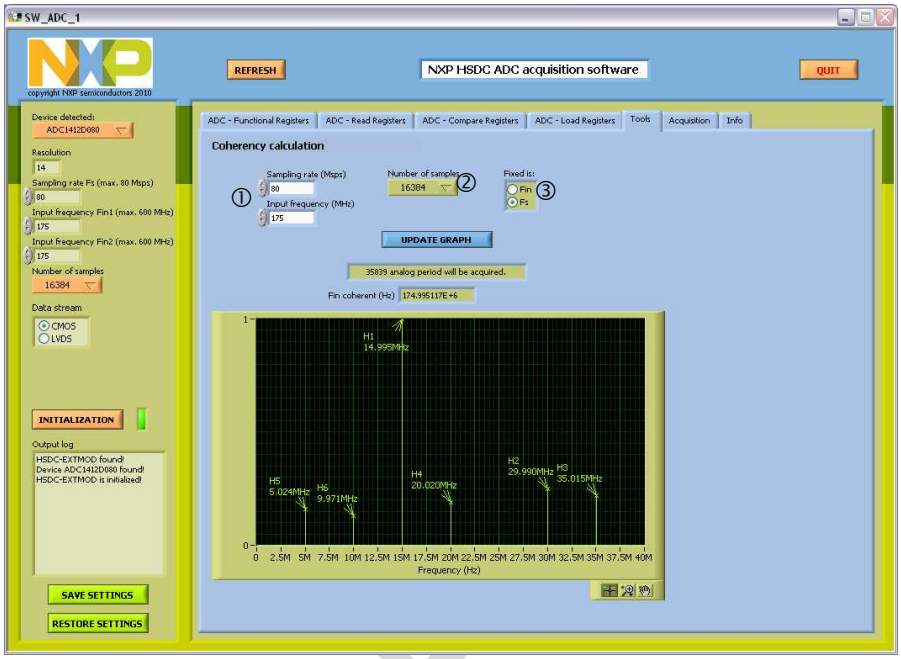


Fig 14. SW_ADC_1_r02: “Tools” page

Note: The level of the harmonics shown does not reproduce the behavior of the ADC; they are only given as indication for location.

3.3.6 Acquisition page

This page will acquire data to evaluate the high dynamic performance of the device:

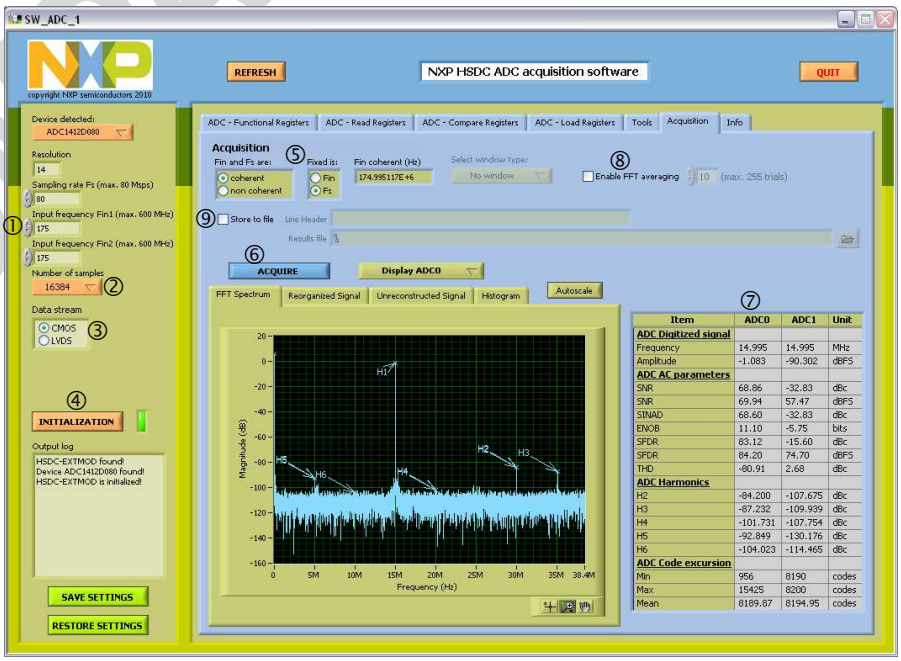


Fig 15. SW_ADC_1_r02: “Acquisition” page

Before proceeding to any acquisition, the user needs to do the following entries:

- the sampling frequency Fs: 80 Msps in our example (field ①);
- the input frequency Fin: 175 MHz in our example for both ADC channels (field ①);
- the number of samples to be acquired 16384 in our example (field ②);
- indicate whether it is CMOS or LVDS DDR (field ③);
- press the “INITIALIZATION” button ④. It will initialized the HSDC-EXTMOD board:
  - FPGA is ready (red LED is flashing ¼ on and ¾ off) ;
  - PLL embedded is locked (green LED is on);
- indicate whether Fin or Fs are coherent or not (field ⑤):
  - if signals are coherent, selected which Fin or Fs are fixed for the calculation (see appendix A.1);
  - if signals are not coherent, select the window for FFT processing to apply (the Blackman window gives better results).
- press the “ACQUIRE” button ⑥ to display the results from the FFT processing. The results fields ⑦ will be updated automatically depending on the display choice using the “Display …” button (“Display ADC0” or “Display ADC1” or “Display ADC0 & ADC1”).
- press “STOP” button to stop acquisition;
- field ⑧ allows to do FFT averaging over up to 255 trials, suitable for small signal analysis;
- field ⑨ allows to store dynamic results to text file. Click on the check box, enter a header as a comment and browse to indicate where to store data file. Table 7 shows how data are stored:

Table 7. Dynamic results as stored in a text file

Content of file is shown as table format

Name	Fin	Fs	Vin	ENOB	SINAD	SNR_C	SNR_FS	SFDR_C	SFDR_FS	THD	H2	H3	H4	H5	H6
	(MHz)	(MHz)	(dBFS)	-	(dBc)	(dBc)	(dBFS)	(dBc)	(dBFS)	(dBc)	(dBc)	(dBc)	(dBc)	(dBc)	(dBc)
ADC1412D080 test															
ADC0	175.00	80.00	-1.08	11.10	68.84	68.56	69.93	83.04	84.12	-80.59	-84.17	-86.48	-106.34	-92.16	-100.45
ADC1	175.00	80.00	-86.74	-5.89	-33.71	-33.71	53.04	-19.91	66.84	4.77	-103.19	-119.04	-111.66	-110.96	-120.78

Note that ADC0 and ADC1 refer to the acquisition path on the HSDC-EXTMOD board. It corresponds respectively to the bottom and top ADC of the ADC1412D, ADC1212D and ADC1112D series.

Note that while acquisition is running, any other action (ADC SPI programming, quit or refresh) is not possible. Stop acquisition first before proceeding to any other task.

3.3.6.1 FFT spectrum

The first graph to be displayed is the FFT spectrum of the digital pattern acquired:

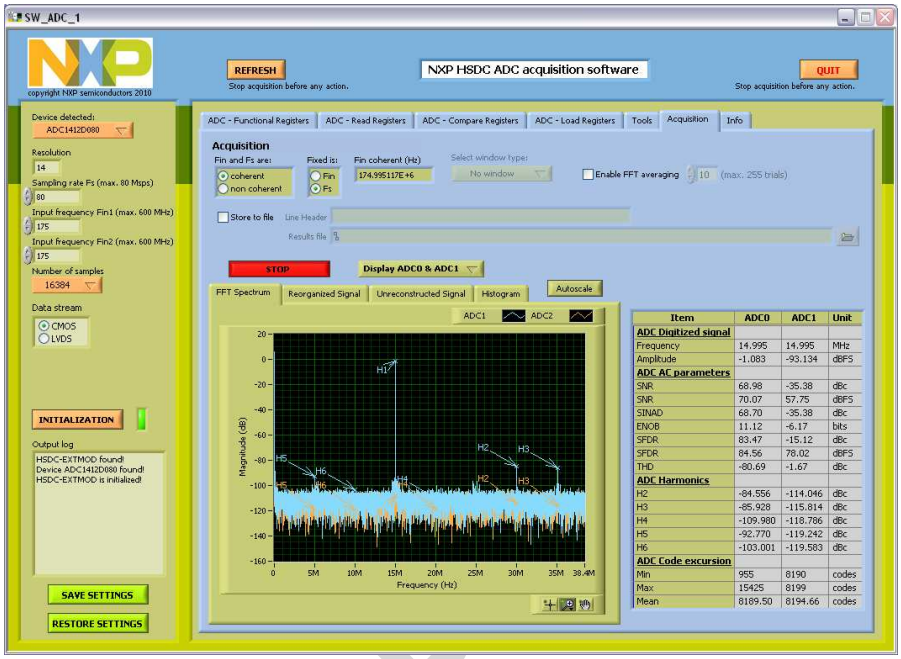


Fig 16. SW_ADC_1_r02: “Acquisition” page, FFT graph

Press the “Autoscale” button to display the whole content.

3.3.6.2 Reorganized signal

The reorganized signal displays the reconstructed sine wave from coherency calculation corresponding to 1 period of the input signal:

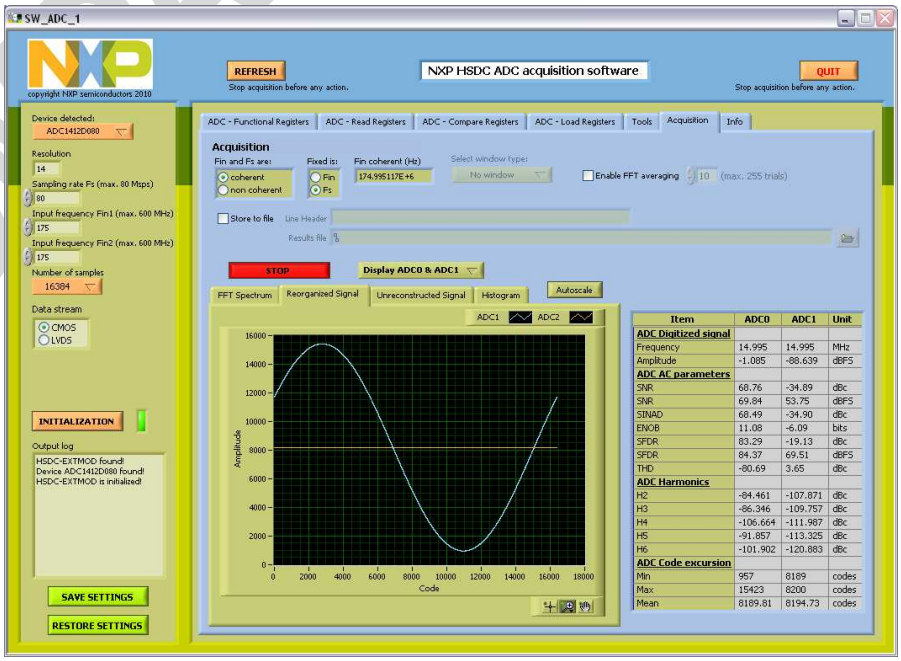


Fig 17. SW_ADC_1_r02: “Acquisition” page, reorganized signal graph

Press the “Autoscale” button to display the whole content.

3.3.6.3 Unreconstruted signal

The unreconstructed signal displays the unreconstructed sine wave corresponding to the whole number of period being acquired following the coherency rule:

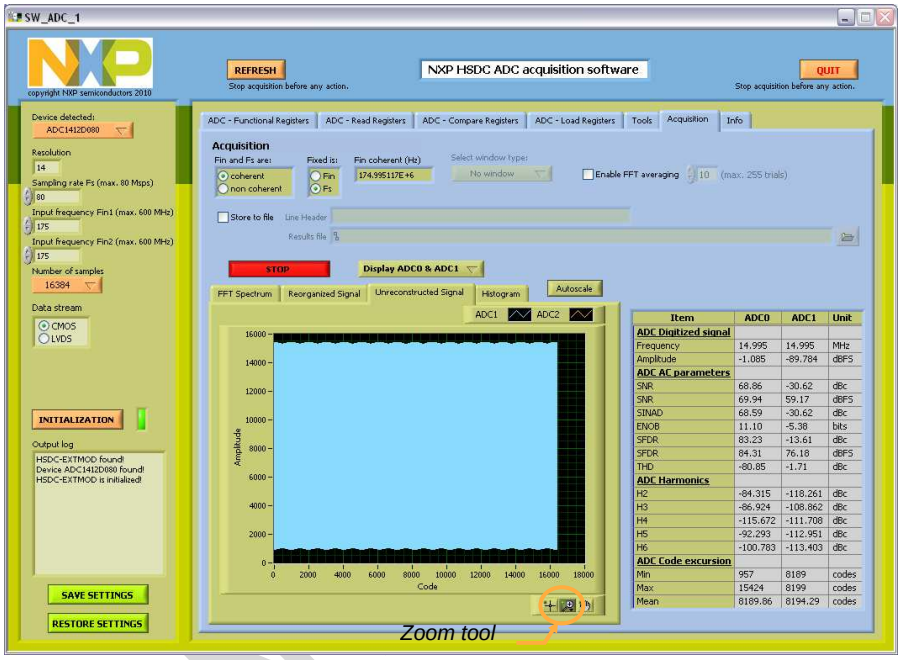


Fig 18. SW_ADC_1_r02: “Acquisition” page, unreconstructed signal graph

Press the “Autoscale” button to display the whole content.

Use the zoom tool to observe in more details all the captured data.

3.3.6.4 Histogram

The histogram graph shows the distribution of output codes. This graph shows which code is present and if there is any missing code in the conversion range:

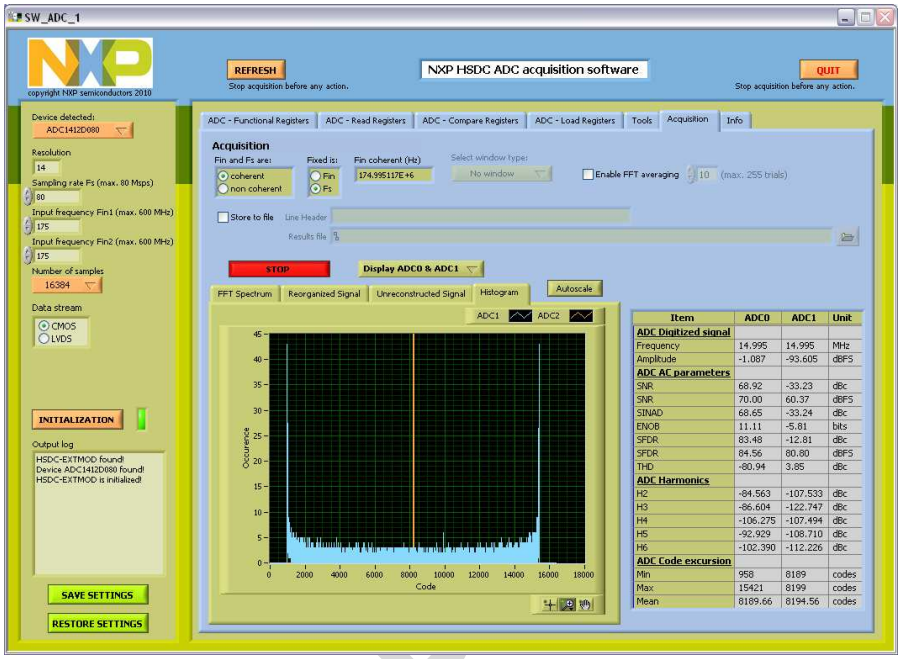


Fig 19. SW_ADC_1_r02: "Acquisition" page, code histogram graph

Press the "Autoscale" button to display the whole content.

The table shows the range of output codes.

3.3.7 Info page

This page will give practical information related to software and hardware settings:

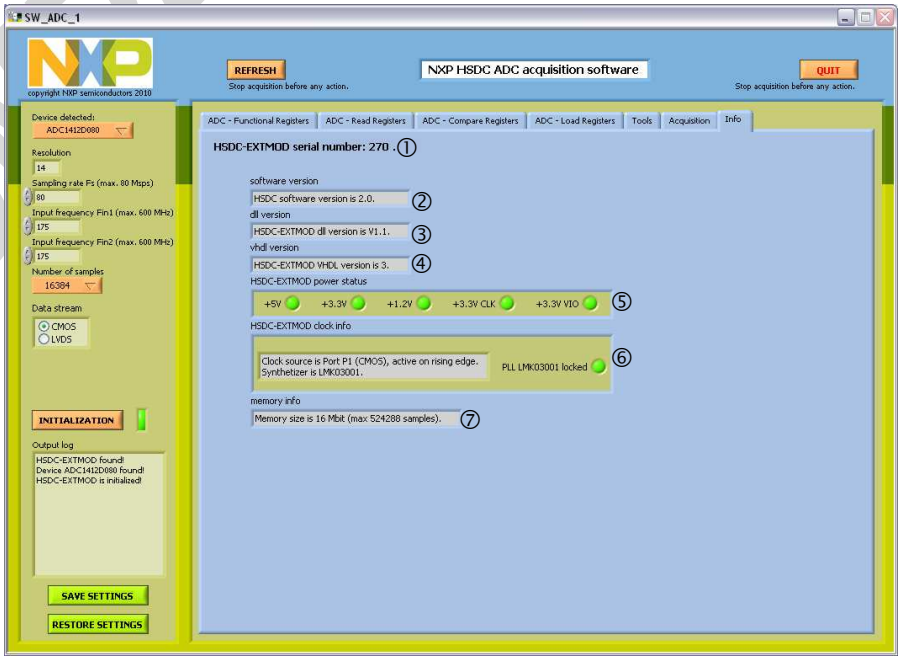


Fig 20. SW_ADC_1_r02: "Info" page

The information visible on this page are:

- board serial number ①;
- HSDC software release number ②;
- HSDC-EXTMOD dll version ③;
- HSDC-EXTMOD vhdl version ④;
- HSDC-EXTMOD supply status ⑤;
- HSDC-EXTMOD clock capability and status version ⑥;
- HSDC-EXTMOD memory capability ⑦.

4. Appendix A.1: coherency calculation

The coherency relies on the fact that clock and analog input signal are synchronized and the first and last samples being captured are adjoining samples: it ensures a continuous digitized time process for the FFT processing.

To achieve this, one has to follow the equation:

$$\frac{F_{in}}{F_s} = \frac{M}{N}$$

where M is an odd integer equal to the number of periods being acquired and N the number of samples acquired.

With Fin, Fs and N known, M has to be chosen such that it follows the equation above. To do this iterative calculation, one has to decide whether Fin or Fs is fixed.

To illustrate this process, let's consider our current example with Fin = 170 MHz, Fs = 125 Msps and N = 16384 samples acquired:

- if Fin is fixed, this leads to M = 36863 periods of input signal to be acquired and a real sampling frequency to be Fs = 124.995737 MHz;
- if Fs is fixed, this leads to M = 36863 periods of input signal to be acquired and a real input frequency to be Fin = 170.005798 MHz.

Those values needs to be programmed in the signal generator and clock generator before capture is done, otherwise the FFT calculation will lead to a non-coherent result as shown below:

Fig 21. SW_ADC_1_r02: "Acquisition" page, non-coherent capture example

The numbers given for SNR, SFDR are completely wrong if coherency is not respected.

5. Notes

For any question, feel free to contact us at the following e-mail dataconverter-support@nxp.com.

6. Contents

For more information, please visit: http://www.nxp.com
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Date of release: 17 December 2010
Document identifier: QS_ADC1412D_10.doc