STFI10NK60Z

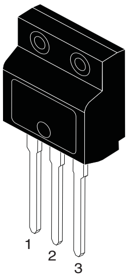
N-channel 600 V, 0.65 Ω, 10 A, Zener-protected SuperMESH™ Power MOSFET in I²PAKFP package

Datasheet — production data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STFI10NK60Z	600 V	< 0.75 Ω	10 A	35 W

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized



I²PAKFP (TO-281)

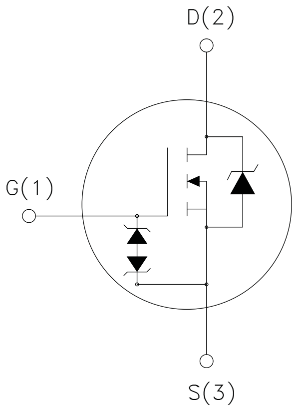
Applications

- Switching applications

Description

This device is an N-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well-established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Figure 1. Internal schematic diagram



AM01476v1

Table 1. Device summary

Order code	Marking	Package	Packaging
STFI10NK60Z	10NK60Z	I^2PAKFP (TO-281)	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	10(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	5.7 (1)	A
I_{DM} (2)	Drain current (pulsed)	36 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	35	W
ESD	Gate-source human body model (R=1,5 kΩ, C=100 pF)	4	kV
dv/dt (3)	Peak diode recovery voltage slope	4.5	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)	2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area
3. $I_{SD} < 10A$, $di/dt < 200A/\mu s$, V_{DD} =80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case Max	3.6	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb Max	62.5	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Repetitive or non repetitive avalanche current	9(1)	A
E_{AS}	Single pulse avalanche energy (starting Tj=25 °C, I_D=I_{AR}, V_{DD}= 50 V)	300	mJ

1. Limited by maximum junction temperature

2 Electrical characteristics

(Tcase = 25 °C unless otherwise specified).

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage, (V_{GS}= 0)	I_D = 250 µA	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V V_{DS} = 600 V, T_C= 125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 4.5 A		0.65	0.75	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15 V, I_D = 4.5 A	-	7.8		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	1370 156 37		pF pF pF
$C_{oss\ eq}$ (2)	Equivalent output capacitance	V_{GS}=0, V_{DS} =0 to 480 V	-	90		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=480 V, I_D = 8 A V_{GS} =10 V *(see Figure 16)*	-	50 10 25	70	nC nC nC

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=300 V, I_D=4 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 15)*	-	20 20	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=300 V, I_D=4 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 15)*	-	55 30	-	ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)		-		10 36	A A
V_{SD}(2)	Forward on voltage	I_{SD}=10 A, V_{GS}=0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=8 A, di/dt = 100 A/µs, V_{DD}=40 V, Tj=150 °C	-	570 4.3 15		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage (I_D=0)	I_{GS}= ± 1 mA	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device’s ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device’s integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

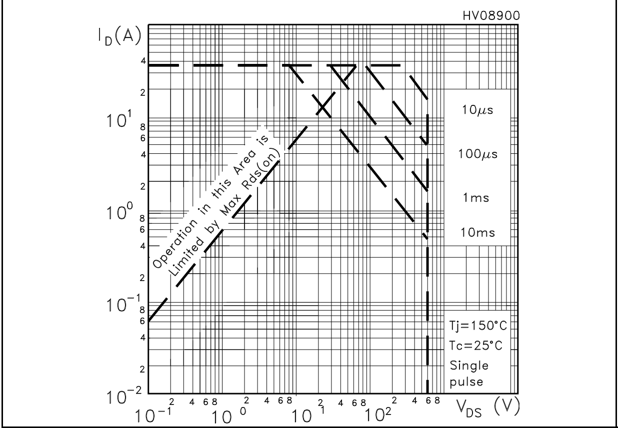


Figure 3. Thermal impedance

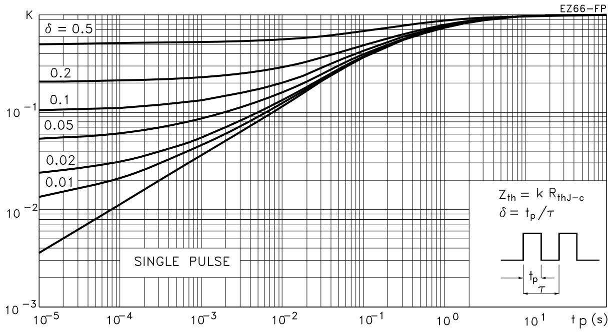


Figure 4. Output characteristics

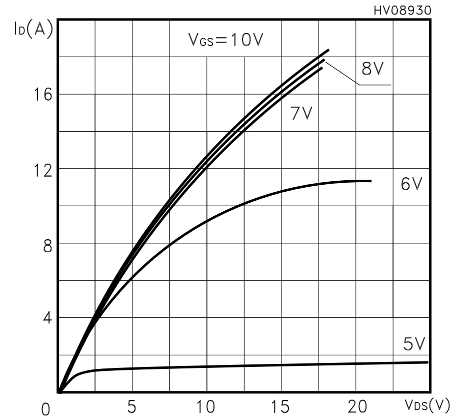


Figure 5. Transfer characteristics

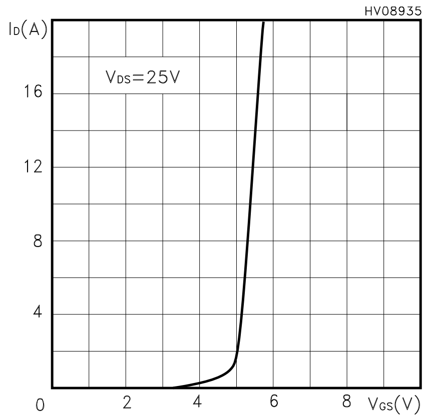


Figure 6. Transconductance

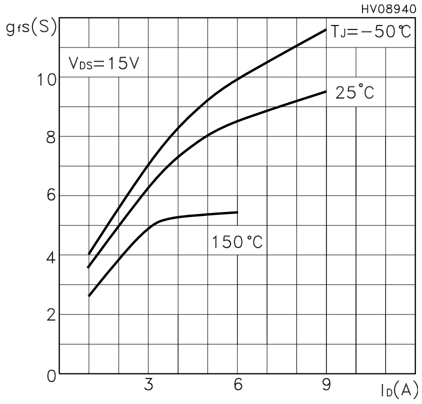


Figure 7. Static drain-source on resistance

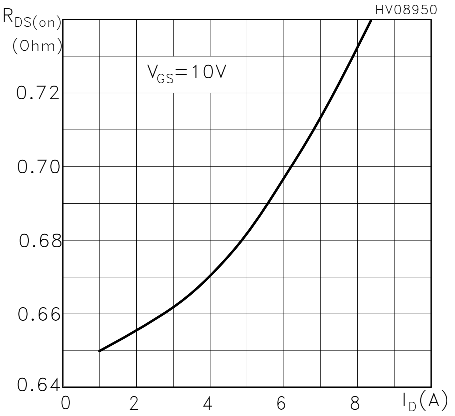


Figure 8. Gate charge vs gate-source voltage

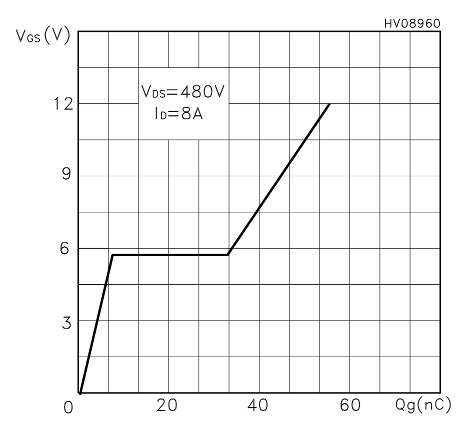


Figure 9. Capacitance variations

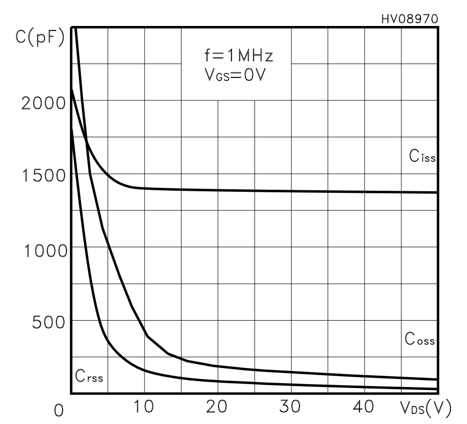


Figure 10. Normalized gate threshold voltage vs temperature

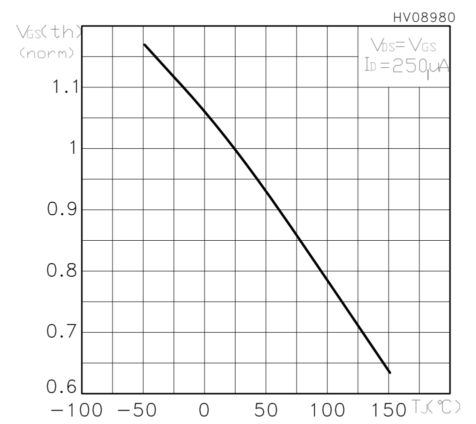


Figure 11. Normalized on resistance vs temperature

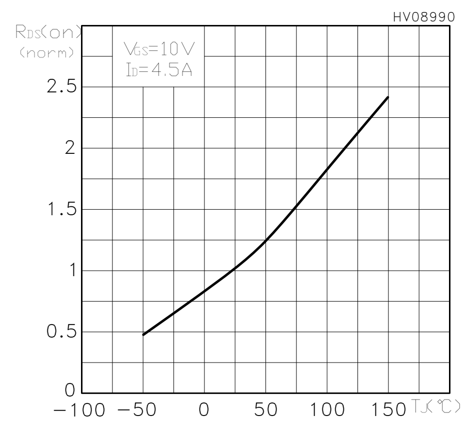


Figure 12. Source-drain diode forward characteristics

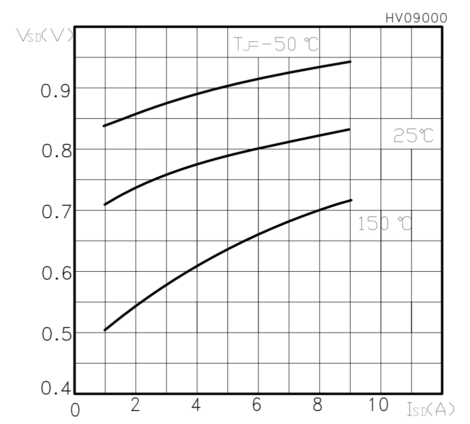


Figure 13. Maximum avalanche energy vs temperature

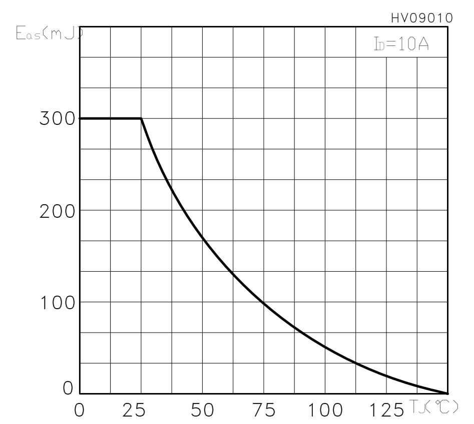
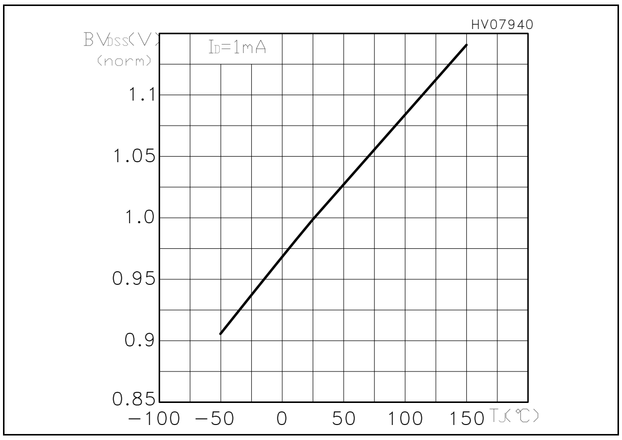


Figure 14. Normalized B_{VDSS} vs temperature



3 Test circuits

Figure 15. Switching times test circuit for resistive load

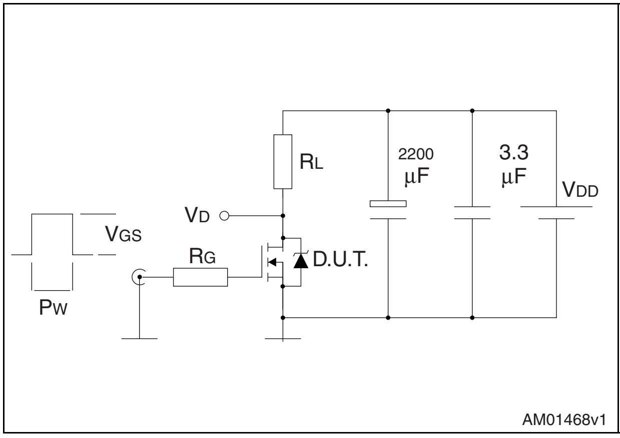


Figure 16. Gate charge test circuit

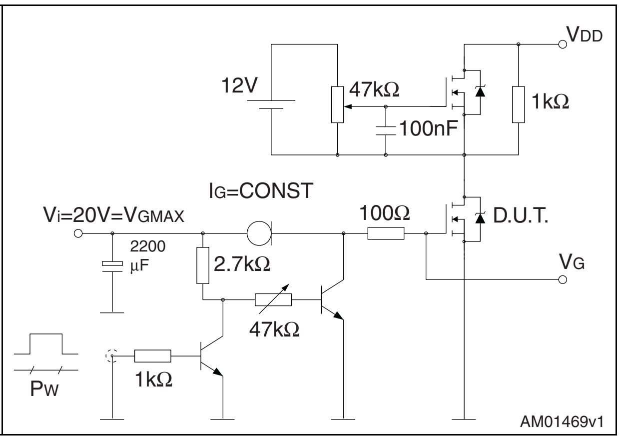


Figure 17. Test circuit for inductive load switching and diode recovery times

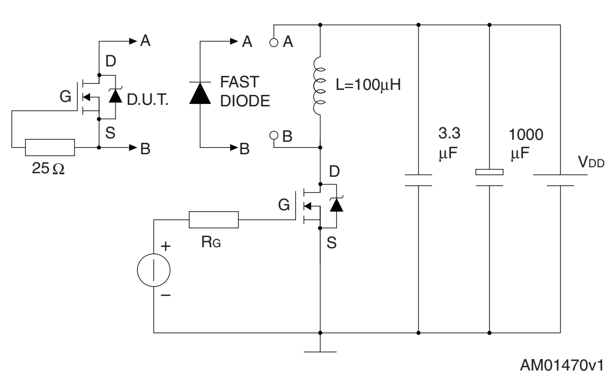


Figure 18. Unclamped inductive load test circuit

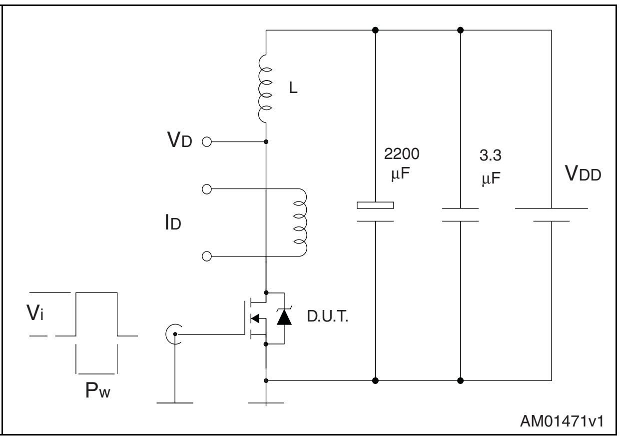


Figure 19. Unclamped inductive waveform

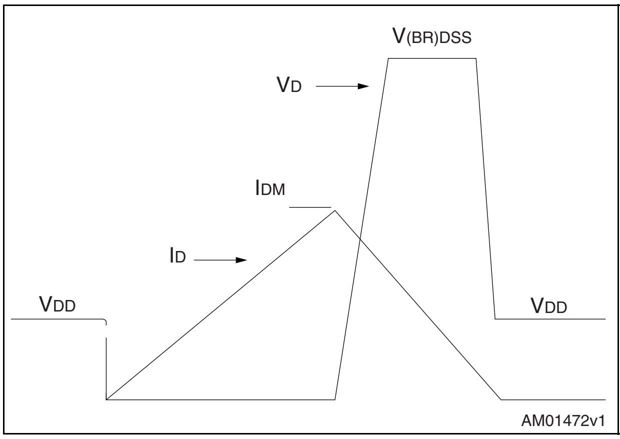
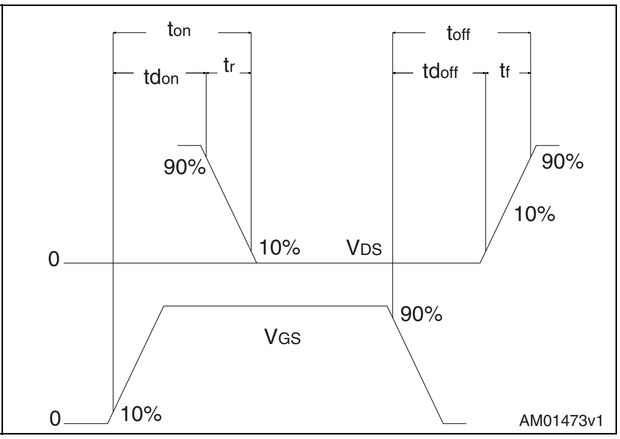


Figure 20. Switching time waveform



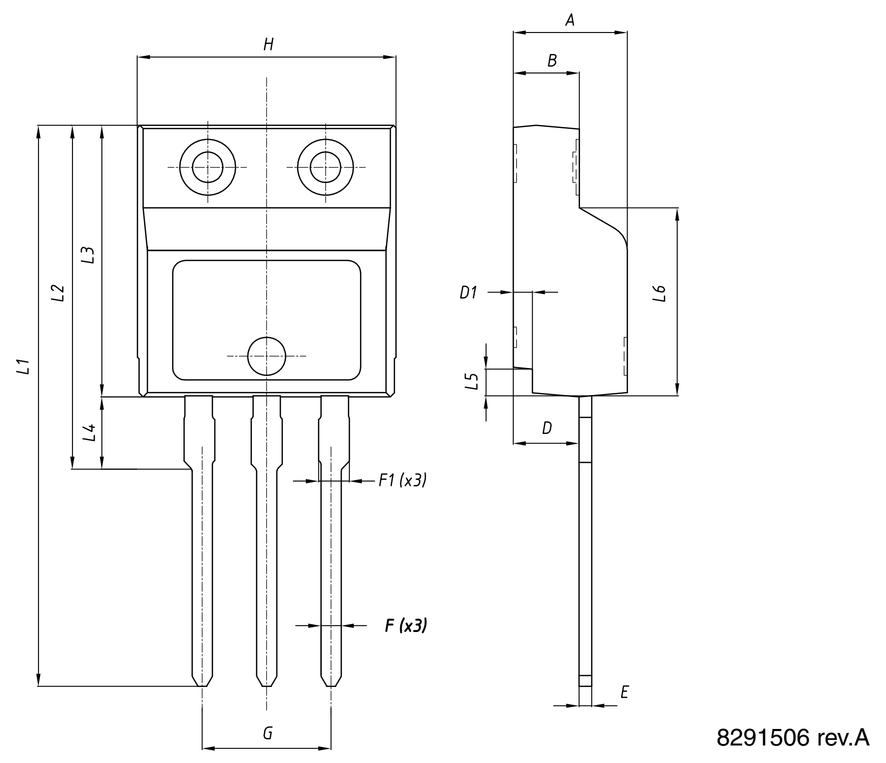
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 10. I^2PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 21. I^2PAKFP (TO-281) drawing



8291506 rev.A

5 Revision history

Table 11. Document revision history

Date	Revision	Changes
27-Jun-2011	1	First release
03-Nov-2011	2	*Figure 2: Safe operating area* and *Figure 3: Thermal impedance* have been added.
19-Mar-2012	3	Document status promoted from preliminary data to production data. Package name has been updated.

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