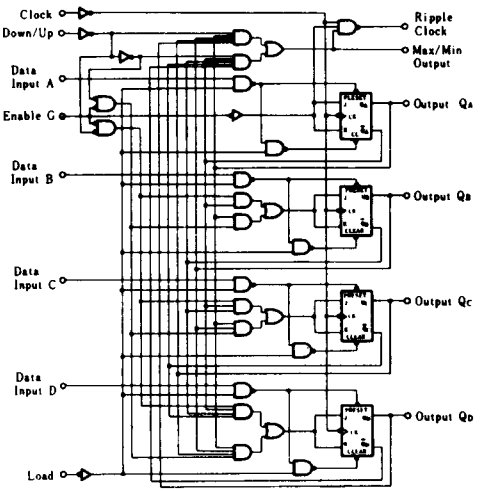
Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down. Level changes at the down/up input should be made only when the clock input is high. This counter is fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

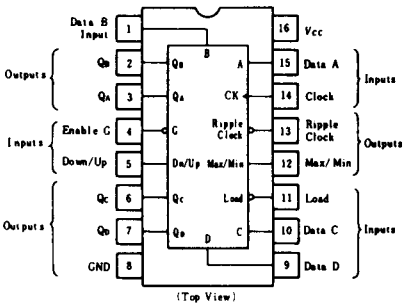
Two outputs have been made available to perform the cascading function; ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycles to the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists.

The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	20	MHz
Clock pulse width	$t_{w\ (CK)}$	25	—	—	ns
Load input pulse width	$t_{w\ (load)}$	35	—	—	ns
Setup time	t_{su}	20	—	—	ns
Hold time	t_h	3	—	—	ns
Enable time	t_{enable}	40	—	—	ns

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	–	–	V
		V_{IL}			–	–	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
		V_{OL}	$V_{CC}=4.75V$, $V_{IN}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$	–	–	0.4	V
				$I_{OL}=8mA$	–	–	0.5	
Input current	Enable	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	60	μA
	Others				–	–	20	
	Enable	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−1.2	mA
	Others				–	–	−0.4	
	Enable	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.3	mA
	Others				–	–	0.1	
Short-circuit output current		I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current**		I_{CC}	$V_{CC}=5.25V$		–	20	35	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

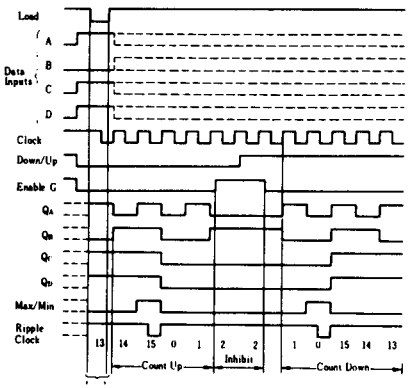
* V_{CC}=5V, Ta=25°C

** I_{CC} is measured with all outputs open and all inputs grounded.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$ $R_L=2k\Omega$	20	25	–	MHz
Propagation delay time	t_{PLH}	Load	Q_A, Q_B, Q_C, Q_D		–	22	33	ns
	t_{PHL}				–	33	50	
	t_{PLH}	Data A ,B,C,D	Q_A, Q_B, Q_C, Q_D		–	20	32	ns
	t_{PHL}				–	27	40	
	t_{PLH}	Clock	Ripple Clock		–	13	20	ns
	t_{PHL}				–	16	24	
	t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D		–	16	24	ns
	t_{PHL}				–	24	36	
	t_{PLH}	Clock	Max/Min		–	28	42	ns
	t_{PHL}				–	37	52	
	t_{PLH}	Down/Up	Ripple Clock		–	30	45	ns
	t_{PHL}				–	30	45	
	t_{PLH}	Down/Up	Max/Min		–	21	33	ns
	t_{PHL}				–	22	33	
	t_{PLH}	Enable	Ripple Clock		–	21	33	ns
	t_{PHL}				–	22	33	

■COUNT SEQUENCES



Illustrated below is the following sequence;

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.

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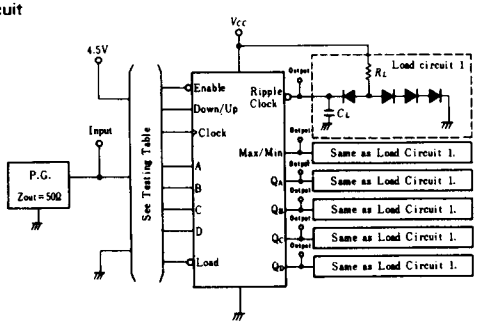
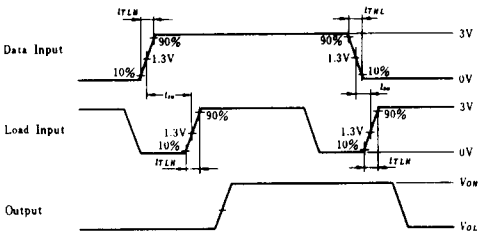
■TESTING METHOD

1) Test Circuit



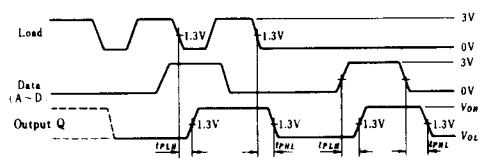
Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 (H).

Waveform



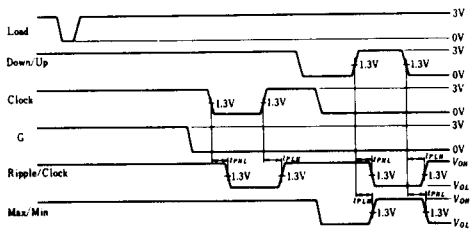
Input pulse: t_{TLH}, $t_{THL} \leqq 10$ns, PRR=1MHz, Duty cycle $\leqq$ 50%

Waveform 1. Load→Q, Data→Q

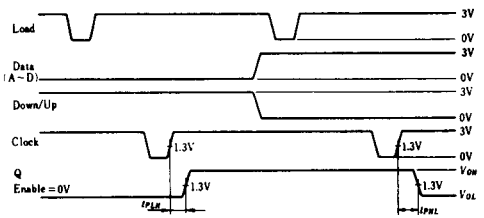


Note) Conditions on other inputs are irrelevant.

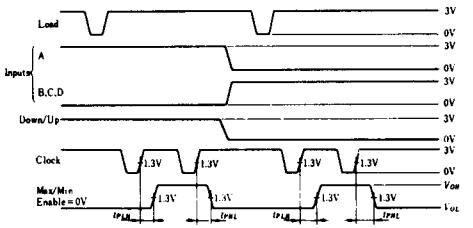
Waveform 2. G→Ripple CK, CK→Ripple CK, Down/Up→Ripple CK, Down/Up→Max/Min



Waveform 3. Clock→Q



Waveform 4. Clock→Max/Min



PACKAGING INFORMATIONS

T-90-20

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

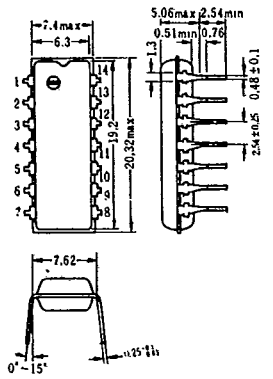
HD 74LS00 P

- Package ; Plastic DIP ; letters P
  Cerdip ; non-letters
- Circuit description
- Prefix : HD ; Hitachi Digital IC

■Plastic DIP

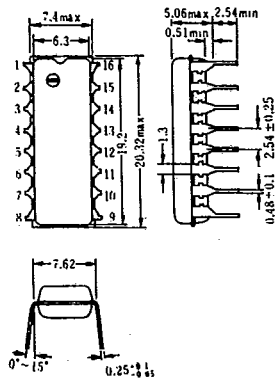
●14 Pin

DP-14



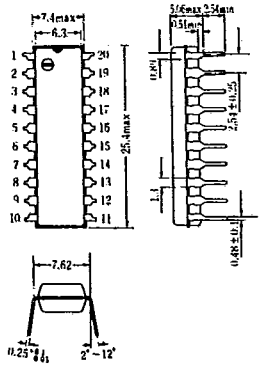
●16 Pin

DP-16



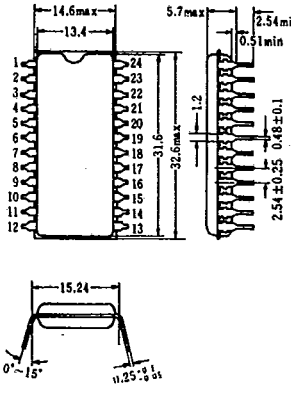
●20 Pin

DP-20



●24 Pin

DP-24



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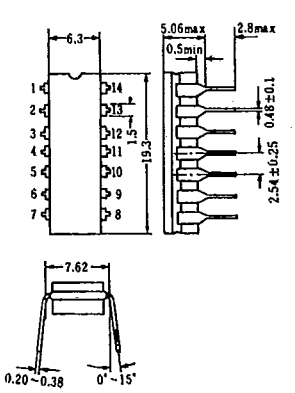
PACKAGING INFORMATIONS

■Cerdip

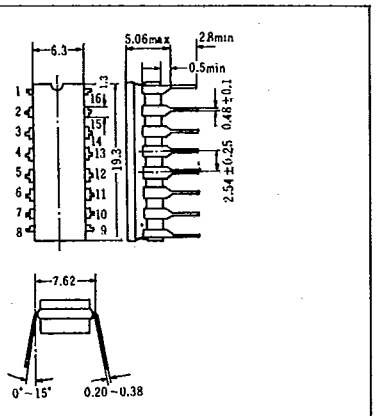
●14 Pin

DG-14



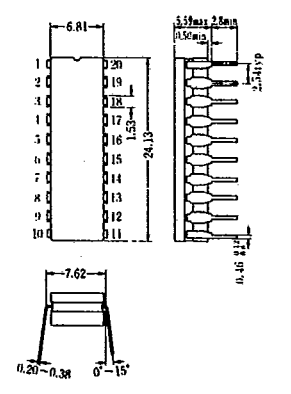
●16 Pin

DG-16



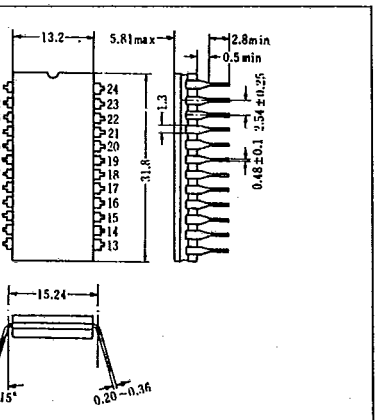
●20 Pin

DG-20



●24 Pin

DG-24



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