Preliminary Product Information

NEC

MOS Integrated Circuit

78K0/KF2

8-BIT SINGLE-CHIP MICROCONTROLLER

The 78K0/KF2 products are 8-bit single-chip microcontrollers of the 78K0 series.

These microcontrollers feature Single-voltage Self-programming Flash memory and many peripherals.

FEATURES

- 78K0 CPU core, 8-bit CISC architecture
- Flash EEPROM and RAM sizes

Item / Product name	Program memory (Flash EEPROM)	Data memory (RAM)
μPD78F0547	128K bytes (Flash)	7K bytes
μPD78F0546	96K bytes (Flash)	5K bytes
μPD78F0545	60K bytes (Flash)	3K bytes
μPD78F0544	48K bytes (Flash)	2K bytes

Minimum instruction cycle

0.1μs (20MHz@4.0V to 5.5V)

0.2μs (10MHz@2.7V to 5.5V)

0.4μs (5MHz@1.8V to 5.5V)

Clock

- MAIN CLOCK
  - Internal Ring-oscillator 8MHz (Typ.)
  - Ceramic/Crystal Oscillator/External CLK (2MHz to 20MHz)
    (Instruction execution time = 100ns(min.) @20MHz)
- SUB CLOCK
  - 32.768KHz Crystal oscillator/ External CLK
- WDT CLOCK
  - Internal Ring-oscillator 240KHz (Typ.)

Peripherals.

- On-Chip Power-On-Clear (POC) Circuit
- Low-Voltage Detector (LVI) Circuit
- Timer
  - 16bit Timer 2ch
  - 8bit Timer 4ch
  - Watch Timer
  - Watchdog Timer (Operable with 240KHz Ring-OSC)
- Serial Interface
  - UART/CSI 1ch
  - UART (with LIN-bus) 1ch
  - Auto-CSI 1ch
  - CSI 1ch
  - IIC 1ch
- Key Interrupt 8ch
- AD CONVERTER
  - 10-bit resolution A/D converter 8ch
- I/O PORT

  Total : 71

  CMOS I/O : 66

  CMOS Output: 1

  N-ch O.D I/O: 4
- MULTUPLIER/DIVIDER
  - 16bit x 16bit, 32bit / 16bit
- Other
  - Self programming
  - PCL / BUZ OUTPUT
  - On-chip debug function (Product name is undecided.)

Interrupt

- Internal 20ch
- External 9ch

Operation Voltage

1.8V to 5.5V

Package

80-pin LQFP (12mm x 12mm, 0.5mm pitch)

80-pin LQFP (14mm x 14mm, 0.65mm pitch)

This information contained in this document is being issued in advance of the production cycle for the product. The parameters for the product may change before final production or NEC Electronics Corporation, at its own discretion,, may withdraw the product prior to its production. Not all products and/ or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

ZUD-CC-04-0129-E
Data Published Oct 2004 N CP(K)

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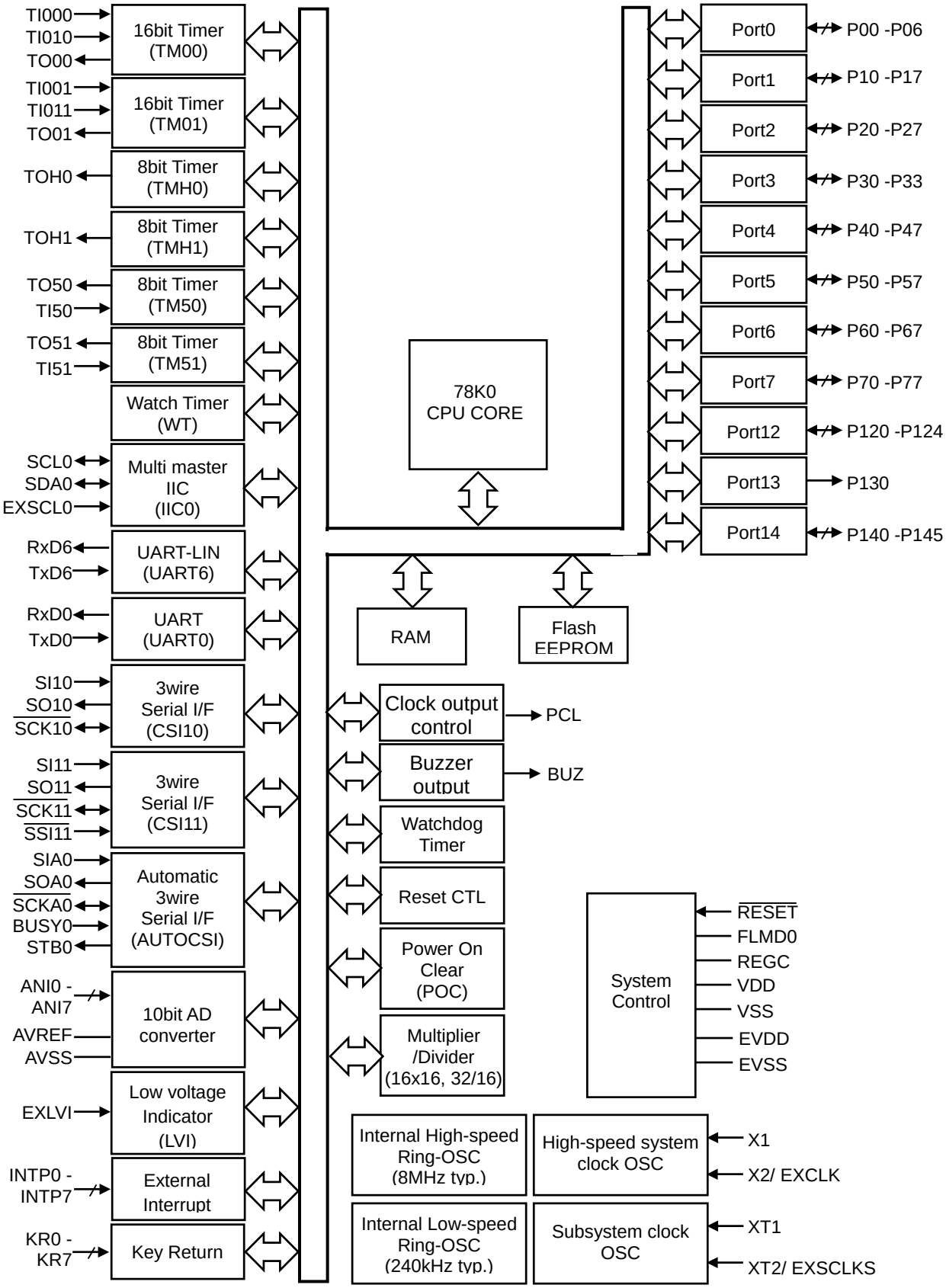
1. Block Diagram

Fig. 78K0/KF2



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2. Pin Lay Out

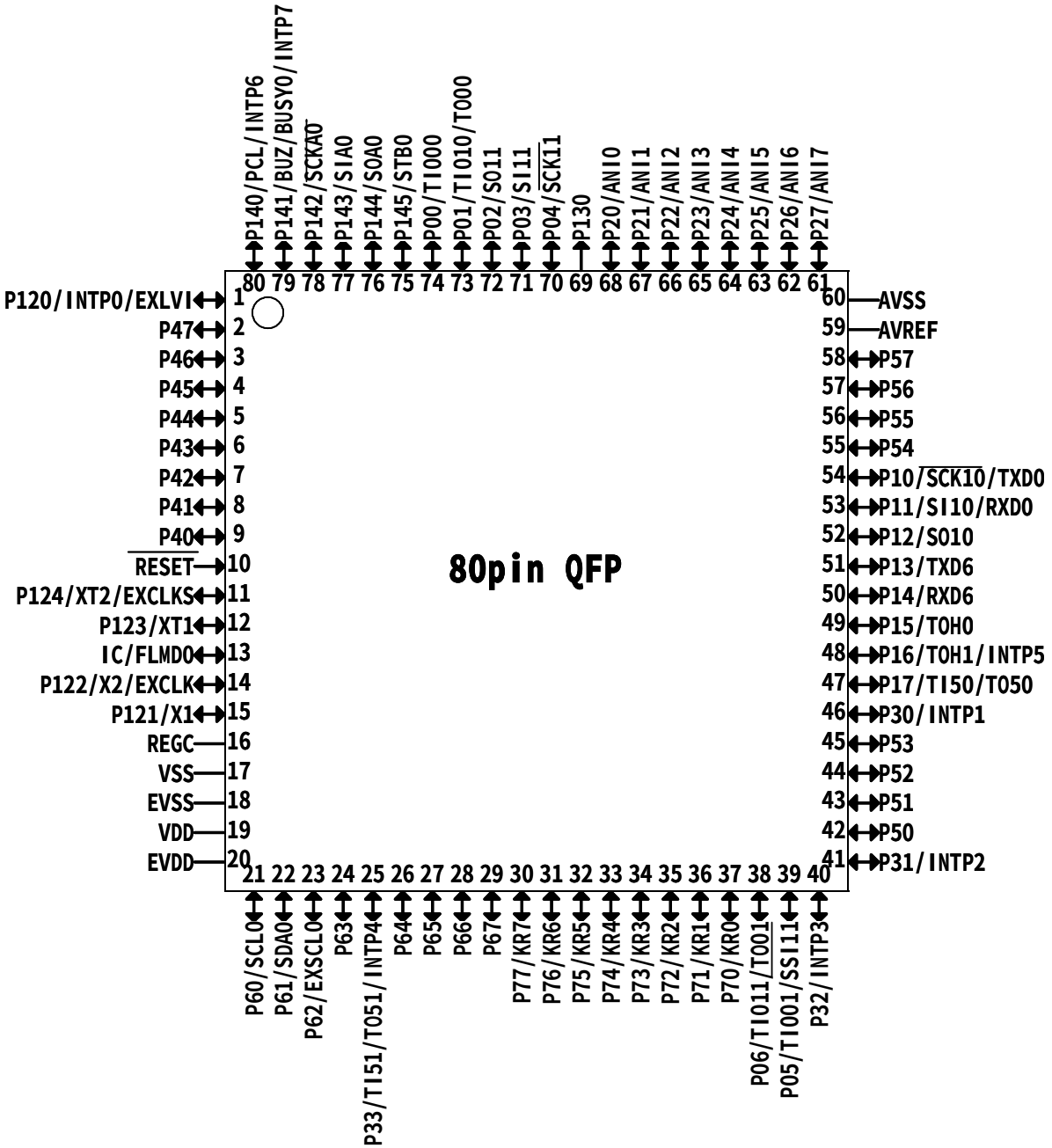
78K0/KF2

80-pin plastic QFP (14 x 14mm 0.65mm pitch)

μPD78F0547GC-UBT, μPD78F0546GC-UBT
μPD78F0545GC-UBT, μPD78F0544GC-UBT

80-pin plastic LQFP (12 x 12mm 0.5mm pitch)

μPD78F0547GK-8EU, μPD78F0546GK-8EU
μPD78F0545GK-8EU, μPD78F0544GK-8EU



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3. Pin Function

Table (1/2)

PIN NAME	Function
VDD	Positive power supply except for ports (except P20-P27 and P121-P124) and AD converter
VSS	Ground potential except for ports (except P20-P27 and P121-P124) and AD converter
EVDD	Positive power supply for ports (except P20-P27 and P121-P124)
EVSS	Ground potential for ports (except P20-P27 and P121-P124)
RESET	System reset input
FLMD0	Flash EEPROM programming mode setting
REGC	Connecting regulator stabilization capacitor. Connect to GND via a capacitor (0.47μF).
AVREF	A/D converter analog power supply and power supply for P20-P27
AVSS	Ground potential for A/D converter and P20 - P27.
P00 /TI000	I/O port
	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of16-bit timer/event counter 00 (TM00)
P01 /TI010 /TO00	I/O port
	Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00 (TM00)
	16-bit timer/event counter 00 output (TM00)
P02 /SO11	I/O port
	Serial data output from serial interface (CSI11)
P03 /SI11	I/O port
	Serial data input to serial interface (CSI11)
P04 /SCK11	I/O port
	Clock input/ output for serial interface (CSI11)
P05 /TI001 /SSI11	I/O port
	External count clock input to 16-bit timer/event counter 01 Capture trigger input to capture registers (CR001, CR011) of16-bit timer/event counter 01 (TM01)
	Chip select input for serial interface (CSI11)
P06 /TI011 /TO01	I/O port
	Capture trigger input to capture register (CR001) of 16-bit timer/event counter 01 (TM01)
	16-bit timer/event counter 01 output (TM01)
P10 /SCK10 /TXD0	I/O port
	Clock input/ output for serial interface (CSI10)
	Serial data output from asynchronous serial interface (UART0)
P11 /SI10 /RXD0	I/O port
	Serial data input to serial interface (CSI10)
	Serial data input to asynchronous serial interface (UART0)
P12 /SO10	I/O port
	Serial data output form serial interface (CSI10)
P13 /TXD6	I/O port
	Serial data output from asynchronous serial interface (UART6)
P14 /RXD6	I/O port
	Serial data input to asynchronous serial interface (UART6)
P15 /TOH0	I/O port
	8-bit timer H0 output (TMH0)
P16 /TOH1 /INTP5	I/O port
	8-bit timer H1 output (TMH1)
	External interrupt request input with specifiable valid edges
P17 /TI50 /TO50	I/O port
	External count clock input to 8-bit timer/event counter 50 (TM50)
	8-bit timer/event counter 50 output (TM50)

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Table(2/2)

PIN NAME	Function
P20- P27 / ANI0- ANI7	I/O ports A/D converter analog input
P30/INTP1	I/O port External interrupt request input with specifiable valid edges
P31/INTP2	
P32/INTP3	
P33 /TI51 /TO51 /INTP4	I/O port External count clock input to 8-bit timer/event counter 51(TM51) 8-bit timer/event counter 51output(TM51) External interrupt request input with specifiable valid edges
P40 - P47	I/O port
P50 – P57	I/O port
P60 /SCL0	I/O port (N-ch Open drain) Clock input/ output for serial interface (IIC0)
P61 /SDA0	I/O port (N-ch Open drain) Serial data input/ output for serial interface (IIC0)
P62 /EXSCL0	I/O port (N-ch Open drain) External clock input for serial interface (IIC0)
P63	I/O port (N-ch Open drain)
P64 – P67	I/O ports
P70 – P77 /KR0 – KR7	I/O ports Key interrupt input
P120 /INTP0 /EXLVI	I/O port External interrupt request input with specifiable valid edges Reference voltage input for Low voltage Indicator
P121 /X1	I/O port (An external oscillation circuit is not used) Connecting resonator for main system clock oscillation
P122 /X2 /EXCLK	I/O port (An external oscillation circuit is not used) Connecting resonator for main system clock oscillation External clock input for main system clock
P123 /XT1	I/O port (An external oscillation circuit is not used) Connecting resonator for subsystem clock oscillation
P124 /XT2 /EXCLKS	I/O port (An external oscillation circuit is not used) Connecting resonator for subsystem clock oscillation External clock input for subsystem clock
P130	Output port
P140 /PCL /INTP6	I/O port Clock output External interrupt request input with specifiable valid edge
P141 /BUZ / INTP7 / BUSY0	I/O port Buzzer output External interrupt request input with specifiable valid edge Busy signal input for serial interface (AUTOCSI)
P142 /SCKA0	I/O port Clock input/ output for serial interface (AUTOCSI)
P143 /SIA0	I/O port Serial data input to serial interface (AUTOCSI)
P144 /SOA0	I/O port Serial data output form serial interface (AUTOCSI)
P145 /STB0	I/O port Strobe signal input to serial interface (AUTOCSI)

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4. Memory space

78K0/KF2 have 64kB linear address area.

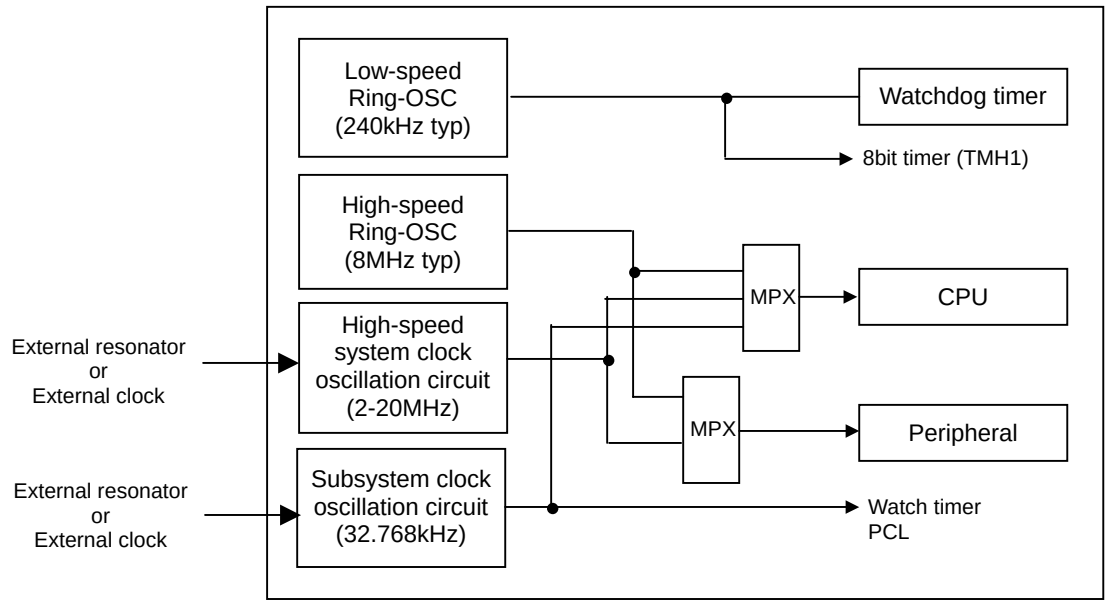
To access more than 64KB ROM area, 96KB and 128KB ROM products have BANK type ROM at address of 8000H to C000H. All BANK ROM size is 16KB.

5. Clock

Products	ROM size	Common ROM	Bank ROM	
		Address	Address	Number of Bank
μPD78F0547	128KB	0000H-7FFFH (32KB)	8000H-BFFFH (16KB)	6
μPD78F0546	96KB	0000H-7FFFH (32KB)	8000H-BFFFH (16KB)	4
μPD78F0545	60KB	0000H-EFFFH (60KB)	-	-
μPD78F0544	48KB	0000H-BFFFH (48KB)	-	-

78K0/KF2 have 2 type internal Ring-OSC and 2 type external resonator oscillation circuit.
78K0/KF2 can be operated high-speed internal Ring-OSC only. Low-speed Ring-OSC can connect to Watch dog timer and 8bit timer (TMH1) only for high secure.

Fig. Clock connecting block image



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6. Outline of Functions of KF2

		μPD78F0544	μPD78F0545	μPD78F0546	μPD78F0547
Internal Memory (Byte)	Flash Memory	48 K	60 K	96 K	128 K
	Bank	-	-	4	6
	High Speed RAM	1K			
	Extend RAM	1 K	2 K	4 K	6 K
Main System Clock	Ceramic/Crystal	- 2 to 20 MHz: V_{DD} = 4.0 to 5.5 V - 2 to 10 MHz: V_{DD} = 2.7 to 5.5 V - 2 to 5 MHz: V_{DD} = 1.8 to 5.5 V			
	Internal Ring-OSC	- 8 MHz(TYP.)			
Sub System Clock		- 32.768 kHz(TYP.)			
Internal Low Speed Ring-OSC (For TMH1, WDT)		- 240 kHz(TYP.)			
Minimum Instruction Cycle		- 0.1 μs (Ceramic/ Crystal Operation f_{XH} = 20 MHz V_{DD} = 4.0 to 5.5 V)			
I/O		Total :71 - CMOS I/O :66 - CMOS Out :1 - N-ch O.D. :4			
Timer		- 16 Bit Timer/Event Counter:2ch - 8 Bit Timer/Event Counter:2ch - 8 bit Timer:2ch - Watch Timer:1ch - Watch Dog Timer:1ch			
	Timer Output	-6(PWM:4)			
PCL output		- 156.25kHz, 312.5kHz, 615kHz, 1.25MHz, 2.5MHz, 5MHz, 10MHz (f_{PRS} = 20 MHz)			
Buzzer Output		- 2.44 kHz, 4.88 kHz, 9.77 kHz, 19.54 kHz(f_{PRS} = 20 MHz)			
A/D Converter		- 10bit x 8ch			
Serial Interface		- UART (with LIN-bus):1ch - CSI/ UART:1ch - CSI:1ch -Auto-CSI: 1chI - I^2C:1ch			
Multiplier/Divider		16bitx16bit, 32bit/8bit			
Interrupt	Internal	20			
	External	9			
Key Return		8ch			
On Chip Debug Function		Product name is undecided.			
Voltage Range		V_{DD} = 1.8 to 5.5 V			
Operation temperature		Ta = -40°C to +85°C			
Package		- 80pin LQFP(12x12) 0.5mm pitch - 80pin QFP(14x14) 0.65mm pitch			

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4. Electrical specification of KF2 (Target)

Caution These specifications show target values, which may change after device evaluation. The operating voltage range may also change.

Absolute Maximum Ratings(T_A = 25°C) (1/2)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			-0.5 to +6.5	V
	EV_{DD}			-0.5 to +6.5	V
	V_{SS}			-0.5 to +0.3	V
	EV_{SS}			-0.5 to +0.3	V
	AV_{REF}			-0.5 to +6.5	V
	AV_{SS}			-0.5 to +0.3	V
Input voltage	V_{I1}			-0.3 to V_{DD} = EV_{DD} +0.3 Note	V
	V_{I2}	P60-P63(N-ch open drain)		-0.3 to +6.5	V
Output voltage	V_O			-0.3 to V_{DD} = EV_{DD} +0.3 Note	V
Analog input voltage	V_{AN}			-0.3 to AV_{REF}+0.3 Note	V
Output current, high	I_{OH}	Per pin		-10	mA
		Total of all pins -80 mA	P00-P04, P40-P47, P120-P124, P130, P140-P145,	-25	mA
			P05-P06, P10-P17,P30-P33, P50-P57,P60-P67, P70-P77	-55	mA

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

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Absolute Maximum Ratings(T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, low	I_{OL}	Per pin		30	mA
		Total of all pins 200 mA	P00-P04, P40-P47, P120-P124, P130, P140-P145,	60	mA
			P05-P06, P10-P17,P30-P33, P50-P57,P60-P67, P70-P77	140	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

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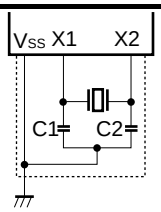
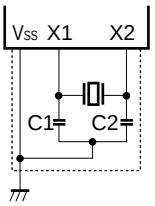
High-Speed System Clock (Crystal/Ceramic) Oscillator Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.3 V ≤ AV_{REF} ≤ V_{DD}= EV_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency(f_{XH})**Note**	4.0 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz
			2.7 V ≤ V_{DD} < 4.0 V	2.0		10.0	
			1.8 V ≤ V_{DD} < 2.7 V	2.0		5.0	
Crystal resonator		Oscillation frequency(f_{XH})**Note**	4.0 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz
			2.7 V ≤ V_{DD} < 4.0 V	2.0		10.0	
			1.8 V ≤ V_{DD} < 2.7 V	2.0		5.0	

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the high-speed system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the Ring-OSC after reset is released, check the oscillation stabilization time of the high-speed system clock using the oscillation stabilization time status register (OSTC). Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

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Ring-OSC Oscillator Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.3 V ≤ AV_{REF} ≤ V_{DD}= EV_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

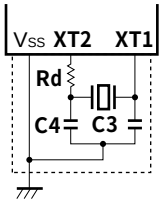
Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
8 MHz Ring-OSC oscillator	High-speed Ring-OSC Oscillation frequency(f_{RH})Note1	2.7 V ≤ V_{DD} ≤ 5.5 V	7.6 Note2	8.0 Note2	8.4 Note2	MHz
		1.8 V ≤ V_{DD} ≤ 5.5 V	T.B.D	8.0 Note2	T.B.D	
240 kHz Ring-OSC oscillator	Low-speed Ring-OSC Oscillation frequency(f_{RL})	2.7 V ≤ V_{DD} ≤ 5.5 V	216	240	264	kHz
		1.8 V ≤ V_{DD} ≤ 5.5 V	T.B.D	240	T.B.D	

Note 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2. This is the frequency in the case of RSTS(RCM.7)=1. This is 5 MHz(TYP.) in the case of RSTS=0.

Subsystem Clock Oscillator Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.3 V ≤ AV_{REF} ≤ V_{DD}= EV_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency(f_{SUB})Note		32	32.768	35	kHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the high-speed system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

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DC Characteristics (1/4)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH1}	Per pin of P00-P06, P10-P17, P30-P33, P40-P47, P50-P57, P64-P67, P70-P77, P120, P130, P140-P145	4.0V ≤ V_{DD} ≤ 5.5V			-3.0	mA
			2.7 V ≤ V_{DD} < 4.0V			-2.5	
			1.8 V ≤ V_{DD} < 2.7V			-1.0	
		Total of P00-P04, P40-P47, P120, P130, P140-P145	4.0V ≤ V_{DD} ≤ 5.5V			-20.0	mA
			2.7 V ≤ V_{DD} < 4.0V			-10.0	
			1.8 V ≤ V_{DD} < 2.7V			-5.0	
		Total of P05-P06, P10-P17, P30-P33, P50-P57, P64-P67, P70-P77	4.0V ≤ V_{DD} ≤ 5.5V			-30.0	mA
			2.7 V ≤ V_{DD} < 4.0V			-19.0	
			1.8 V ≤ V_{DD} < 2.7V			-10.0	
		Total of all pins	4.0V ≤ V_{DD} ≤ 5.5V			-50.0	mA
			2.7 V ≤ V_{DD} < 4.0V			-29.0	
			1.8 V ≤ V_{DD} < 2.7V			-15.0	
	I_{OH2}	Per pin of P20-P27, P121-P124 Note	1.8V ≤ V_{DD} ≤ 5.5V			-0.1	mA
Output current, low	I_{OL1}	Per pin of P00-P06, P10-P17, P30-P33, P40-P47, P50-P57, P64-P67, P70-P77, P120, P130, P140-P145	4.0V ≤ V_{DD} ≤ 5.5V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0V			5.0	
			1.8 V ≤ V_{DD} < 2.7V			2.0	
		Per pin of P60-P63	4.0V ≤ V_{DD} ≤ 5.5V			15.0	mA
			2.7 V ≤ V_{DD} < 4.0V			5.0	
			1.8 V ≤ V_{DD} < 2.7V			2.0	
		Total of P00-P04, P40-P47, P120, P130, P140-P145	4.0V ≤ V_{DD} ≤ 5.5V			20.0	mA
			2.7 V ≤ V_{DD} < 4.0V			15.0	
			1.8 V ≤ V_{DD} < 2.7V			9.0	
		Total of P05-P06, P10-P17, P30-P33, P50-P57, P64-P67, P70-P77	4.0V ≤ V_{DD} ≤ 5.5V			45.0	mA
			2.7 V ≤ V_{DD} < 4.0V			35.0	
			1.8 V ≤ V_{DD} < 2.7V			20.0	
		Total of all pins	4.0V ≤ V_{DD} ≤ 5.5V			65.0	mA
			2.7 V ≤ V_{DD} < 4.0V			50.0	
			1.8 V ≤ V_{DD} < 2.7V			29.0	
	I_{OL2}	Per pin of P20-P27, P121-P124 Note	1.8V ≤ V_{DD} ≤ 5.5V			0.4	mA

Note When used as digital input ports, set AV_{REF} = V_{DD}. = EV_{DD}.

Caution This specification is Duty = 70% condition of I_{OH} and I_{OL}.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

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DC Characteristics (2/4)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P02, P12, P13, P15, P40-P47, P50-P57, P60-P67, P121-P124, P144-P145	0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00, P01, P03-P06, P10-P11, P14, P16-P17, P30-P33, P70-P77, P120, P140-P143, $\overline{\text{RESET}}$	0.8V_{DD}		V_{DD}	V
	V_{IH3}	P20-P27 **Note**	0.7AV_{REF}		AV_{REF}	V
Input voltage, low	V_{IL1}	P02, P12, P13, P15, P40-P47, P50-P57, P60-P67, P121-P124, P144-P145	0		0.3V_{DD}	V
	V_{IL2}	P00, P01, P03-P06, P10-P11, P14, P16-P17, P30-P33, P70-P77, P120, P140-P143, $\overline{\text{RESET}}$	0		0.2V_{DD}	V
	V_{IL3}	P20-P27 **Note**	0		0.3AV_{REF}	V

Note When used as digital input ports, set AV_{REF} = V_{DD} = EV_{DD}.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

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DC Characteristics (3/4)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	I_{OH} = -3.0 mA	P00-P06, P10-P17, P30-P33, P40-P47, P50-P57, P64-P67, P70-P77, P120, P130, P140-P145	4.0V ≤ V_{DD} ≤ 5.5V	V_{DD}-0.7			V
		I_{OH} = -2.5 mA		2.7 V ≤ V_{DD} ≤ 5.5V	V_{DD}-0.5			V
		I_{OH} = -1.0 mA		1.8 V ≤ V_{DD} ≤ 5.5V	V_{DD}-0.5			V
	V_{OH2}	I_{OH} = -0.1 mA	P20-P27 P121-P124	1.8 V ≤ V_{DD} ≤ 5.5 V AV_{REF} = V_{DD} = EV_{DD}	V_{DD}-0.5			V
Output voltage, low	V_{OL1}	I_{OL} = 8.5 mA	P00-P06, P10-P17, P30-P33, P40-P47, P50-P57, P64-P67, P70-P77, P120, P130, P140-P145	4.0V ≤ V_{DD} ≤ 5.5V			0.7	V
		I_{OL} = 1.0 mA		2.7 V ≤ V_{DD} ≤ 5.5V			0.5	V
		I_{OL} = 0.5 mA		1.8 V ≤ V_{DD} ≤ 5.5V			0.4	V
	V_{OL2}	I_{OL} = 0.4 mA	P20-P27 P121-P124	1.8 V ≤ V_{DD} ≤ 5.5 V AV_{REF} = V_{DD} = EV_{DD}			0.4	V
	V_{OL3}	I_{OL} = 15.0 mA	P60-P63	4.0V ≤ V_{DD} ≤ 5.5V			2.0	V
		I_{OL} = 5.0 mA					0.4	V
		I_{OL} = 3.0 mA		2.7 V ≤ V_{DD} ≤ 5.5V			0.4	V
		I_{OL} = 2.0 mA		1.8 V ≤ V_{DD} ≤ 5.5V			0.4	V
Input leakage current, high	I_{LIH1}	V_I = V_{DD} = EV_{DD}	P00-P06, P10-P17, P30-P33, P40-P47, P50-P57, P64-P67, P70-P77, P120-P124, P130, P140-P145				1	μA
	I_{LIH2}	V_I = AV_{REF}	P20-P27				1	μA
	I_{LIH3}	V_I = V_{DD} = EV_{DD}	X1, X2, XT1, XT2 (When use External oscillator)				20	μA
Input leakage current, low	I_{LIL1}	V_I = V_{SS} = EV_{SS}	P00-P06, P10-P17, P30-P33, P40-P47, P50-P57, P64-P67, P70-P77, P120-P124, P130, P140-P145				-1	μA
	I_{LIL2}	V_I = AV_{REF}	P20-P27				-1	μA
	I_{LIL3}	V_I = V_{SS} = EV_{SS}	X1, X2, XT1, XT2 (When use External oscillator)				-20	μA
Pull-up resistance value	R_U	V_I = V_{DD} = EV_{DD}			10	20	100	kΩ
FLMD0 supply voltage	V_{IL}	In normal operation mode			0		0.2V_{DD}	V
	V_{IH}	In flash memory programming mode			0.8V_{DD}		V_{DD}	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

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DC Characteristics (4/4)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.3 V ≤ AV_{REF} ≤ V_{DD} =EV_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current[Note1]	I_{DD1}	Operation mode	f_{XH} = 20 MHz [Note2], V_{DD} = 5.0 V		4.7	5.8	mA
			f_{XH} = 10 MHz [Note2], V_{DD} = 5.0 V [Note3]		2.5	3.5	mA
			f_{XH} = 5 MHz [Note2], V_{DD} = 3.0 V [Note3]		1.5	2.2	mA
			f_{RH} = 8 MHz [Note2], V_{DD} = 5.0 V		1.9	2.7	mA
			f_{SUB} = 32.768 kHz [Note2], V_{DD} = 5.0 V		17	T.B.D.	μA
	I_{DD2}	HALT mode	f_{XH} = 20 MHz [Note2], V_{DD} = 5.0 V		2.2	2.6	mA
			f_{XH} = 10 MHz [Note2], V_{DD} = 5.0 V [Note3]		1.0	1.2	mA
			f_{XH} = 5 MHz [Note2], V_{DD} = 3.0 V [Note3]		0.55	0.65	mA
			f_{RH} = 8 MHz [Note2], V_{DD} = 5.0 V		0.6	0.65	mA
			f_{SUB} = 32.768 kHz [Note2], V_{DD} = 5.0 V		3.5	T.B.D.	μA
	I_{DD3}	STOP mode	V_{DD} = EV_{DD} = 5.0 V		1	20	μA
	I_{ADC}	A/D converter operating current	A/D converter operating		0.57	1.3	mA
			A/D converter not operating		T.B.D.	T.B.D.	mA
	I_{WDT}	Watchdog Time operating current	240 kHz Ring-OSC operating		5	10	μA
	I_{LVI}	LVI operating current			9	T.B.D.	μA

Notes 1. Total current flowing through the internal power supply (V_{DD}).
2. Input square-wave
3. When AMPH(OSCCTL.0) = 0.

Remark 1. f_{XH}: High-Speed System Clock oscillation frequency (X1 clock oscillation frequency or External main system clock frequency).
2. f_{RH}: High-speed Ring-OSC oscillation frequency.
3. f_{SUB}: Subsystem Clock oscillation frequency (XT1 clock oscillation frequency or External subsystem clock frequency).

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AC Characteristics

(1)Basic operation

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.3 V ≤ AV_{REF} ≤ V_{DD} =EV_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock(f_{XP}) operation	High-speed system clock(f_{XH})	4.0 V ≤ V_{DD} ≤5.5 V	0.1		16	μs
				2.7 V ≤ V_{DD} < 4.0 V	0.2		16	μs
				1.8 V ≤ V_{DD} < 2.7 V	0.4		16	μs
			High-speed Ring-OSC clock(f_{RH})	2.7 V ≤ V_{DD} < 5.5 V	0.25		4	μs
				1.8 V ≤ V_{DD} < 2.7 V	0.5		4	μs
		Subsystem clock(f_{SUB})operation			114	122	125	μs
External main system clock frequency	f_{EXCLK}	4.0 V ≤ V_{DD} ≤ 5.5 V			2.0		20.0	MHz
		2.7 V ≤ V_{DD} < 4.0 V			2.0		10.0	MHz
		1.8 V ≤ V_{DD} < 2.7 V			2.0		5.0	MHz
External main system clock input high-/low-level width	t_{EXCLKH}, t_{EXCLKL}				(1/ f_{EXCLK} x 1/2) - 1			ns
External subsystem clock frequency	f_{EXCLKS}				32	32.768	35	kHz
External subsystem clock input high-/low-level width	$t_{EXCLKSH}$, $t_{EXCLKSL}$				(1/ f_{EXCLKS} x 1/2) - 5			ns
TI000, TI010, TI001, TI011 input high-level width, low-level width	t_{TIH0}, t_{TIL0}	4.0 V ≤ V_{DD} ≤ 5.5 V			2/f_{sam} + 0.1 Note1			μs
		2.7 V ≤ V_{DD} < 4.0 V			2/f_{sam} + 0.2 Note1			μs
TI50, TI51 input frequency	f_{TI5}	4.0 V ≤ V_{DD} ≤ 5.5 V					10	MHz
		2.7 V ≤ V_{DD} < 4.0 V					10	MHz
		1.8 V ≤ V_{DD} < 2.7 V					5	MHz
TI50, TI51 input high-level width, low-level width	t_{TIH5}, t_{TIL5}	4.0 V ≤ V_{DD} ≤ 5.5 V			50			ns
		2.7 V ≤ V_{DD} < 4.0 V			50			ns
		1.8 V ≤ V_{DD} < 2.7 V			100			ns
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}				1			μs
Key return input low-level width	t_{KR}				250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10 Note2			μs

Notes 1. Selection of f_{sam} = f_{PRS}, f_{PRS} /4, f_{PRS} /256 or f_{PRS}, f_{PRS} /16, f_{PRS} /64 is possible using bits 0 and 1 (PRM000, PRM001 or PRM010,PRM011) of prescaler mode register 00 and 01 (PRM00,PRM01). Note that when selecting the TI000 or TI001 valid edge as the count clock, f_{sam} = f_{PRS}.

2. Input low level signal into $\overline{\text{RESET}}$ pin until power supply voltage is stabilized in the case of the power supply voltage rise time is slowly (more than 3.4ms).

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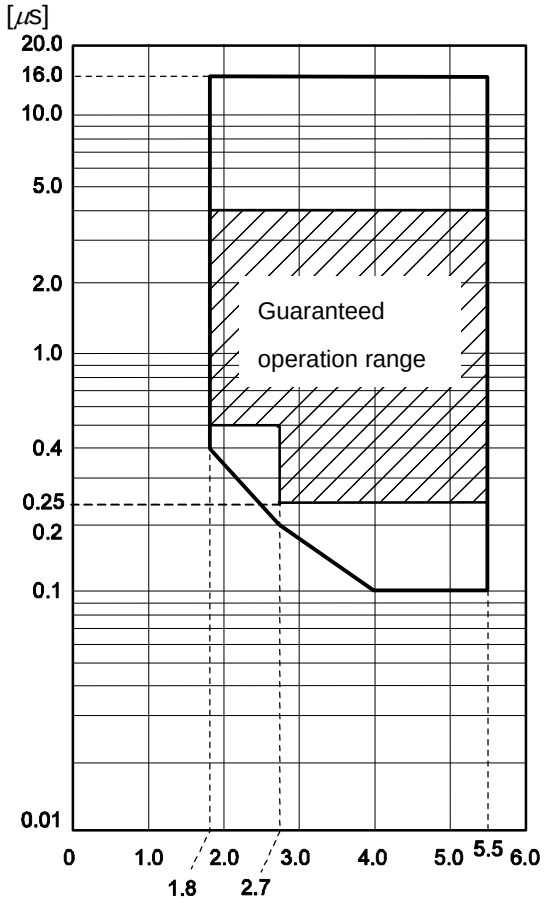
T_{CY} vs V_{DD} (main system clock operation)



Remark The values indicated by the shaded section are only when the High-speed Ring-OSC clock is selected.

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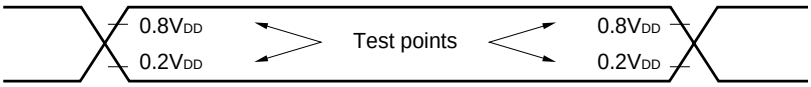
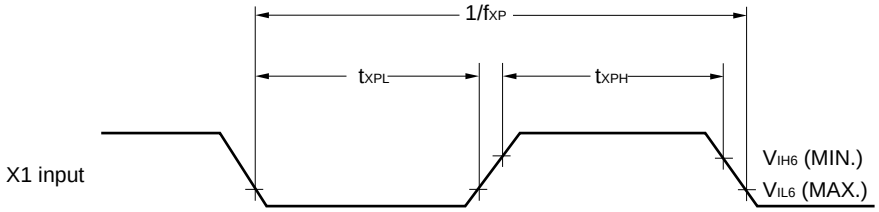
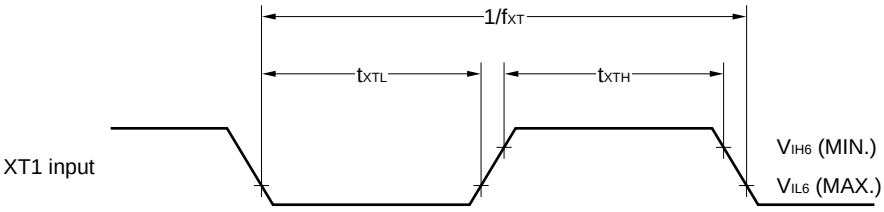
AC Timing Test Points (Excluding X1 Input)

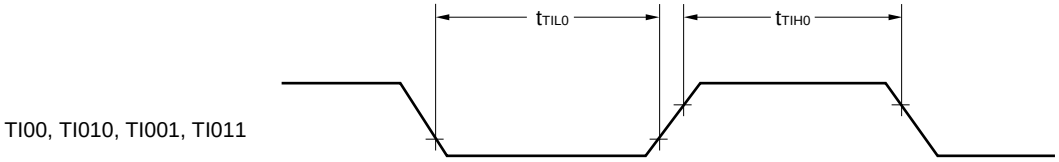


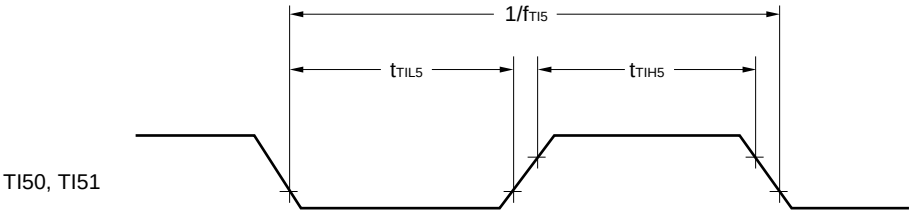
Clock Timing



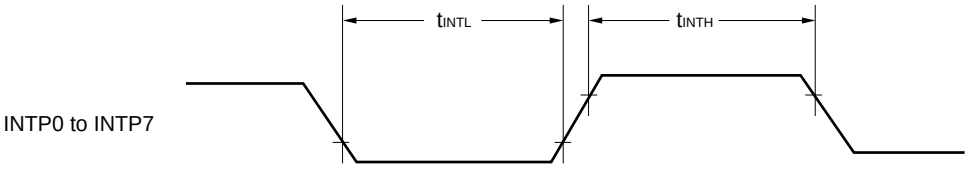


TI Timing

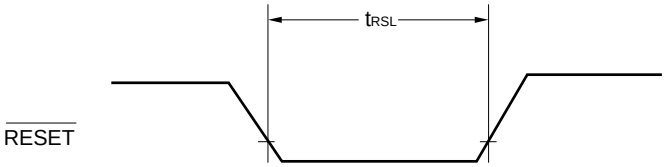




Interrupt Request Input Timing



RESET Input Timing



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(2) Serial interface

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.3 V ≤ AV_{REF} ≤ V_{DD}= EV_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

(a)UART mode (UART6, dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					312.5	kbps

(b) UART mode (UART0, dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					312.5	kbps

(c) IIC0 mode

Parameter	Symbol	Normal mode		High speed mode		Unit
		MIN.	. MAX	MIN.	. MAX	
SCL0 clock frequency	f_{CLK}	0	100	0	400	kHz
Start/restart condition setup time[Note1]	$t_{SU: STA}$	4.8	-	0.7	-	μs
hold time	$t_{HD: STA}$	4.1	-	0.7	-	μs
Hold time in SCL = ”L”	t_{LOW}	5.0	-	1.25	-	μs
Hold time in SCL = ”H”	t_{HIGH}	5.0	-	1.25	-	μs
Data setup time (reception)	$t_{SU: DAT}$	0	-	0	-	μs
Data hold time (sending)[Note2]	$t_{HD: DAT}$	0.47	4.0	0.23	1.00	μs

Notes 1. The first clock pulse is generated after this period in the case of the start/restart condition.

2. The MAX of $t_{HD:DAT}$ is normal transition value. Wait is occurred in the term of ACK(acknowledge) .

Caution Specification at 1.8 V ≤ V_{DD} < 2.7V is not fixed.

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(d) 3-wire serial I/O mode (CSI10, CSI11 master mode, $\overline{SCK1n}$…internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1n}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.0 V	200			ns
$\overline{SCK1n}$ high-/low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2 - 10[Not1]			ns
SI1n setup time (to $\overline{SCK1n}$↑)	t_{SIK1}		30			ns
SI1n hold time (to $\overline{SCK1n}$↑)	t_{KSI1}		30			ns
Delay time from $\overline{SCK1n}$↓ to SO1n output	t_{KSO1}	C = 50 pF[Note2]			40	ns

Notes 1. This is the value when the high-speed system clock (f_{XH}) is operating.
2. C is the load capacitance of the SCK1n and SO1n output lines.

(e) 3-wire serial I/O mode (CSI10, CSI11 slave mode, $\overline{SCK1n}$…external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1n}$ cycle time	t_{KCY2}		400			ns
$\overline{SCK1n}$ high-/low-level width	t_{KH2}, t_{KL2}		T.B.D			ns
SI1n setup time (to $\overline{SCK1n}$↑)	t_{SIK2}		80			ns
SI1n hold time (to $\overline{SCK1n}$↑)	t_{KSI2}		50			ns
Delay time from $\overline{SCK1n}$↓ to SO1n output	t_{KSO2}	C = 50 pF[Note]			120	ns

Note C is the load capacitance of the SO1n output lines.

Remark n = 0, 1

Caution Specification at 1.8 V ≤ V_{DD} < 2.7V is not fixed.

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(f) 3-wire serial I/O mode with automatic transmit/ receive function (AUTOCSI $\overline{SCKA0}$•••internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKA0}$ cycle time	t_{KCY3}	4.0 V ≤ V_{DD} ≤ 5.5 V		600			ns
		2.7 V ≤ V_{DD} < 4.0 V		1200			ns
$\overline{SCKA0}$ high-/low-level width	t_{KH3}	4.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY3}/2 - 50$ Not1			ns
	t_{KL3}	2.7 V ≤ V_{DD} < 4.0 V		$t_{KCY3}/2 - 100$ Not1			ns
SIA0 setup time (to $\overline{SCKA0}$↑)	t_{SIK3}			100			ns
SIA0 hold time (to $\overline{SCKA0}$↑)	t_{KSI3}			300			ns
Delay time from $\overline{SCKA0}$↓ to SOA0	t_{KSO3}	C = 100 pF Note2	4.0 V ≤ V_{DD} ≤ 5.5 V			200	ns
			2.7 V ≤ V_{DD} < 4.0 V			300	ns
Time from $\overline{SCKA0}$↑ to STB0↑	t_{SBD}			$t_{KCY3}/2 - 100$ Not1			ns
Strobe signal high level width	t_{SBW}	4.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY3} - 30$ Not1			ns
		2.7 V ≤ V_{DD} < 4.0 V		$t_{KCY3} - 60$ Not1			ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}			100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.0 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.7 V ≤ V_{DD} < 4.0 V		150			ns
Time from busy inactive to $\overline{SCKA0}$↓	t_{SPS}					$2t_{KCY3}$	ns

Notes 1. This is the value when the high-speed system clock (f_{XH}) is operating.
2. C is the load capacitance of the SCKA0 and SOA0 output lines.

(g) 3-wire serial I/O mode with automatic transmit/ receive function (AUTOCSI $\overline{SCKA0}$•••external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKA0}$ cycle time	t_{KCY4}	4.0 V ≤ V_{DD} ≤ 5.5 V		600			ns
		2.7 V ≤ V_{DD} < 4.0 V		1200			ns
$\overline{SCKA0}$ high-/low-level width	t_{KH4}	4.0 V ≤ V_{DD} ≤ 5.5 V		T.B.D			ns
	t_{KL4}	2.7 V ≤ V_{DD} < 4.0 V		T.B.D			ns
SIA0 setup time (to $\overline{SCKA0}$↑)	t_{SIK4}			100			ns
SIA0 hold time (to $\overline{SCKA0}$↑)	t_{KSI4}			300			ns
Delay time from $\overline{SCKA0}$↓ to SOA0 output	t_{KSO4}	C = 50 pF Note	4.0 V ≤ V_{DD} ≤ 5.5 V			200	ns
			2.7 V ≤ V_{DD} < 4.0 V			300	ns

Note C is the load capacitance of the SOA0 output lines.

Caution Specification at 1.8 V ≤ V_{DD} < 2.7V is not fixed.

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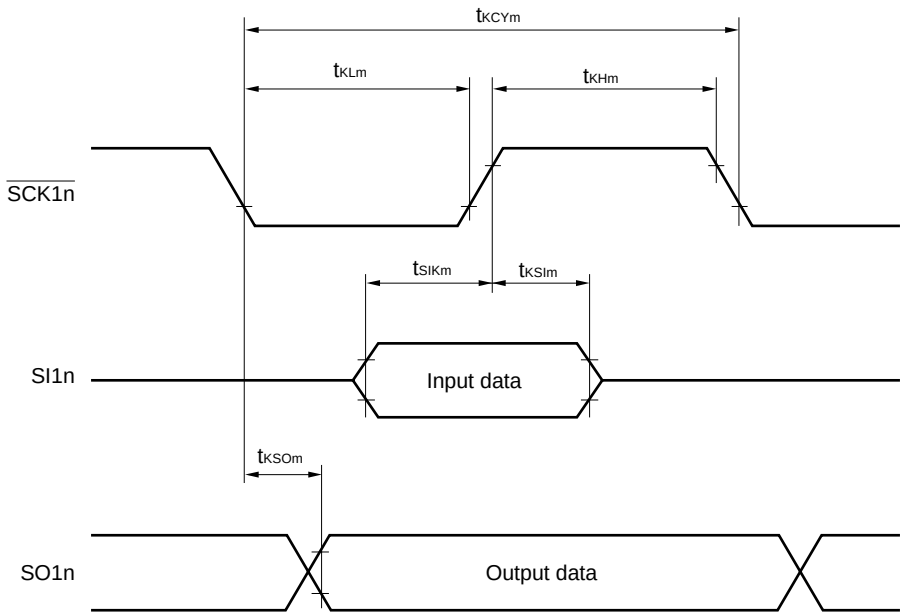
Serial Transfer Timing

3-wire serial I/O mode:



Remark m = 1, 2
n = 0, 1

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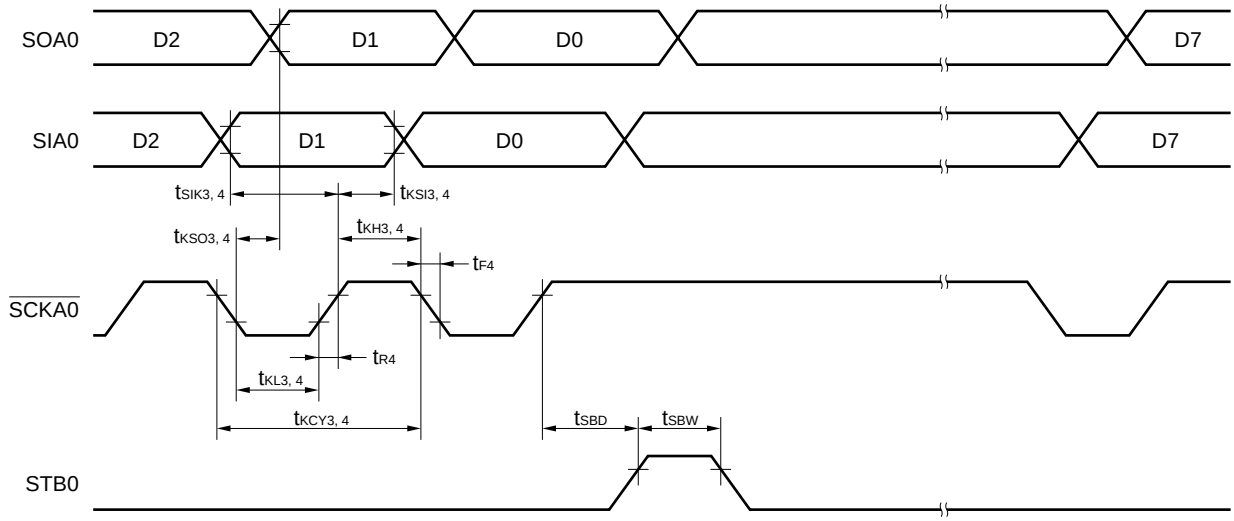
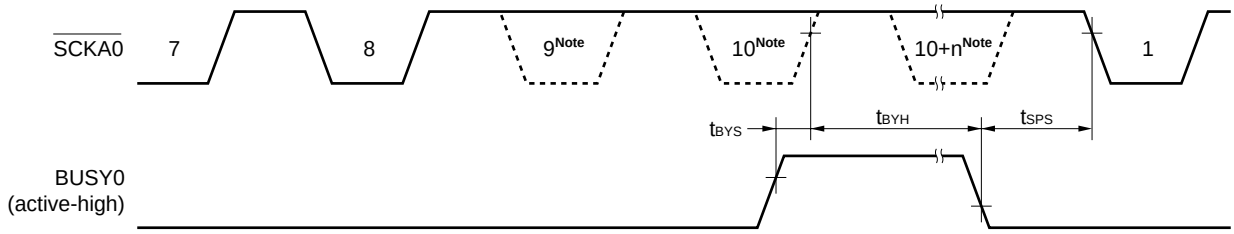
3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

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A/D Converter Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.3 V ≤ AV_{REF} ≤ V_{DD} = EV_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				10	bit
Overall error Note1,2	A_{INL}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ 5.5 V			±0.6	%FSR
		AV_{REF} < 2.7 V			T.B.D.	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	6.6		30	μs
		2.7 V ≤ AV_{REF} ≤ 5.5 V	6.6		30	μs
		AV_{REF} < 2.7 V	11		T.B.D.	μs
Zero-scale error Note1,2	E_{ZS}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ 5.5 V			±0.6	%FSR
		AV_{REF} < 2.7 V			T.B.D.	%FSR
Full-scale error Note1,2	E_{FS}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ 5.5 V			±0.6	%FSR
		AV_{REF} <2.7 V			T.B.D.	%FSR
Integral linearity error Note1	I_{LE}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} ≤ 5.5 V			±4.5	LSB
		AV_{REF} < 2.7 V			T.B.D.	LSB
Differential linearity error Note1	D_{LE}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} ≤ 5.5 V			±2.0	LSB
		AV_{REF} < 2.7 V			T.B.D.	%FSR
Analog input voltage	V_{AIN}		AV_{SS}		AV_{REF}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

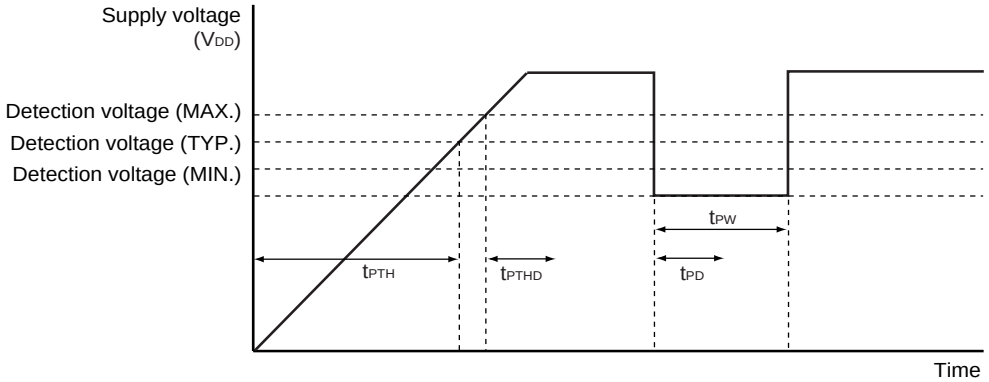
POC Circuit Characteristics (T_A = -40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC}		1.3	1.5	1.7	V
Power supply rise time	t_{PTH}	V_{DD} : V_{POC} →1.8 V (MIN. value of V_{DD})		75	T.B.D	mV/ms
Minimum pulse width	t_{PW}		T.B.D.	50		μs

Notes 1. When voltage rises, time required from detection to reset release

2. When voltage drops, time required from detection to reset occur.

POC Circuit Timing



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LVI Circuit Characteristics (T_A = -40 to +85°C)

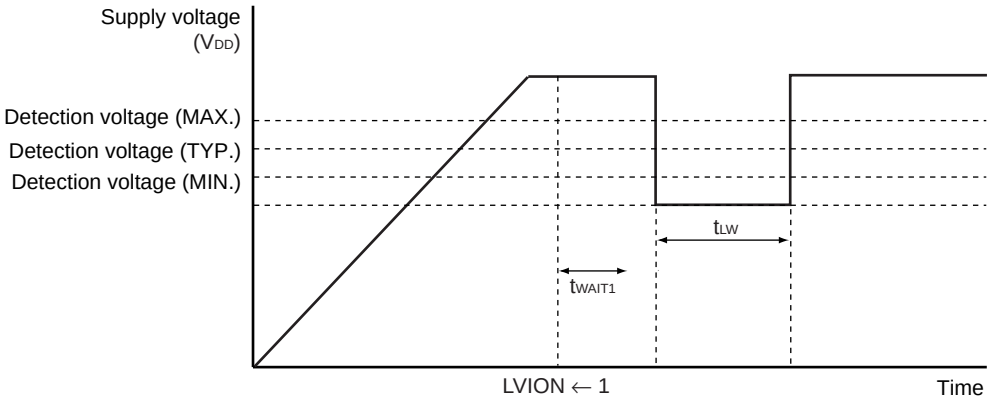
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.10	4.20	4.30	V
		V_{LVI1}		3.95	4.05	4.15	V
		V_{LVI2}		3.81	3.91	4.01	V
		V_{LVI3}		3.66	3.76	3.86	V
		V_{LVI4}		3.51	3.61	3.71	V
		V_{LVI5}		3.37	3.47	3.57	V
		V_{LVI6}		3.22	3.32	3.42	V
		V_{LVI7}		3.07	3.17	3.27	V
		V_{LVI8}		2.93	3.03	3.13	V
		V_{LVI9}		2.78	2.88	2.98	V
		V_{LVI10}		2.63	2.73	2.83	V
		V_{LVI11}		2.49	2.59	2.69	V
		V_{LVI12}		2.34	2.44	2.54	V
		V_{LVI13}		2.19	2.29	2.39	V
		V_{LVI14}		2.05	2.15	2.25	V
		V_{LVI15}		1.90	2.00	2.10	V
	External input pin[Note1]	EXLVI	EXLVI < V_{DD} = EV_{DD}		1.21		V
Minimum pulse width		t_{LW}		T.B.D.	50		μs
Operation stabilization wait time[Note2]		T_{LWAIT1}			10	T.B.D	μs

Note 1. Using EXLVI/P120/INTP0 pin

2. Time required from setting LVION to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1-15

LVI Circuit Timing



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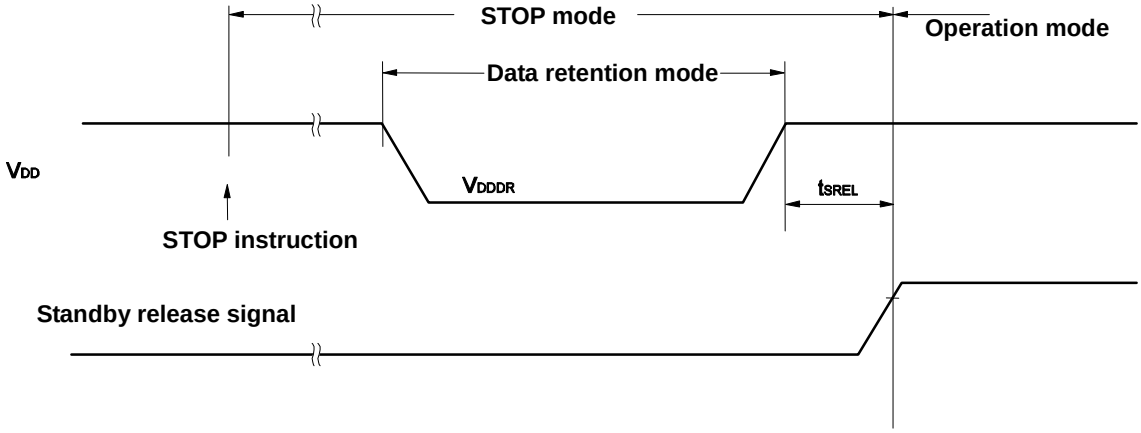
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = -40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.3[Note]		5.5	V

Note Dependence on POC detection voltage. The data is held before POC reset, but is not held after POC reset when voltage drops.



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Flash Memory Programming Characteristics

(T_A = -40 to +85°C, 2.3 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.3 V ≤ AV_{REF} ≤ V_{DD} = EV_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

(1) Basic characteristics

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} supply voltage		I_{DD}	f_{XP} = 10 MHz (TYP.), 20 MHz (MAX.)		4.5	11.0	mA
Erase time[Note1]	Chip unit	T_{eraca}			20	T.B.D	ms
	Sector unit	T_{erasa}			20	T.B.D	ms
Write time		T_{wrwa}			50.	T.B.D.	μs
Number of rewrites per chip		C_{erwr}	1 erase + 1 write after erase = 1 rewrite[Note2]	100			time

Notes 1. The prewrite time before erasure and the erase verify time (writeback time) are not included.

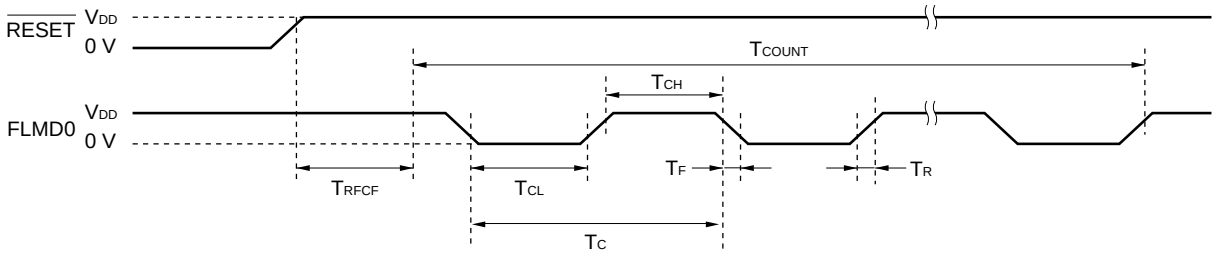
2. When a product is first written after shipment, "erase → write" and "write only" are both taken as one rewrite.

(2) Serial write operation characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time from $\overline{RESET}\uparrow$ to FLMD0 count start	T_{RFCF}		T.B.D	10	T.B.D	ms
Count execution time	T_{COUNT}		T.B.D	10	T.B.D	ms
FLMD0 counter high-/low-level width	T_{CH}/T_{CL}		Tc x 0.45			μs
FLMD0 counter rise/fall time	T_R/T_F		12.5			μs

Remark These values may change after evaluation.

Serial Write Operation



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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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