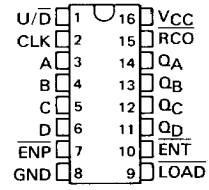
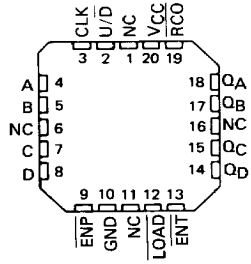
'S168 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS
'LS169B, 'S169 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

SN54S168, SN54LS169B, SN54S169 . . . J OR W PACKAGE
SN74S168, SN74LS169B, SN74S169 . . . D, J OR N PACKAGE
(TOP VIEW)



- **Programmable Look-Ahead Up/Down Binary/Decade Counters**
- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**

SN54S168, SN54LS169B, SN54S169 . . . FK PACKAGE
SN74S168, SN74LS169B, SN74S169 . . . FN PACKAGE
(TOP VIEW)



NC-No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high speed counting applications. The 'S168 is a decade counter and the 'LS169B and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

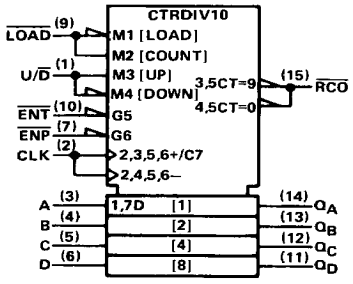
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS169B	35MHz	35MHz	100mW
'S168,'S169	70MHz	55MHz	500mW

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$, $\overline{ENT}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the $\overline{ENP}$ or $\overline{ENT}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

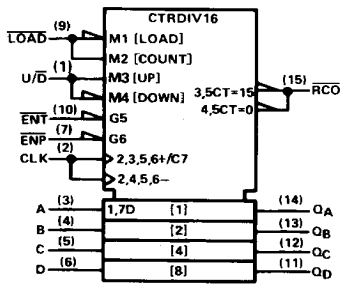
These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, U/$\overline{D}$) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

logic symbols

'S168



'LS169B, 'S169



Pin numbers shown on logic notation are for D, J or N packages.

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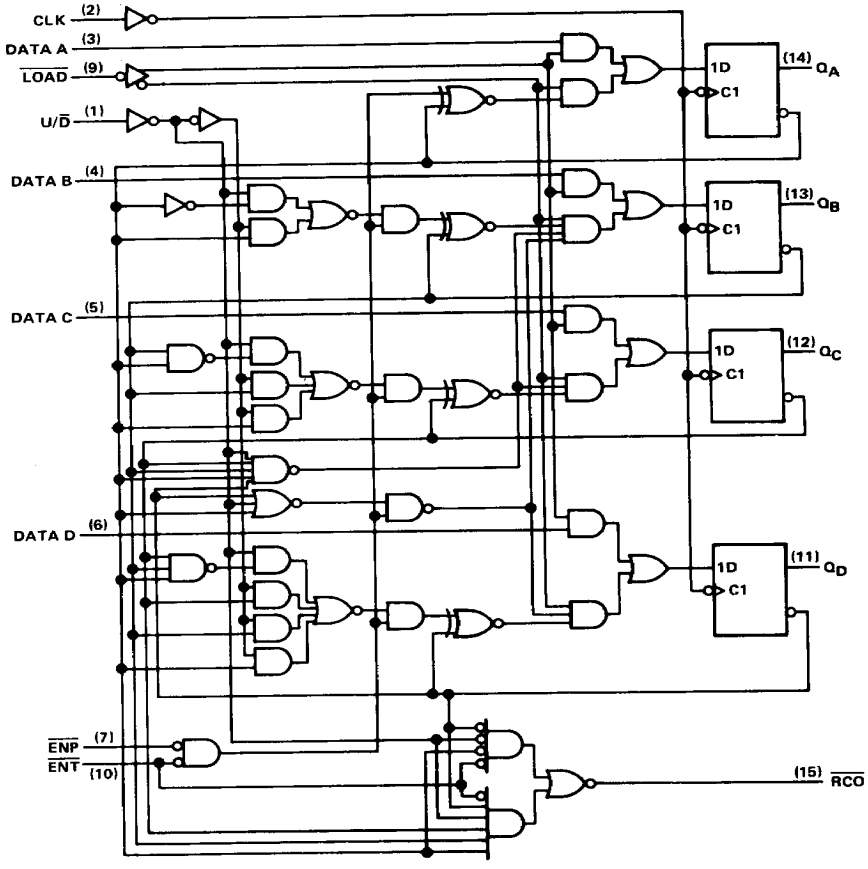
logic diagram

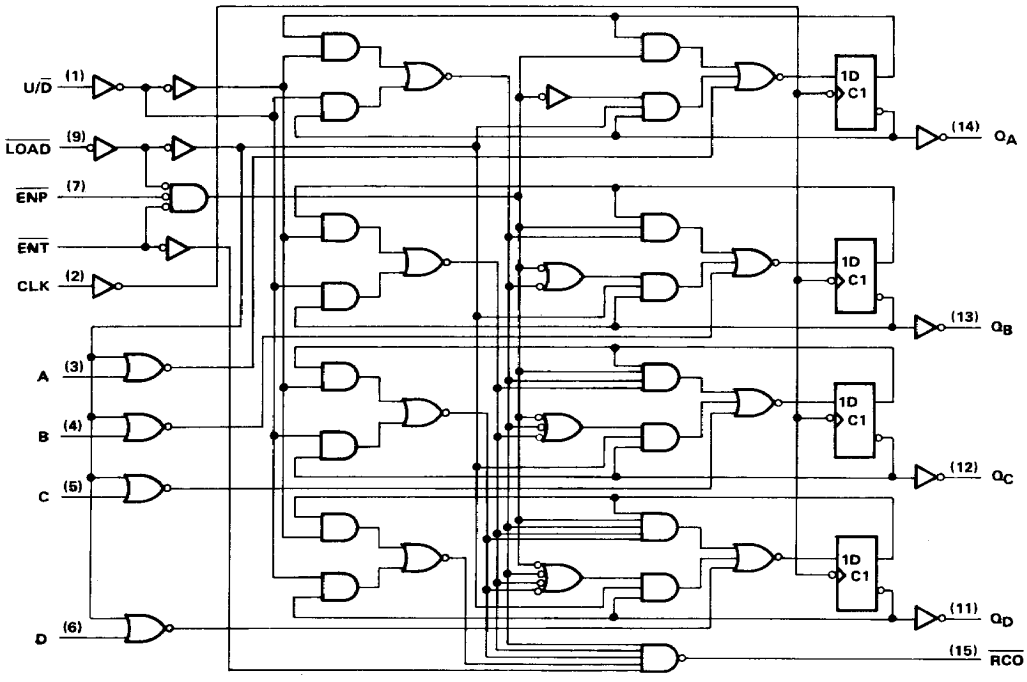
SN54S168, SN74S168 DECADE COUNTERS



Pin numbers shown on logic notation are for D, J or N packages.

logic diagram

SN54LS169B, SN74LS169B BINARY COUNTERS



Pin numbers shown on logic notation are for D, J or N packages.

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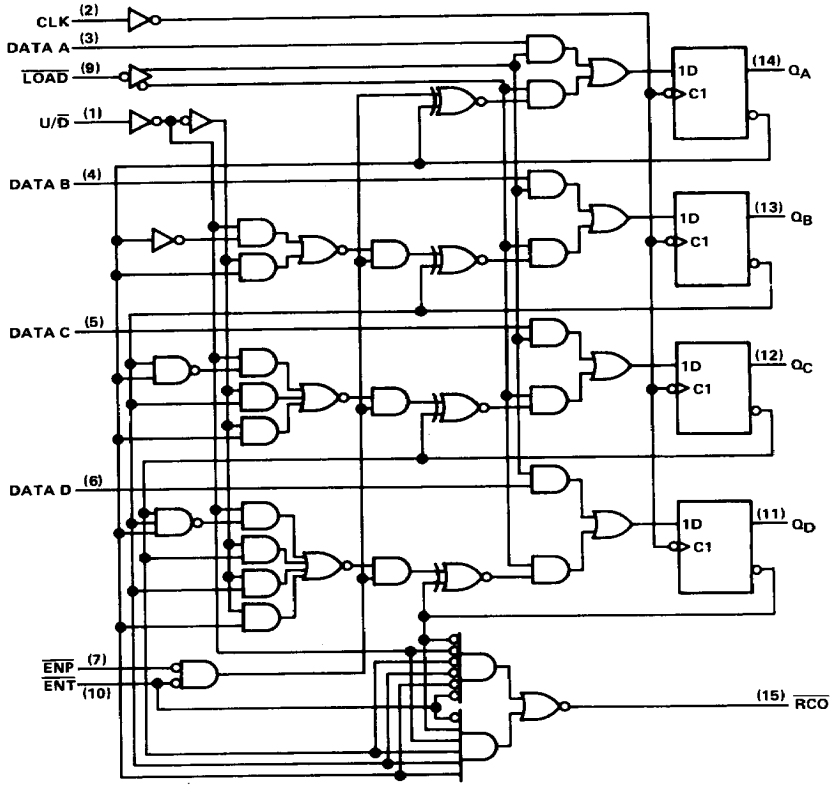
logic diagram

SN54S169, SN74S169 BINARY COUNTERS



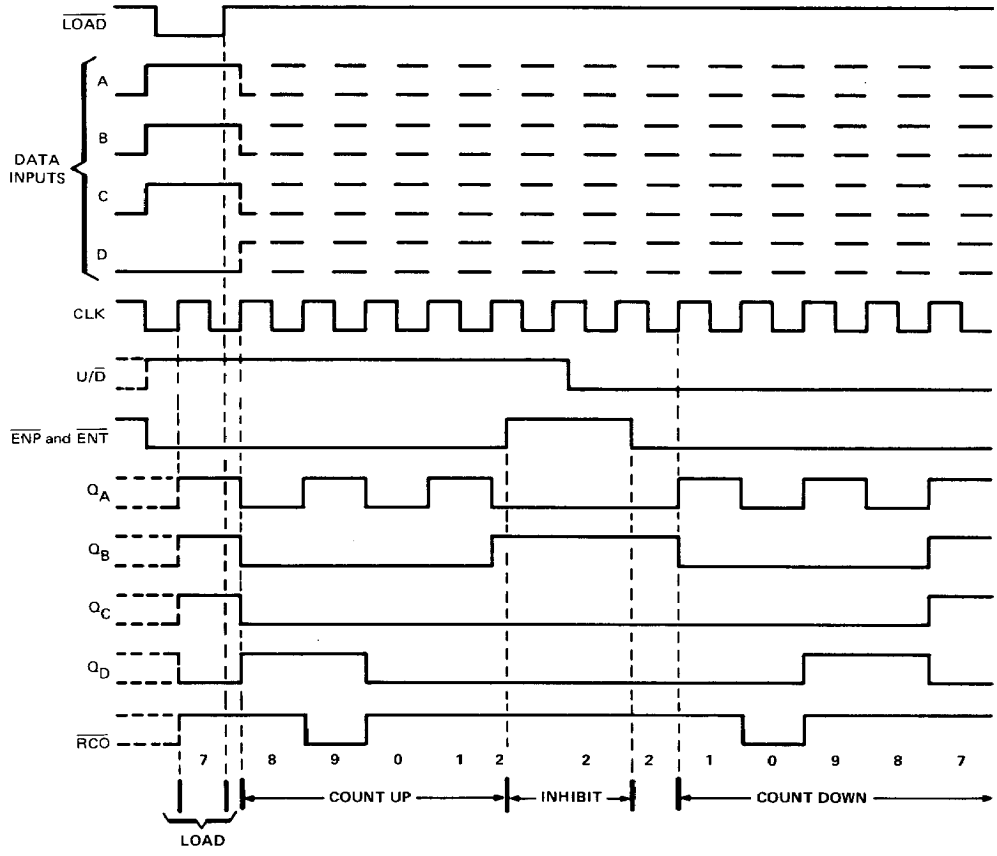
Pin numbers shown on logic notation are for D, J or N packages.

'S168 DECADE COUNTER

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



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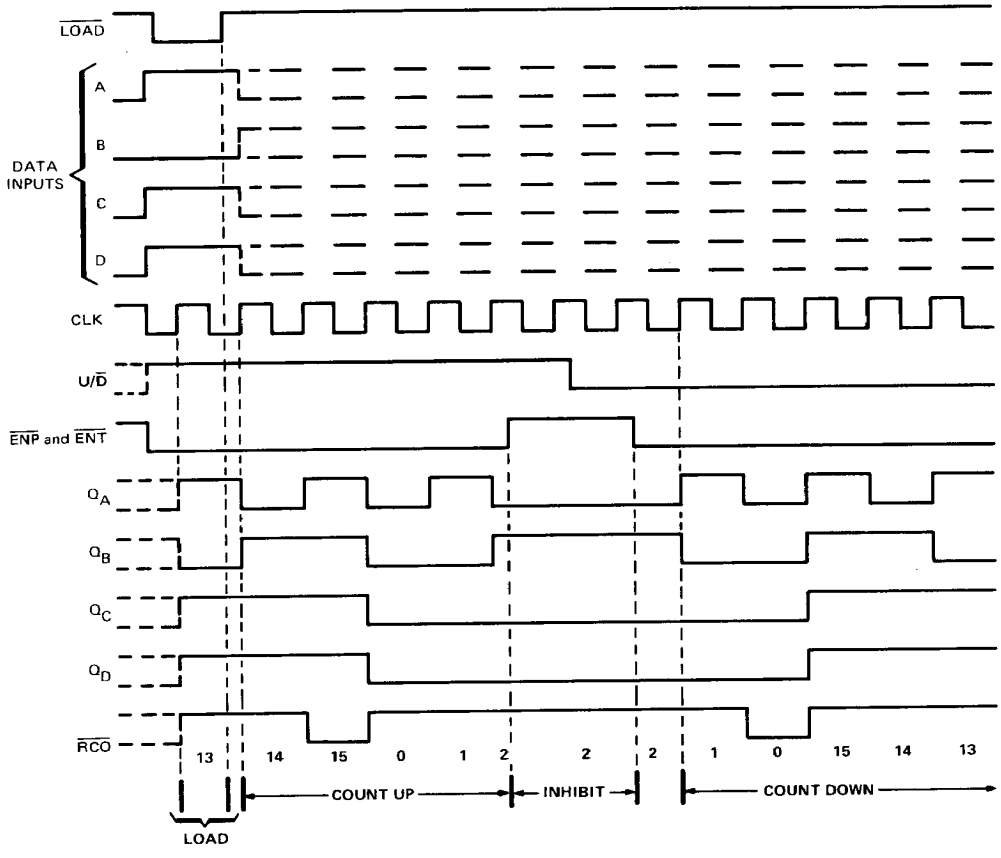
'LS169B, 'S169 BINARY COUNTERS

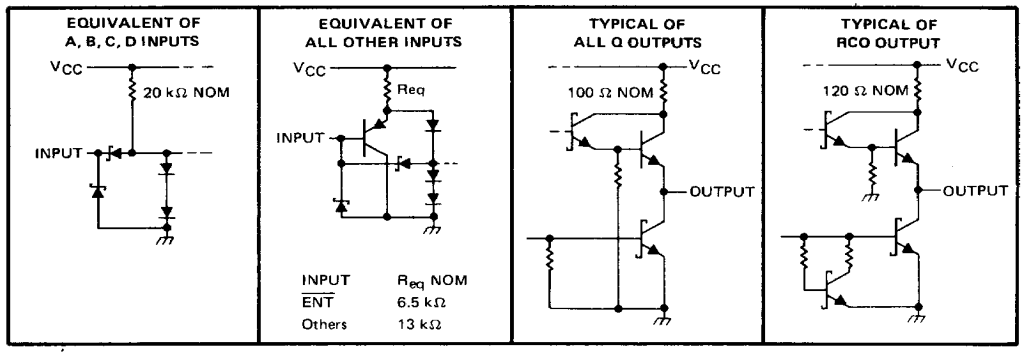
typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS169B . . . . . −55°C to 125°C
SN74LS169B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3 TTL DEVICES

recommended operating conditions

			SN54LS169B			SN74LS169B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level-input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	$\overline{RCO}$			−0.4			−0.4	mA
		Any Q			−1.2			−1.2	mA
I_{OL}	Low-level output current	$\overline{RCO}$			4			8	mA
		Any Q			12			24	mA
f_{clock}	Clock frequency		0			0			MHz
$t_{w(clock)}$	Width of clock pulse (high or low) (see Figure 1)		25			25			ns
t_{su}	Setup time, (see Figure 1)	Data inputs A, B, C, D	30			30			ns
		$\overline{ENP}$ or $\overline{ENT}$	30			30			
		$\overline{Load}$	35			35			
		Up/Down	35			35			
t_h	Hold time at any input with respect to clock (see Figure 1)		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS169B			SN74LS169B			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA					−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	$\overline{RCO}$	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
		Any Q	I_{OH} = −1.2 mA	2.4	3.2		2.4	3.2		
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	$\overline{RCO}$	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
		Any Q	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
			I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = MAX, V_I = 7 V					0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V					20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V	$\overline{U/D}$, $\overline{LOAD}$, $\overline{ENP}$, CLK				−0.2			−0.2	mA
		All other inputs				−0.4			−0.4	
I_{OS}§	V_{CC} = MAX, V_O = 0 V	$\overline{RCO}$		−20		−100	−20		−100	mA
		Any Q		−30		−130	−30		−130	
I_{CC}	V_{CC} = MAX, See Note 2				28	45		28	45	mA

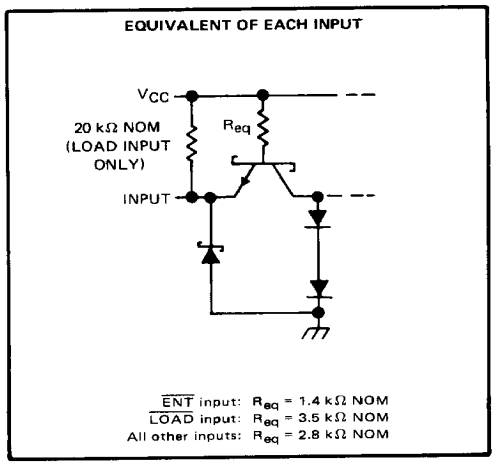
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

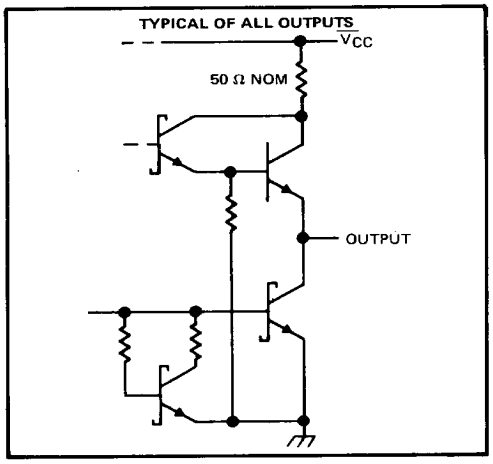
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS169B			UNIT
				MIN	TYP	MAX	
f_{max}				20	35		MHz
t_{PLH}	CLK	$\overline{RCO}$	R_L = 2 kΩ, C_L = 15 pF		26	40	ns
t_{PHL}					17	25	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$			15	25	ns
t_{PHL}					11	20	
t_{PLH}	$U/\overline{D}$	$\overline{RCO}$			23	35	ns
t_{PHL}					15	25	
t_{PLH}	CLK	Any Q	R_L = 667 Ω, C_L = 45 pF		16	25	ns
t_{PHL}					17	25	

¶ Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (15), the ripple carry output will be out of phase.
NOTE 3: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 5) . . . . . 5.5 V
Operating free-air temperature range: SN54S168, SN54S169 (see Note 6) . . . . . −55°C to 125°C
SN74S168, SN74S169 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54S168 SN54S169			SN74S168 SN74S169			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		40	0		40	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low) (see Figure 1)		10			10			ns
Setup time, t_{su} (see Figure 1)	Data inputs A, B, C, D	4			4			ns
	$\overline{ENP}$ or $\overline{ENT}$	14			14			
	$\overline{Load}$	6			6			
	Up/Down	20			20			
Hold time at any input with respect to clock, t_h (see Figure 1)		1			1			ns
Operating free-air temperature, T_A (see Note 6)		−55		125	0		70	°C

NOTES: 4. Voltage values, except interemitter voltage, are with respect to network ground terminal.
5. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs $\overline{ENP}$ and $\overline{ENT}$.
6. An SN54S168 or SN54S169 in the W package operating at free-air temperatures above 91°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 26°C/W.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S168 SN54S169			SN74S168 SN74S169			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current, $\overline{ENT}$	V_{CC} = MAX, V_I = 2.7 V			100			100	µA
	Load		−10		−200	−10		−200	
	Other inputs				50			50	
I_{IL}	Low-level input current, $\overline{ENT}$	V_{CC} = MAX, V_I = 0.5 V			−4			−4	mA
	Other inputs				−2			−2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		100	160		100	160	mA

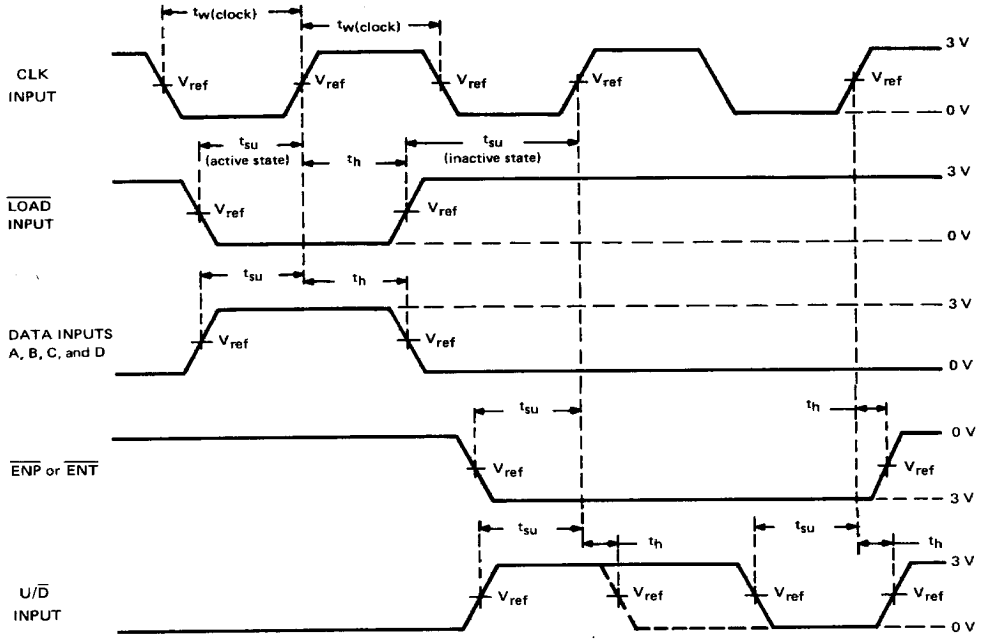
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	UP/DOWN = HIGH			UP/DOWN = LOW			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Figures 2 and 3 and Note 3	40	70		40	55		MHz
t_{PLH}	CLK	$\overline{RCO}$			14	21		14	21	ns
t_{PHL}					20	28		20	28	
t_{PLH}	CLK	Any Q			8	15		8	15	ns
t_{PHL}					11	15		11	15	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$			7.5	11		6	12	ns
t_{PHL}					15	22		15	25	
t_{PLH}◇	U/$\overline{D}$	$\overline{RCO}$			9	15		8	15	ns
t_{PHL}◇					10	15		16	22	

¶f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'S168 or 15 for 'S169), the ripple carry output will be out of phase.
NOTE 3: See General Information Section for load circuits and voltage waveforms.

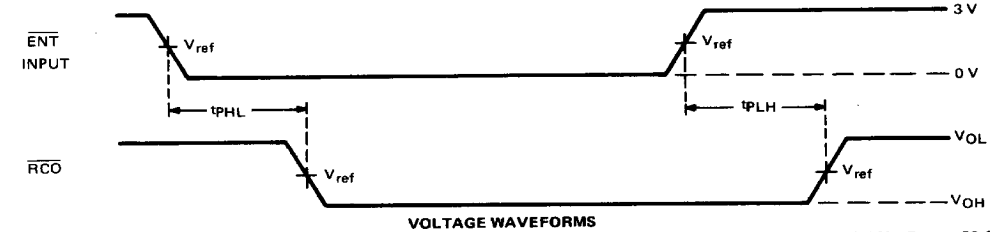
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for 'LS169B, $t_r \leq 15$ ns, $t_f \leq 6$ ns, and for 'S168 and 'S169, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
B. For 'LS169B, $V_{ref} = 1.3$ V; for 'S168 and 'S169, $V_{ref} = 1.5$ V.

FIGURE 1–PULSE WIDTHS, SETUP TIMES, HOLD TIMES



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for 'LS169B, $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S168 and 'S169, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
B. t_{PLH} and t_{PHL} from enable T input to ripple carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'S168, all Q outputs high for 'LS169B and 'S169).
C. For 'LS169B, $V_{ref} = 1.3$ V; for 'S168 and 'S169, $V_{ref} = 1.5$ V.
D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9 for 'S168 or 15 or 'LS169B and 'S169), the ripple carry output will be out of phase.

FIGURE 2–PROPAGATION DELAY TIMES TO CARRY OUTPUT

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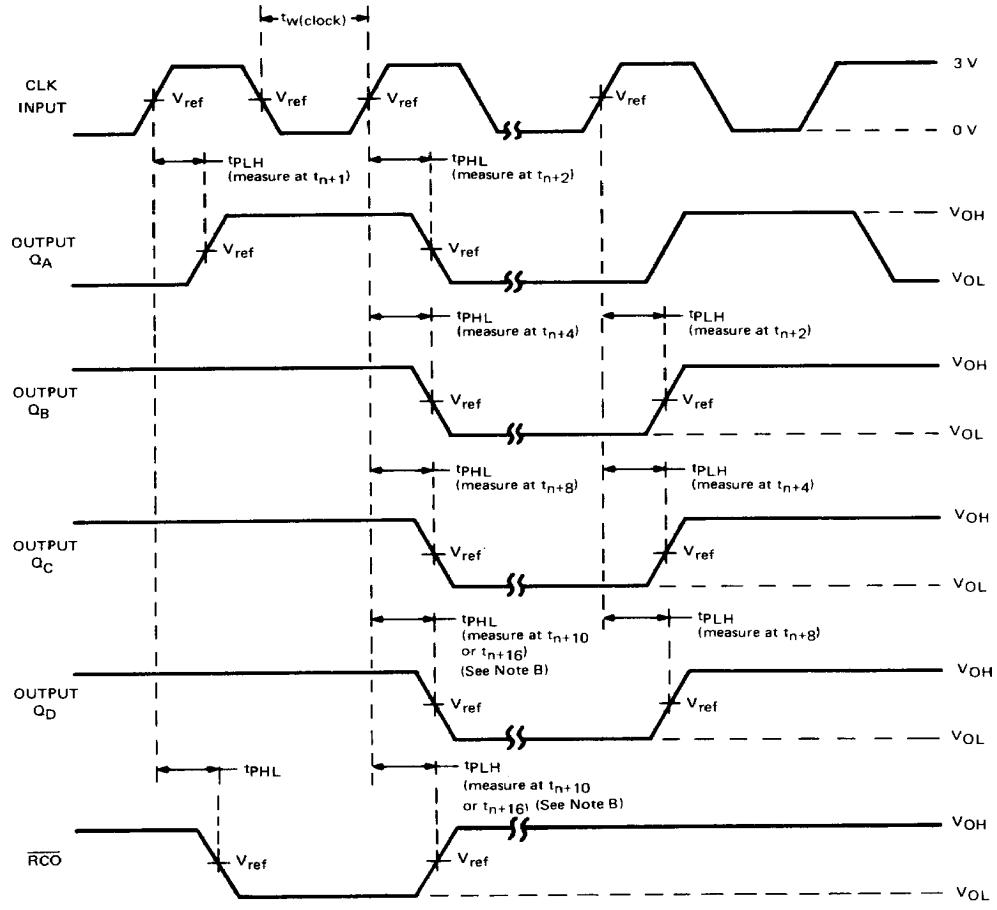
PARAMETER MEASUREMENT INFORMATION



UP-COUNT VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for 'LS169B, $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S168 and 'S169, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{max}.
B. Outputs Q_D and carry are tested at t_{n+10} for the 'S168 and at t_{n+16} for the 'LS169B and 'S169, where t_n is the bit-time when all outputs are low.
C. For 'LS169B, $V_{ref} = 1.3$ V; for 'S168 and 'S169, $V_{ref} = 1.5$ V.

FIGURE 3—PROPAGATION DELAY TIMES FROM CLOCK