Technical Summary

MPC860SAR/D
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MPC860SAR PowerQUICC™ Technical Summary

The MPC860SAR ATM communication controller is an enhanced version of the MPC860 PowerQUICC™ family. In addition to all existing MPC860MH capabilities, the MPC860SAR includes support for asynchronous transfer mode (ATM).

ATM support includes all ATM layer functions and some AAL functions, including segmentation and reassembly (SAR) for AAL5. The 860SAR also supports reception and transmission of raw ATM cells directly to and from memory (also known as AAL0), enabling other AAL protocols to be supported in software.

ATM traffic types directly supported include constant bit rate (CBR) and unspecified bit rate (UBR), with a flexible hardware scheduler enabling implementation of other traffic types in software, such as available bit rate (ABR).

The physical interface can be accomplished with the 860SAR by two methods. The first method is via a standard UTOPIA port. The second method is serially, via any of the serial communication controllers (SCCs) of the 860SAR. In addition to the ATM layer and AAL layer functionality, the 860SAR also provides transmission convergence (TC) sublayer functionality, modeled after the TC mapping of ATM cells into T1/E1 frames. Thus, the 860SAR can receive any serial ATM data stream with byte-aligned synchronization, including T1, E1, and ADSL.

Like the other MPC860 devices, the MPC860SAR can be used in a variety of controller applications, excelling particularly in communications and networking products that provide WAN to LAN functionality. These include routers, ATM line card controllers, residential broadband network interface units, and ADSL modem and infrastructure applications. The integration of the high-performance MPC860 core and ATM SAR in the 860SAR also enables the design of an ATM switch controller in a single part.

The 860SAR integrates two separate processing blocks, common with all MPC860 devices. These are:

- A high-performance core which can be used as a general-purpose processor for application programming
- A RISC engine embedded in the communication processor module (CPM) which is designed to provide the communications protocol processing provided by the MPC860.

In addition to ATM, the 860SAR also supports all of the performance and functionality of the MPC860MH, including multichannel HDLC and Ethernet. This is because the CPM of the 860SAR is based on the CPM of the MPC860MH. This enables the 860SAR to provide protocol processing (HDLC or transparent mode) for time-division multiplexed channels. The only function missing is microcode support for some DSP functions, which has been replaced with the ATM microcode.

1.1 MPC860SAR PowerQUICC Features

The following list summarizes the key features of the MPC860SAR PowerQUICC:

- ATM support
  - Compliant with ATM forum UNI 4.0 specification
  - Cell processing up to 50–70 Mbps at 50-MHz system clock
  - Cell multiplexing/demultiplexing
  - Support of AAL5 and AAL0 protocols on a per-VC basis
    - (AAL0 support enables OAM and software implementation of other protocols)
  - ATM pace control (APC) scheduler, providing:
    - Direct support of constant bit rate (CBR)
    - Direct support of unspecified bit rate (UBR)
    - Control mechanisms enabling software support of available bit rate (ABR)
  - Support for two types of physical interfaces
    - UTOPIA
    - Byte-aligned serial (e.g. T1/E1/ADSL)
  - UTOPIA-mode ATM supports:
    - UTOPIA level 1 master with cell-level handshake
    - Multi-PHY (up to 4 physical layer devices)
    - Connection to 25 Mbps, 51 Mbps, or 155 Mbps framers
    - UTOPIA clock rates of 1:2 or 1:3 system clock rates
  - Serial-mode ATM connection supports:
    - Transmission convergence (TC) function for T1/E1/ADSL lines
    - Cell delineation
    - Cell payload scrambling/descrambling
    - Automatic idle/unassigned cell insertion/stripping
    - Header error control (HEC) generation, checking, and statistics
    - Glueless interface to Motorola CopperGold ADSL transceiver
  - Receive VP/VC connection lookup mechanisms, including:
    - Internal sequential lookup table supporting up to 32 connections
    - Support for up to 64K connections using external memory via address compression or content-addressable memory (CAM)
  - Independent transmit/receive buffer descriptor ring data structures for each connection
  - Interrupt report per channel using exception queue

— Supports 53-byte or up to 64-byte (expanded) ATM cells
— AAL5 segmentation and reassembly (SAR) features for segmentation
  – Segment CPCS_PDU directly from system memory
  – CPCS_PDU padding
  – CRC32 generation
  – Automatic last cell marking (in PTI field of cell header)
  – Automatic CS_UU, CPI, and LENGTH insertion in last cell
— AAL5 segmentation and reassembly (SAR) features for reassembly:
  – Reassembles CPCS_PDU directly into system memory
  – Removes CPCS_PDU padding
  – CRC32 checking
  – CS_UU, CPI, and LENGTH reporting
  – CLP and congestion reporting
  – Interrupts per buffer or per message
  – Error reporting, including CRC, length mismatch, message abort
— AAL0 features for transmit include the following:
  – Transmits user-defined cell from transmit emory buffer
  – Automatic HEC generation
  – Optional CRC10 insertion
— AAL0 features for receive include the following:
  – Copies entire cell into receive memory buffer
  – Provides interrupt per cell
  – Optional CRC10 checking

- Embedded MPC860SAR core with 66 MIPS at 50 MHz (using Dhrystone 2.1)
  — Single issue, 32-bit version of the embedded MPC860SAR core (fully compatible with PowerPC user instruction set architecture definition) with 32- x 32-bit fixed-point registers
    – Performs branch folding and branch prediction with conditional prefetch, but without conditional execution
    – 4-Kbyte data cache and 4-Kbyte instruction cache, each with an MMU
    – Instruction and data caches are two-way, set associative, physical address, 4-word line burst, least-recently used (LRU) replacement algorithm, lockable on-line granularity
    – Memory management units (MMUs) with 32-entry translation lookaside buffers (TLBs) and fully-associative instruction and data TLBs
    – MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 8 protection groups
  — Advanced on-chip emulation debug mode
  — Data bus dynamic bus sizing for 8-, 16-, and 32-bit buses
  — Thirty-two address lines
  — Completely static design (0-MHz to 50-MHz operation)

- System integration unit (SIU)
  - Hardware bus monitor
  - Spurious interrupt monitor
  - Software watchdog
  - Periodic interrupt timer
  - Low-power stop mode
  - Clock synthesizer
  - decrementer defined by the PowerPC Architecture
  - Time base and real-time clock defined by the PowerPC Architecture
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Memory controller (eight banks)
  - Contains complete dynamic random-access memory (DRAM) controller
  - Each bank can be a chip-select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 15 wait states programmable per memory bank
  - Glueless interface to DRAM single in-line memory modules (SIMMs), synchronous DRAM (SDRAM), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), Flash EPROM, etc.
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes, 32 Kbyte to 256 Mbyte
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - Twelve-port pins with interrupt capability
  - Sixteen internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest-priority request
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports two independent PCMCIA sockets
  - Supports eight memory or I/O windows

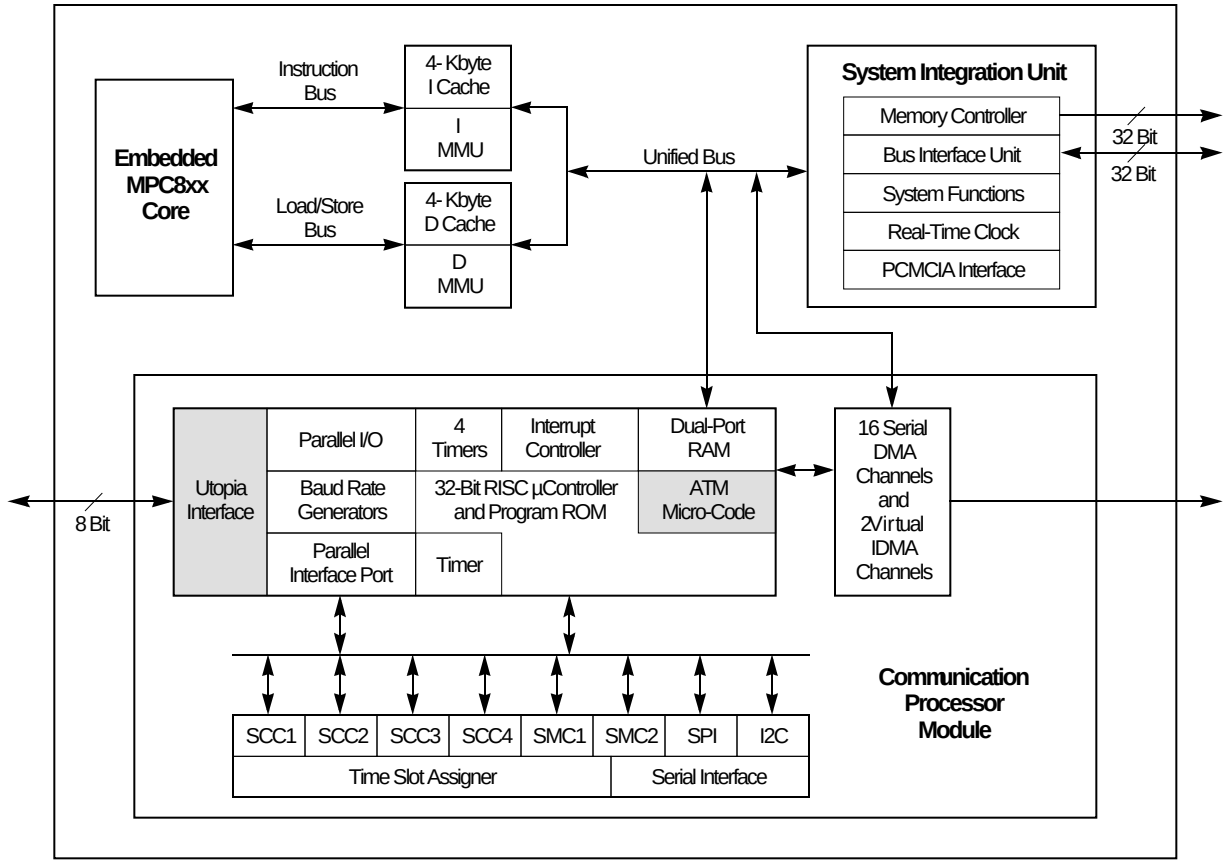
- Communications processor module (CPM)
  - Supports all functionality and performance of MPC860MH
  - RISC controller
  - Communication specific commands (e.g., graceful stop transmit, close receive buffer descriptor, RxBD)
  - Up to 384 buffer descriptors
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 5 Kbytes of dual-port RAM
  - Sixteen serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability
- Four baud rate generators
  - Independent and can be connected to any serial communication controller (SCC) or serial management controller (SMC)
  - Allow changes during operation
  - Autobaud support option
- Four SCCs (serial communication controllers)
  - QMC microcode for protocol processing of 64 time-division multiplexed channels
  - Ethernet/IEEE 802.3 on SCC1–4, supporting full 10-Mbps operation
  - HDLC/SDLC™ (all channels supported at 2 Mbps)
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk™
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- QUICC multichannel controller (QMC) microcode features
  - Up to 64 independent communication channels on a single SCC
  - Arbitrary mapping of 0–31 channels to any of 0–31 TDM time slots
  - Supports either transparent or HDLC protocols for each channel
  - Independent Tx/Rx buffer descriptors and event/interrupt reporting for each channel
  - Running QMC microcode independently on multiple SCCs allows even more channels (for example, 64 at 50-MHz system frequency)
- Two serial management controllers (SMCs)
  - UART
  - Transparent
  - General circuit interface (GCI) controller

  - Can be connected to the time-division-multiplexed (TDM) channels
- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One I^2C® (interprocessor-integrated circuit) port
  - Supports master and slave modes
  - Supports multimaster environment
- Time slot assigner
  - Allows SCCs and SMCs to run in multiplexed and/or nonmultiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, Frame Syncs, clocking
  - Allows dynamic changes
  - Can be internally connected to six serial channels (four SCCs and two SMCs)
- Parallel interface port
  - Centronics™ interface support
  - Supports fast connection between compatible ports on MPC860 or MC68360
- Low-power support
  - Full-on: all units fully powered
  - Doze: core functional units disabled except time base decrementer, PLL, memory controller, real-time clock, and communication processor module in low-power standby
  - Sleep: all units disabled except real-time clock and periodic interrupt timer. PLL is active for fast wake-up.
  - Deep-sleep: all units disabled including PLL, except real-time clock and periodic interrupt timer
  - Low-power stop: to provide lower power dissipation
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports = ≠ < >conditions
  - Each watchpoint can generate a breakpoint internally
- 3.3-V operation with 5-V TTL compatibility
- 357-pin ball grid array (BGA) package

1.2 MPC860SAR Architecture Overview

The 860SAR integrates the embedded MPC860SAR core with high-performance, low-power peripherals, and extends the Motorola data communications family of embedded processors into high-end communications and networking products.

The 860SAR is comprised of three modules that use the 32-bit internal bus—embedded MPC860SAR core, system integration unit (SIU), and the communication processor module (CPM). See Figure 1. for the 860SAR block diagram.



Note: Changes from MPC860 are shaded.

Figure 1. . MPC860SAR PowerQUICC Block Diagram

1.2.1 Embedded MPC860SAR Core

The embedded MPC860SAR core is compliant with the PowerPC user instruction set architecture definition. It has a fully-static design that consists of two functional blocks—the integer block and the load/store block. It executes all integer and load/store operations directly on the hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. Its interface to the internal and external buses is 32 bits. The core uses a two-instruction load/store queue, a four-instruction prefetch queue, and a six-instruction history buffer. The core performs branch folding and branch prediction with conditional prefetch, but without conditional execution. The core can operate on 32-bit external operands with one bus cycle.

The integer block supports 32- x 32-bit fixed-point general-purpose registers. It can execute one integer instruction on each clock cycle. Each element in the integer block is only clocked when valid data is present in the data queue ready for operation, which assures that the power consumption of the device is held to the absolute minimum required to perform an operation.

The embedded MPC860SAR core is integrated with the memory management units (MMUs) and 4-Kbyte instruction and data caches. The MMUs provide a 32-entry, fully-associative instruction and data TLB, with multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Mbytes. It supports 16 virtual

address spaces with eight protection groups. Three special registers are available as scratch registers to support software table walk and update.

The instruction cache is 4 Kbytes, two-way, set associative with physical addressing. It allows single-cycle access on hit with no added latency for miss. It has four words per line and supports burst linefill using a least recently used (LRU) replacement algorithm. The cache can be locked on a line basis for application-critical routines. The data cache is 4 Kbytes, two-way, set associative with physical addressing. It allows single-cycle access on hit with one added clock latency for miss. It has four words per line and supports burst linefill using an LRU replacement algorithm. The cache can be locked on a line basis for application-critical routines and can be programmed to support copy-back or write-through via the MMU. The inhibit mode can be programmed per MMU page.

The embedded MPC860SAR core with its instruction and data caches delivers approximately 66 MIPS at 50 MHz (using Dhrystone 2.1) based on the assumption that it is issuing one instruction per cycle with a cache hit rate of 94%.

The embedded MPC860SAR core contains a much improved debug interface that provides superior debug capabilities without causing any degradation in the speed of operation. This interface supports six watchpoint pins that are used to detect software events. Internally it has eight comparators, four of which operate on the effective address on the address bus. The remaining four comparators are split, with two comparators operating on the effective address on the data bus and two comparators operating on the data on the data bus. The embedded MPC860SAR core can compare using =, ≠, <, > conditions to generate watchpoints. Each watchpoint can then generate a breakpoint that can be programmed to trigger in a programmable number of events.

1.2.2 System Interface Unit (SIU)

The SIU on the MPC860 PowerQUICC family integrates general-purpose features useful in almost any 32-bit processor system, enhancing the performance provided by the system integration module (SIM) on the MC68360 QUICC device.

Although the embedded MPC860SAR core is always a 32-bit device internally, it may be configured to operate with an 8-, 16- or 32-bit data bus. Regardless of the choice of the system bus size, dynamic bus sizing is supported, which allows 8-, 16-, and 32-bit peripherals and memory to coexist in the 32-bit system bus. The SIU also provides power management functions, reset control, decrementer, time base and real-time clock.

The memory controller supports up to eight memory banks with glueless interfaces to DRAM, SRAM, SSRAM, EPROM, Flash EPROM, SRDRAM, EDO and other peripherals with two-clock access to external SRAM and bursting support. It provides variable block sizes from 32 Kbytes to 256 Mbytes. The memory controller provides 0 to 15 wait states for each bank of memory and can use address type matching to qualify each memory bank access. It provides four byte-enable signals for varying width devices, one output enable signal, and one boot chip-select available at reset.

The DRAM interface supports 8-, 16-, and 32-bit ports. Memory banks can be defined in depths of 256 Kbytes, 512 Kbytes, 1 Mbyte, 2 Mbytes, 4 Mbytes, 8 Mbytes, 16 Mbytes, 32 Mbytes, or 64 Mbytes for all port sizes. In addition, the memory depth can be defined as 64 Kbytes and 128 Kbytes for 8-bit memory or 128 Mbytes and 256 Mbytes for 32-bit memory. The DRAM controller supports page mode access for successive transfers within bursts. The MPC860 supports a glueless interface to one bank of DRAM while external buffers are required for additional memory banks. The refresh unit provides $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, a programmable refresh timer, refresh active during external reset, disable refresh modes, and stacking for a maximum of seven refresh cycles. The DRAM interface uses a programmable state machine to support almost any memory interface.

The PCMCIA interface is a master (socket) controller and is compliant with release 2.1. The interface supports up to two independent PCMCIA sockets requiring only external transceivers/buffers. It provides eight memory or I/O windows that can be allocated to the socket. If only one PCMCIA port is being used, the unused PCMCIA port may be used as general-purpose input with interrupt capability.

1.2.3 Communications Processor Module (CPM)

The MPC860 PowerQUICC family, like the earlier generation MC68360 QUICC, implements a dual-processor architecture. This dual-processor architecture provides both a high-performance, general-purpose processor for application programming use as well as a special-purpose communication processor (CPM) uniquely designed for communications needs.

The CPM contains features that allow the PowerQUICC to excel in communications and networking products. These features may be divided into three subgroups:

- Communications processor (CP)
- Sixteen independent serial DMA (SDMA) controllers
- Four general-purpose timers

The communication processor module provides the communication features of the MPC860 PowerQUICC family. It includes a RISC processor, four serial communication controllers (SCC), four serial management controllers (SMC), one serial peripheral interface (SPI), one I^2C Interface, 5 Kbytes of dual-port RAM, an interrupt controller, a time-slot assigner, three parallel ports, a parallel interface port, four independent baud rate generators, and sixteen serial DMA channels to support the SCCs, SMCs, SPI, and I^2C.

The SDMAs provide two channels of general-purpose DMA capability for each communications channel. They offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic.

The four general-purpose timers on the CPM are identical to the timers found on the MC68360 and still support the internal cascading of two timers to form a 32-bit timer.

The PowerQUICC family maintains the best features of the MC68360 QUICC' while making changes required to provide for the increased flexibility, integration, and performance requested by customers demanding the performance of the PowerPC architecture. Because the CPM architectural approach remains intact between the PowerQUICC family and the MC68360 QUICC, an MC68360 QUICC user can easily become familiar with the PowerQUICC.

Additionally, like the MC68MH360 QUICC32 and the MPC860MH, the 860SAR supports the QMC microcode, enabling it to provide protocol processing for multiple time-division-multiplexed channels over a single SCC.

1.3 Power Management

The MPC860 PowerQUICC family supports a wide range of power management features including full-on, doze, sleep, deep-sleep, and low-power stop. In full-on mode, the MPC860 processor is fully powered with all internal units operating at the full speed of the processor. There is a gear mode determined by a clock divider that allows the operating system to reduce the operational frequency of the processor.

Doze mode disables core functional units except the time base, decrementer, PLL, memory controller, real-time clock, and places the communication processor module in low-power standby mode. Sleep mode disables everything except the real-time clock and periodic interrupt timer, thus leaving the PLL active for quick wake-up. The deep-sleep mode then disables the PLL for lower power, but slower wake-up.

Low-power stop disables all logic in the processor except the minimum logic required to restart the device, and provides the lowest power consumption but requires the longest wake-up time.

1.4 ATM Support

Support for asynchronous transfer mode (ATM) has been integrated into the 860SAR by inclusion of ATM microcode in the ROM of the CPM and addition of a UTOPIA port, multiplexed onto parallel port D. The serial communications signals that existed on port D for the standard MPC860 have been multiplexed onto port A and port C, similarly to the MC68360.

ATM processing is performed in the CPM RISC by microcoded routines. The ATM performance of the 860SAR will vary depending on the mode of the physical interface (serial or UTOPIA) and the protocol processing performed (AAL0 or AAL5).

The UTOPIA port of the 860SAR is 8 bits wide. Handshaking is performed on a cell basis. The UTOPIA port has no FIFO; the UTOPIA PHY will contain internal storage so that cells (typically only one cell) will be held there until the 860SAR is ready to process it, upon which the cell will be transferred all at once. Two bits of 'PHY address' are also included in the UTOPIA port to enable implementation of multi-PHY UTOPIA for up to 4 PHY devices. If multi-PHY UTOPIA is implemented, external logic will have to decode these signals in order to gate the transmit and receive cell handshaking signals to and from the appropriate PHY devices.

The receive channel of the 860SAR has a higher priority than the transmit channel, enabling the (maximum) 70 Mbps ATM bandwidth of the 860SAR to be dynamically switched between the receive and transmit channels. Thus the 860SAR can be connected to full-duplex high-speed channels (e.g. 51 Mbps) without loss of cells; the transmit bandwidth will merely drop when the receive port is operating at maximum speed. For connection to higher-speed UTOPIA connections (e.g. 155 Mbps), an external FIFO will be required, and the time-average of the bandwidth processed by the 860SAR must be less than 70 Mbps.

Serial-mode ATM can be performed over any of the SCCs for a byte-aligned serial stream only. This means that an indication of a byte boundary in the serial stream must be given to the 860SAR SCC. With frame-based transmission (e.g. T1, E1, or ADSL), ATM cells are mapped into n-byte frames at byte boundaries, and a frame-sync signal is always provided; thus signals in a frame-based format can be gluelessly connected to the MPC860 via either of the TDM interfaces (TDM_a or TDM_b). Serial streams that have no indication of byte boundaries can only be supported if external logic provides a byte-boundary sync.

The ATM pace control (APC) transmit scheduler is also implemented in microcode. However, a CPM timer (Timer 4) is also dedicated to generate the clock which is counted by the APC. The speed of this timer defines the granularity of the control of the APC.

The receive connection table can be implemented either in internal memory or external memory, or with a combination. Internal memory can be used to support up to 32 connections. Additional connections can be supported with external memory using address compression, with some loss of performance. It is possible to use a combination of internal connections and external connections with address compression, enabling the user to minimize performance loss by keeping the highest-traffic connections in internal memory. Finally, features also exist to enable use of a content-addressable memory (CAM), to support a large number of connections in external memory with no performance loss.

Buffer descriptors and buffers for the ATM virtual circuit connections (VCCs) can be contained in internal or external memory, but will typically be contained in external memory. The ATM microcode uses bursting DMA to maximize the performance of the ATM connections.

Support for expanded cells (up to 64 bytes) is also provided. While the standard size of cells on the ATM network is 53 bytes, support for larger cells enables the user to tag additional information onto a cell. An example use of this tag information is insertion of a card address when implementing ATM over a shared backplane in an ATM switch.

1.4.1 QMC Microcode

The standard MPC860 can handle one logical channel performing the protocol framework for each of its serial channels. This logical channel can be used in time-division-multiplexed interfaces. In contrast, the QMC microcode emulates up to 64 serial controllers that can operate in either HDLC mode or transparent mode within one single SCC.

See the documentation for the MPC860MH for more details on the features and operation of the QMC microcode.

1.5 Software Compatibility Issues

The following list summarizes the major software differences between the MC68360 QUICC and the MPC860 PowerQUICC family:

- Since the MPC860 PowerQUICC family uses an embedded MPC860SAR core, code written for the MC68360 must be recompiled for the PowerPC instruction set. Code that accesses the MC68360 peripherals requires only minor modifications for use with the MPC860. Although the functions performed by the PowerQUICC SIU are similar to those performed by the QUICC SIM, the initialization sequence for the SIU is different and, therefore, code that accesses the SIU must be rewritten. Many developers of 68K compilers now provide compilers which also support the PowerPC architecture.
- When porting code from the MC68360 CPM to the MPC860 CPM, the software writer will find new options for hardware breakpoint on CPU commands, address, and serial request that are useful for software debugging. Support for single-step operation with all the registers of the CPM visible makes software development for the CPM on the MPC860 processor even simpler.

1.6 PowerQUICC Glueless System Design

A fundamental design goal of the MPC860 PowerQUICC family is the ease of interface to other system components. Figure 2 shows a system configuration that offers one EPROM, one Flash EPROM, and

supports two DRAM SIMMs. Depending on the capacitance on the system bus, external buffers may be required. From a logic standpoint, however, a glueless system is maintained.

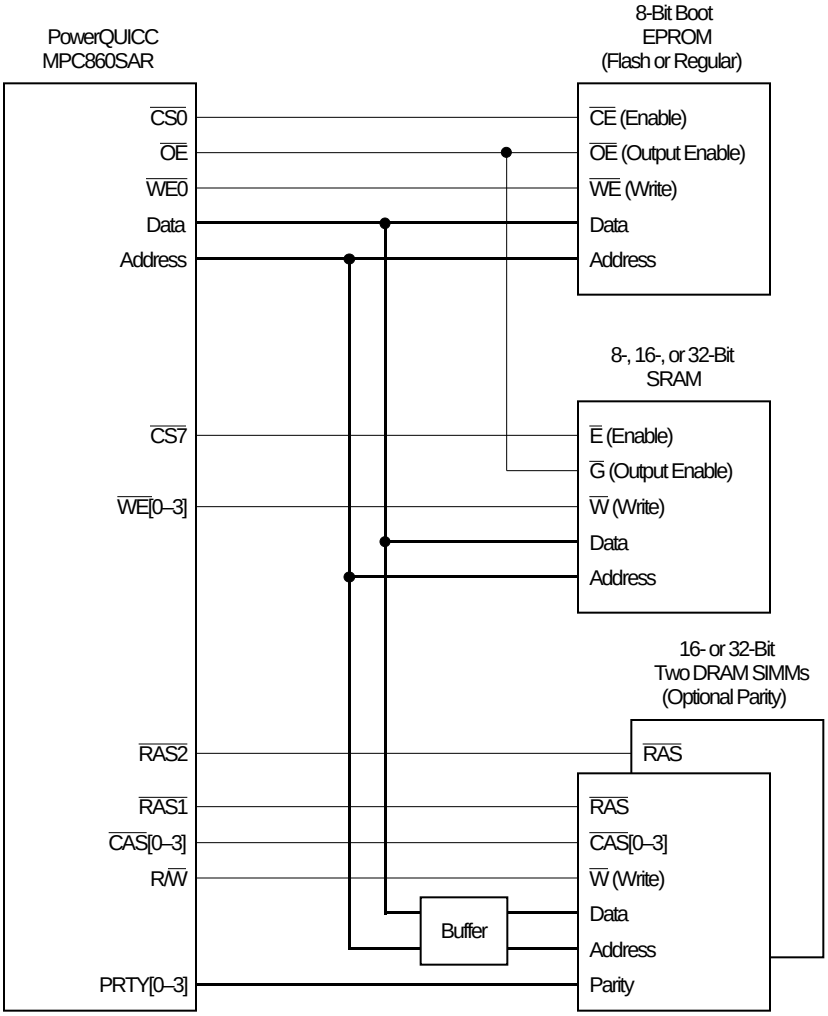


Figure 2. . MPC860 System Configuration

Figure 3 shows the glueless connection of the 860SAR serial channels and UTOPIA interface to physical layer framers and transceivers.

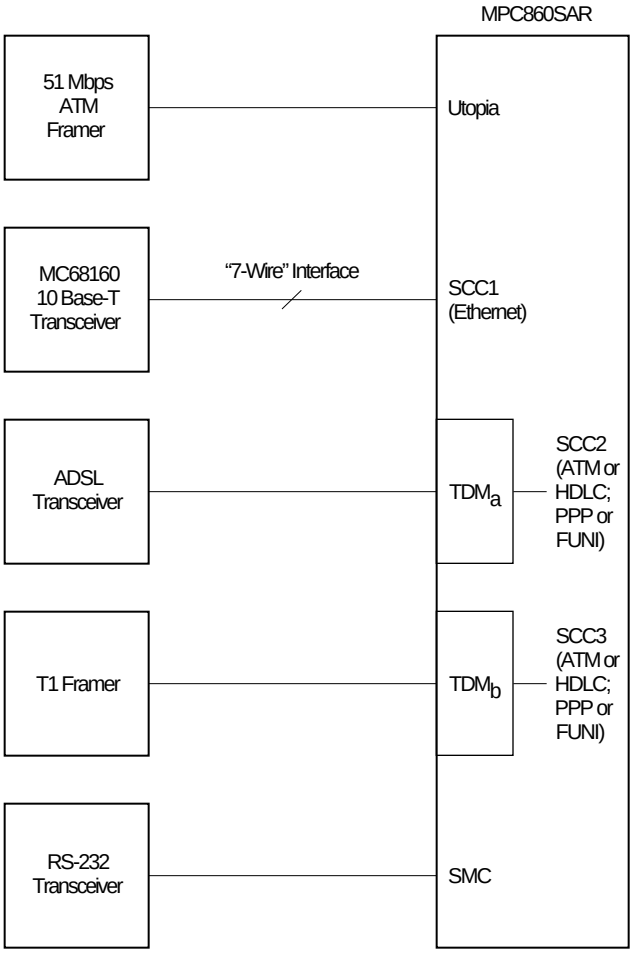


Figure 3. . MPC860SAR Serial Configuration

1.7 Ordering Information

Table 1. identifies the packages and operating frequencies available for the 860SAR.

Table 1. . MPC860SAR Package/Frequency Availability

Package Type	Frequency (MHz)	Temperature	Order Number
Ball grid array (ZP suffix)	25	0°C to 70°C	MPC860SRZP25
	40	0°C to 70°C	MPC860SRZP40
	50	0°C to 70°C	MPC860SRZP50
Ball grid array (CZP suffix)	TBD	–40°C to 85°C	TBD

Ordering Information

The documents listed in Table 2. can be used as reference for the 860SAR. These documents can be obtained from the Literature Distribution Centers at the addresses listed on the back page. Visit the website for more information

Table 2. . Documentation

Document Title	Order Number	Description
QMC Supplement to MC68360 and MPC860 User's Manuals	QMCSUPPLEMENT/AD	Supports MC68MH360, MPC860MH and MPC860DH devices
MPC860 User's Manual	MPC860UM/AD	Detailed information for design

Table 3. Document Revision History

Revision	Date	Changes
0.1	12/2001	Revised for new template, added this revision table, removed MAC (multiply and accumulate references).

HOW TO REACH US:

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