RAIL TO RAIL FET INPUT OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The ALD 1704 is a CMOS monolithic operational amplifier with FET input that has rail to rail input and output voltage ranges. The input voltage range and output voltage range are very close to the positive and negative power supply voltages. Typically the input voltage can be at the positive power supply voltage (V_{DD}) or the negative power supply voltage (V_{SS}). The output voltage swings to within 60 mV of either positive or negative power supply voltages at rated load.

This device is designed as an alternative to the popular J FET input operational amplifiers in applications where lower operating voltages, such as 9 V battery or ±3.25 V to ±6 V power supplies are being used. It offers high slew rate of 5V/µs at low operating power of 30 mW. Since the ALD 1704 is designed and manufactured with Advanced Linear Devices' standard enhanced ACMOS silicon gate CMOS process, it also offers low unit cost and exceptional reliability.

The rail to rail input and output feature of the ALD 1704 allows a lower operating supply voltage for a given signal voltage range and allows numerous analog serial stages to be implemented without losing operating voltage margin. The output stage is designed to drive up to 10 mA into 400 pF capacitive and 1.5 KΩ resistive loads. Short circuit protection to either ground or the power supply rails is at approximately 15 mA clamp current. Due to complementary output stage design, the output can both source and sink 10 mA into a load with symmetrical drive and is ideally suited for applications where push-pull voltage drive is desired.

The offset voltage is trimmed on-chip to eliminate the need for external nulling in many applications. For precision applications, the output is designed to settle to 0.1% in 2 µs. For large signal buffer applications, the operational amplifier can function as an ultra-high input impedance voltage follower /buffer that allows input (and output) voltage swings from positive to negative supply voltages. This feature is intended to greatly simplify systems design and permit elimination of higher voltage power supplies in many applications.

ORDERING INFORMATION

	Operating Temperature Range		
	-55°C to +125°C	0°C to +70°C	0°C to +70°C
+25°C V_{OS} Max (mV)	8-Pin CERDIP Package	8-Pin Small Outline Package (SOIC)	8-Pin Plastic Dip Package
0.9	ALD 1704A DA		ALD 1704A PA
2.0	ALD 1704B DA		ALD 1704B PA
4.5	ALD 1704 DA	ALD 1704SA	ALD 1704 PA
10.0			ALD 1704G PA
10.0			ALD 1704 Z (Dice)

1030 West Maude Avenue, Bldg. 501, Sunnyvale, CA 94086-2810
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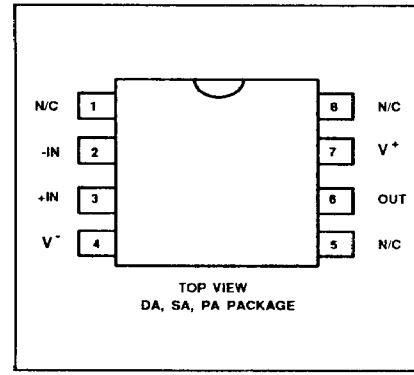
PIN CONFIGURATION



TOP VIEW
DA, SA, PA PACKAGE

FEATURES

- 5.0 V/µs slew rate
- Rail to rail input and output voltage ranges
- High capacitive load capability – up to 400 pF
- No frequency compensation required – unity gain stable
- Extremely low input bias currents – 1.0 pA typical (20 pA max.)
- Ideal for high source impedance applications
- High voltage gain – typically 150 V/mV
- Output short circuit protected
- Unity gain bandwidth of 2.1 MHz

APPLICATIONS

- Voltage amplifier
- Voltage follower/buffer
- Charge integrator
- Photodiode amplifier
- Data acquisition systems
- High performance portable instruments
- Signal conditioning circuits
- Low leakage amplifiers
- Active filters
- Sample/Hold amplifier
- Picoammeter
- Current to voltage converter
- Coaxial cable driver
- Capacitive sensor amplifier
- Piezoelectric transducer amplifier

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}		12V
Differential input voltage range		-0.3V to V_{DD} +0.3V
Power dissipation		600 mW
Operating temperature range	1704XPA/1704XSA	0°C to +70°C
	1704XDA	-55°C to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature,10 seconds		+300°C

DC AND OPERATING ELECTRICAL CHARACTERISTICS
T_A = 25°C V_S = ±5.0V unless otherwise specified

		1704A			1704B			1704			1704G				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Supply Voltage	V_S	±3.25		±6.0	±3.25		±6.0	±3.25		±6.0	±3.25		±6.0	V	Dual Supply
	V_{DD}	6.5		12.0	6.5		12.0	6.5		12.0	6.5		12.0	V	Single Supply
Input Offset Voltage	V_{OS}			0.9			2.0			4.5			10.0	mV	R_S≤100KΩ
				1.7			2.8			5.3			11.0	mV	0°C≤T_A≤+70°C
Input Offset Current	I_{OS}		1.0	15		1.0	15		1.0	15		1.0	25	pA	T_A=25°C
				240			240			240			240	pA	0°C≤T_A≤+70°C
Input Bias Current	I_B		1.0	20		1.0	20		1.0	20		1.0	30	pA	T_A=25°C
				300			300			300			300	pA	0°C≤T_A≤+70°C
Input Voltage Range	V_{IR}	-5.0		+5.0	-5.0		+5.0	-5.0		+5.0		±5.0		V	
Input Resistance	R_{IN}		10^{12}			10^{12}			10^{12}			10^{12}		Ω	
Input Offset Voltage Drift	TCV_{OS}		5			5			5			7		µV/°C	R_S≤100KΩ
Power Supply Rejection Ratio	PSRR	70	80		65	80		65	80		60	80		dB	R_S≤100KΩ
															0°C≤T_A≤+70°C
Common Mode Rejection Ratio	CMRR	70	83		65	83		65	83		60	83		dB	R_S≤100KΩ
															0°C≤T_A≤+70°C
Large Signal Voltage Gain	A_V	50	150		50	150		50	150		32	150		V/mV	R_L=10KΩ
			150			150			150			150		V/mV	No Load
		40			40			40			20			V/mV	0°C≤T_A≤+70°C
Output Voltage Range	V_O low		-4.96	-4.90		-4.96	-4.90		-4.96	-4.90		-4.96	-4.90	V	R_L=10KΩ
	V_O high	4.90	4.95		4.90	4.95		4.90	4.95		4.90	4.95			0°C≤T_A≤+70°C
Output Short Circuit Current	I_{SC}		15			15			15			15		mA	
Supply Current	I_S		3.0	4.5		3.0	4.5		3.0	4.5		3.0	5.0	mA	V_{IN} = 0V No Load
Power Dissipation	P_D		30	45		30	45		30	45		30	50	mW	V_s = ±5.0 No Load
Input Capacitance	C_{IN}		1			1			1			1		pF	
Bandwidth	B_W		2.1			2.1			2.1			2.1		MHz	
Slew Rate	S_R		5.0			5.0			5.0			5.0		V/µS	A_V=+1 R_L=2.0KΩ
Rise time	t_r		0.1			0.1			0.1			0.1		µS	R_L=2.0KΩ
Overshoot Factor			15			15			15			15		%	R_L=2.0KΩ C_L=100pF

Design & Operating Notes:

1. The ALD 1704 CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. The ALD 1704 is internally compensated for unity gain stability using a novel scheme that produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency. A unity gain buffer using the ALD 1704 will typically drive 400 pF of external load capacitance without stability problems. In the inverting unity gain configuration, it can drive up to 800pF of load capacitance. Compared to other CMOS operational amplifiers, the ALD 1704 has shown itself to be more resistant to parasitic oscillations.

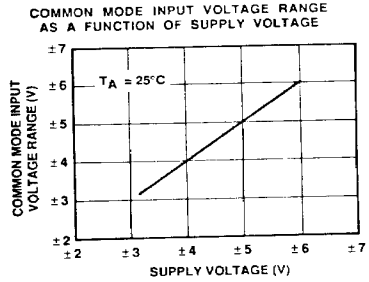
2. The ALD 1704 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail to rail input common mode voltage range. This means that with the ranges of common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5 V above the negative supply voltage. Since offset voltage trimming on the 1704 is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain larger than 2 (10V operation), where the common mode voltage does not make excursions below this switching point. The user should however, be aware that this switching does take place if the operational amplifier is connected as a unity gain buffer and should make provision to allow for input offset voltage variations.

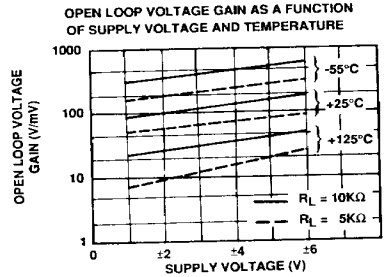
3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. Normally, this extremely high input impedance of greater than $10^{12}\ \Omega$ would not be a problem as the source impedance would limit the node impedance. However, for applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

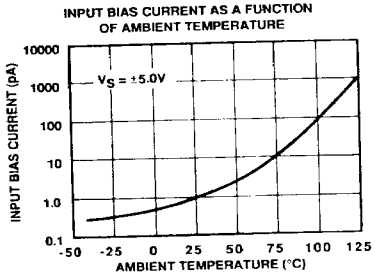
4. The output stage consists of symmetrical class AB complementary output drivers, capable of driving a low resistance load with up to 10 mA source current and 10 mA sink current. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. When connected in the voltage follower configuration, the oscillation resistant feature, combined with the rail to rail input and output feature, makes an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.

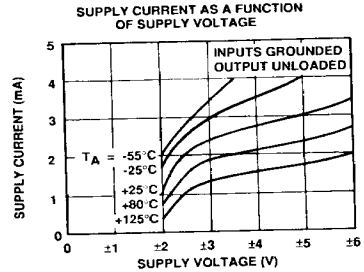
5. The ALD 1704 operational amplifier has been designed to provide full static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages to not exceed 0.3V of the power supply voltage levels.

TYPICAL PERFORMANCE CHARACTERISTICS



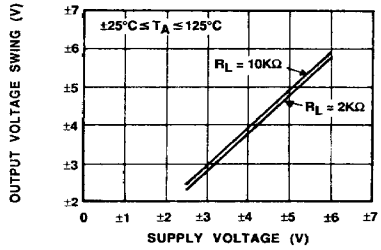




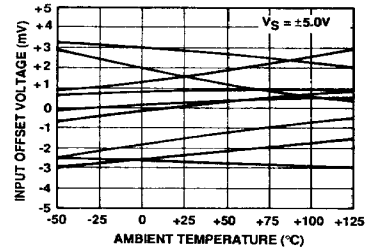


TYPICAL PERFORMANCE CHARACTERISTICS

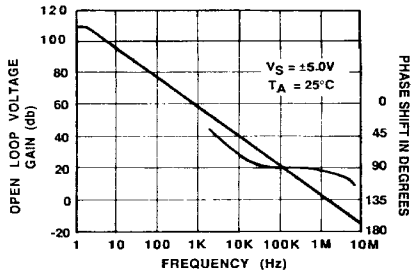
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



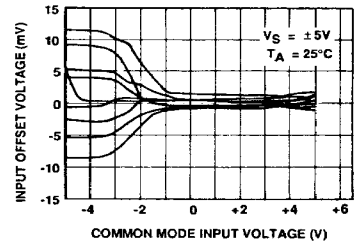
INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE REPRESENTATIVE UNITS



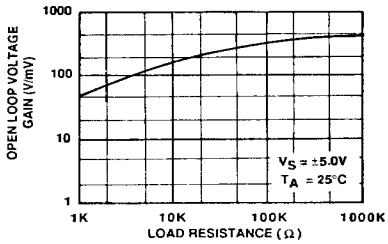
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



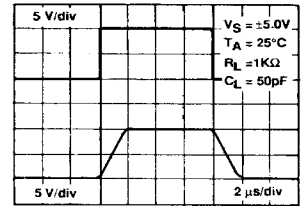
INPUT OFFSET VOLTAGE AS A FUNCTION OF COMMON MODE INPUT VOLTAGE



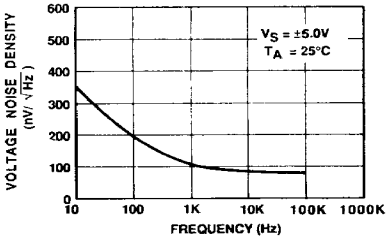
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



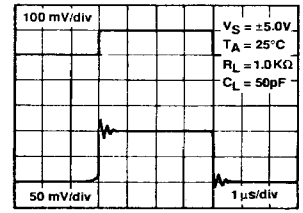
LARGE-SIGNAL TRANSIENT RESPONSE



VOLTAGE NOISE DENSITY AS A FUNCTION OF FREQUENCY



SMALL-SIGNAL TRANSIENT RESPONSE



DC AND OPERATING ELECTRICAL CHARACTERISTICS (cont'd)
T_A = 25°C V_S = ±5.0V unless otherwise specificied

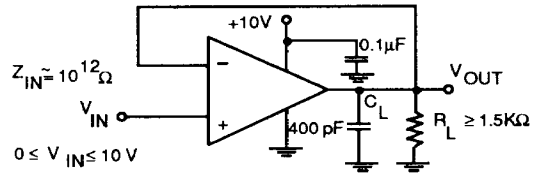
Parameter	Symbol	1704A			1704B			1704			1704G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Maximum Load Capacitance	C_L		400			400			400			400		pF	
Input Noise Voltage	e_n		100			100			100			100		nV/√Hz	f=1 KHz
Input Current Noise	i_n		.001			.001			.001			.001		pA/√Hz	f=10 Hz
Settling Time	t_s		5.0 2.0			5.0 2.0			5.0 2.0			5.0 2.0		µs µs	0.01% 0.1% A_V=-1 R_L=5KΩ C_L=50 pF

V_S = ±5.0V −55°C ≤ T_A ≤ +125°C unless otherwise specified

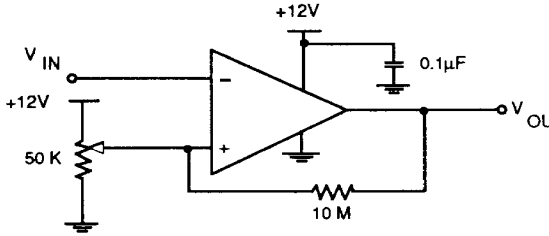
Parameter	Symbol	1704A DA			1704B DA			1704 DA			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input Offset Voltage	V_{OS}			2.0			4.0			7.0	mV	R_S≤100KΩ
Input Offset Current	I_{OS}			8.0			8.0			8.0	nA	
Input Bias Current	I_B			10.0			10.0			10.0	nA	
Power Supply Rejection Ratio	PSRR	60	75		60	75		60	75		dB	R_S≤100KΩ
Common Mode Rejection Ratio	CMRR	60	83		60	83		60	83		dB	R_S≤100KΩ
Large Signal Voltage Gain	A_V	30	125		30	125		30	125		V/mV	R_L=10KΩ
Output Voltage Range	$V_O$low $V_O$high	4.8	-4.9 4.9	-4.8	4.8	-4.9 4.9	-4.8	4.8	-4.9 4.9	-4.8	V V	R_L=10KΩ

TYPICAL APPLICATIONS

RAIL TO RAIL VOLTAGE FOLLOWER/BUFFER



RAIL TO RAIL VOLTAGE COMPARATOR



LOW OFFSET SUMMING AMPLIFIER

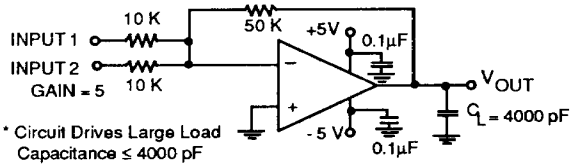
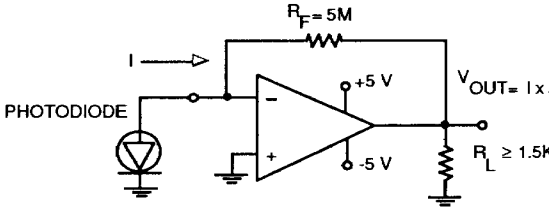
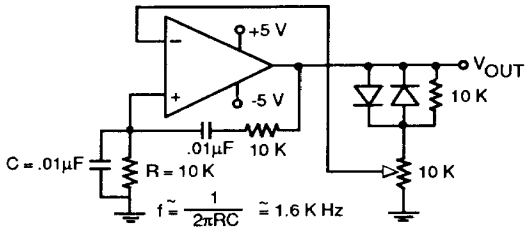


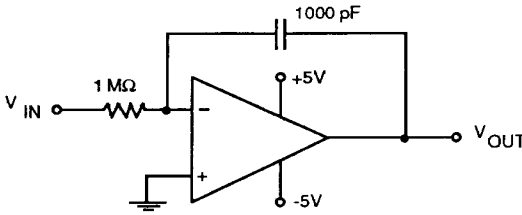
PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER



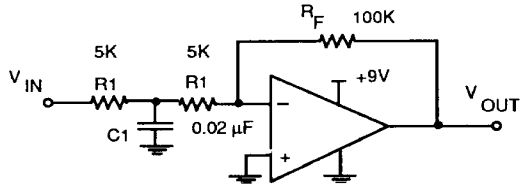
WIEN BRIDGE OSCILLATOR (RAIL TO RAIL) SINE WAVE GENERATOR



PRECISION CHARGE INTEGRATOR



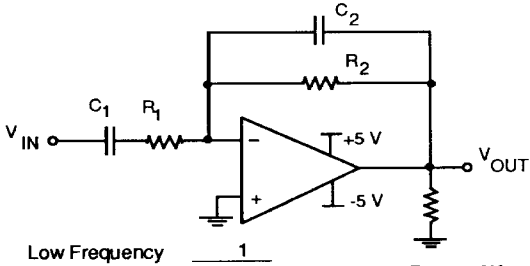
LOW PASS FILTER (RFI FILTER)



$$\text{Cutoff frequency} = \frac{1}{\pi R_1 C_1} = 3.2 \text{ KHz}$$

Gain = 10 Frequency roll-off 20 dB/decade

BANDPASS NETWORK



Low Frequency Breakpoint $fL = \frac{1}{2\pi R_1 C_1} = 160$ Hz

High Frequency Cutoff $fH = \frac{1}{2\pi R_2 C_2} = 32$ KHz

R_1 = 10K
C_1 = 100 nF
R_2 = 10K
C_2 = 500 pF