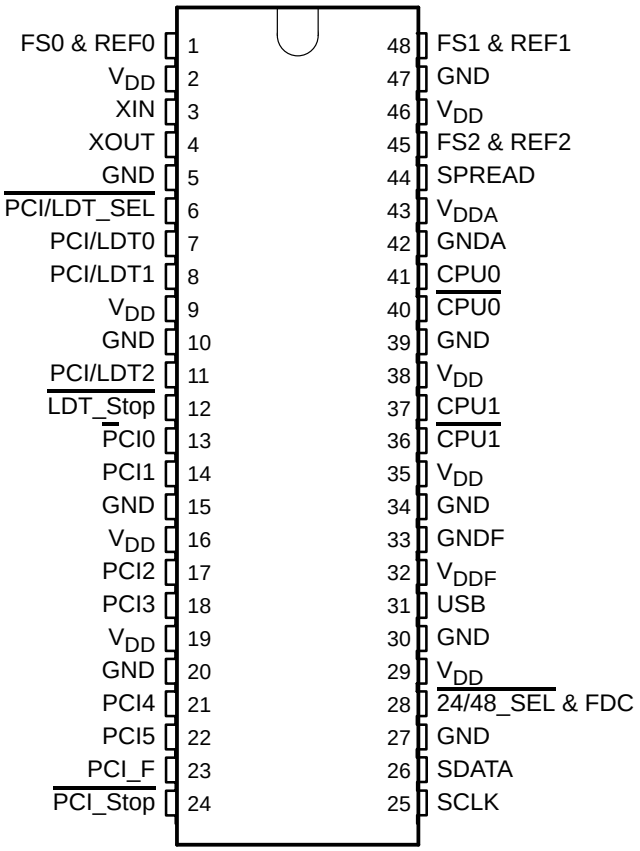
- **Generates Clocks for AMD-K8 Clawhammer Desktop Systems**
- **Uses a 14.318-MHz Crystal Input to Generate Multiple Output Frequencies**
- **Includes Spread Spectrum Clocking (SSC), 0.5% Downspread for Reduced EMI**
- **Power Management Control Terminals**
- **SMBus Serial Interface Provides Output Enable and Control**
- **Low-Output Skew and Low Jitter for Clock Distribution**
- **Operates From Single 3.3-V Supply**
- **Generates the Following Clocks:**
  - **2 CPU (3.3 V, 180° shifted pairs, 200/166/133/100 MHz)**
  - **6 PCI (3.3 V, 33 MHz)**
  - **1 PCI_F (3.3 V, 33 MHz)**
  - **3 REF (3.3 V, 14.318 MHz)**
  - **1 USB (3.3 V, 48 MHz)**
  - **1 FDC (3.3 V, 24 MHz or 48 MHz)**
  - **3 PCI/LDT† (3.3 V, 33 MHz or 66 MHz)**
- **Packaged in 48-Pin SSOP Package**

DL PACKAGE
(TOP VIEW)



description

The CDC960 is a clock synthesizer/driver and buffer that generates CPU, PCI, PCI/LDT, USB, FDC, and REF system clock signals to support PCs with an AMD-K8 Clawhammer-class system.

All output frequencies are generated from a 14.318-MHz crystal input. A reference clock input can be provided at the XIN input instead of a crystal. It is recommended to use the bypass mode of the internal oscillator in this case. Two phase-locked loops (PLLs) are used to generate the host frequencies and 48-MHz clock frequencies. On-chip loop filters and internal feedback eliminate the need for external components.

The device provides a standard mode (100 kbps) SMBus 1.1 serial interface for device control. The implementation is as a slave with read and write capability. The device address is specified in the SMBus serial interface device address table. Both SMBus inputs (SDATA and SCLK) provide integrated pullup resistors (typically 150 kΩ).

Seven 8-bit SMBus registers provide individual enable control for each of the outputs. The controllable outputs default to enabled at power up and can be placed in a disabled mode with a low-level output when a low-level control bit is written to the control register. The registers must be accessed in sequential order (i.e., random access of the registers not supported).

The CPU, PCI, PCI_F, LDT, FDC (24/48-MHz), and USB (48-MHz) clock outputs provide low-skew/low-jitter clock signals for reliable clock operation. All outputs have 3-state capability, which can be selected via control inputs FS0, FS1, and FS2 at power-up preset condition.

†LDT is equivalent to HT66 shown on AMD specification.

description (continued)

The CPU bus is a 3.3-V differential push-pull output type. All others are single-ended CMOS buffers.

The host frequencies are fixed and are controlled by the FS0, FS1 and FS2 signals at power-up. The CPU bus frequencies are 200, 166, 133 and 100 MHz.

Because the CDC960 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. With use of external reference clock, this signal must be fixed-frequency and fixed-phase prior stabilization time starts.

FUNCTION TABLES

DEVICE FREQUENCY SELECT FUNCTIONS

SMBUS CONTROLLED		INPUTS					OUTPUTS							
FS4 (Byte 0, Bit 5)	FS3 (Byte 0, Bit 4)	$\overline{24/48\_SEL}$‡	$\overline{PCI/LDT\_SEL}$‡	FS2	FS1	FS0	CPU	PCI_F PCI	PCI/LDT	USB†	FDC†	REF†	Comment	FUNCTION
L	L	H	H	H	H	H	200 MHz	33 MHz	33 MHz	48 MHz	24 MHz	14.31818 MHz		FSx and 24/48_SEL# pins are latched at power up
L	L	H	L	H	H	H	200 MHz	33 MHz	66 MHz	48 MHz	24 MHz	14.31818 MHz		
L	L	L	H	H	H	H	200 MHz	33 MHz	33 MHz	48 MHz	48 MHz	14.31818 MHz		
L	L	L	L	H	H	H	200 MHz	33 MHz	66 MHz	48 MHz	48 MHz	14.31818 MHz		
L	L	H/L	H/L	H	H	L	166 MHz	33 MHz	33/66 MHz	48 MHz	24/48 MHz	14.31818 MHz		
L	L	H/L	H/L	H	L	H	133 MHz	33 MHz	33/66 MHz	48 MHz	24/48 MHz	14.31818 MHz		
L	L	H/L	H/L	H	L	L	100 MHz	33 MHz	33/66 MHz	48 MHz	24/48 MHz	14.31818 MHz		
L	L	X	H	L	L	H	Xin	Xin/6	Xin/6	L	L	L	$f_{(xin)}$ = 0 to 200 MHz	Modes Test: PLL by-pass mode
L	L	X	L	L	L	H	Xin	Xin/6	Xin/3	L	L	L		
L	L	H	H	L	H	H	Xin	Xin/6	Xin/6	Xin/2	Xin/4	Xin	$f_{(xin)}$ = 0 to 16 MHz	
L	L	H	L	L	H	H	Xin	Xin/6	Xin/3	Xin/2	Xin/4	Xin		
L	L	L	H	L	H	H	Xin	Xin/6	Xin/6	Xin/2	Xin/2	Xin		
L	L	L	L	L	H	H	Xin	Xin/6	Xin/3	Xin/2	Xin/2	Xin		
L	L	X	X	L	H	L	Reserved for future use							
L	L	X	X	L	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z		
L	H	H/L	H/L	H	H	H	90 MHz	30 MHz	30/60 MHz	48 MHz	24/48 MHz	14.31818 MHz	–10%	
L	H	H/L	H/L	H	H	L	119 MHz	30 MHz	30/60 MHz	48 MHz	24/48 MHz	14.31818 MHz	–10%	
L	H	H/L	H/L	H	L	H	180 MHz	36.3 MHz	36.3/72.6 MHz	48 MHz	24/48 MHz	14.31818 MHz	–10%	
L	H	H/L	H/L	H	L	L	180 MHz	30 MHz	30/60 MHz	48 MHz	24/48 MHz	14.31818 MHz	–10%	
L	H	H/L	H/L	L	H	H	111 MHz	36.9 MHz	36.9/73.9 MHz	48 MHz	24/48 MHz	14.31818 MHz	10%	
L	H	H/L	H/L	L	H	L	148 MHz	36.9 MHz	36.9/73.9 MHz	48 MHz	24/48 MHz	14.31818 MHz	10%	
L	H	H/L	H/L	L	L	H	222 MHz	44.4 MHz	44.4/88.8 MHz	48 MHz	24/48 MHz	14.31818 MHz	10%	
L	H	H/L	H/L	L	L	L	222 MHz	36.9 MHz	36.9/73.9 MHz	48 MHz	24/48 MHz	14.31818 MHz	10%	
H	X	H/L	H/L	X	X	X	Not-yet-defined settings							

† If the REF, USB, and FDC outputs are disabled in by pass mode, the Xin-input can be driven with an external clock signal from 0 MHz to 200 MHz. Otherwise the maximum input frequency is limited to 16 MHz.

‡ $\overline{24/48\_SEL}$ and $\overline{PCI/LDT\_SEL}$ inputs operate independently from each other and the frequency of the corresponding bus, as shown in detail for the 200-MHz configuration.

FUNCTION TABLES (Continued)

SPREAD SPECTRUM

INPUT		
Spread	0	Spread spectrum disabled
	1	Spread spectrum enabled, –0.5% at CPU/$\overline{\text{CPU}}$, PCI/LDT, PCI_F, PCI

DEVICE ENABLE FUNCTIONS

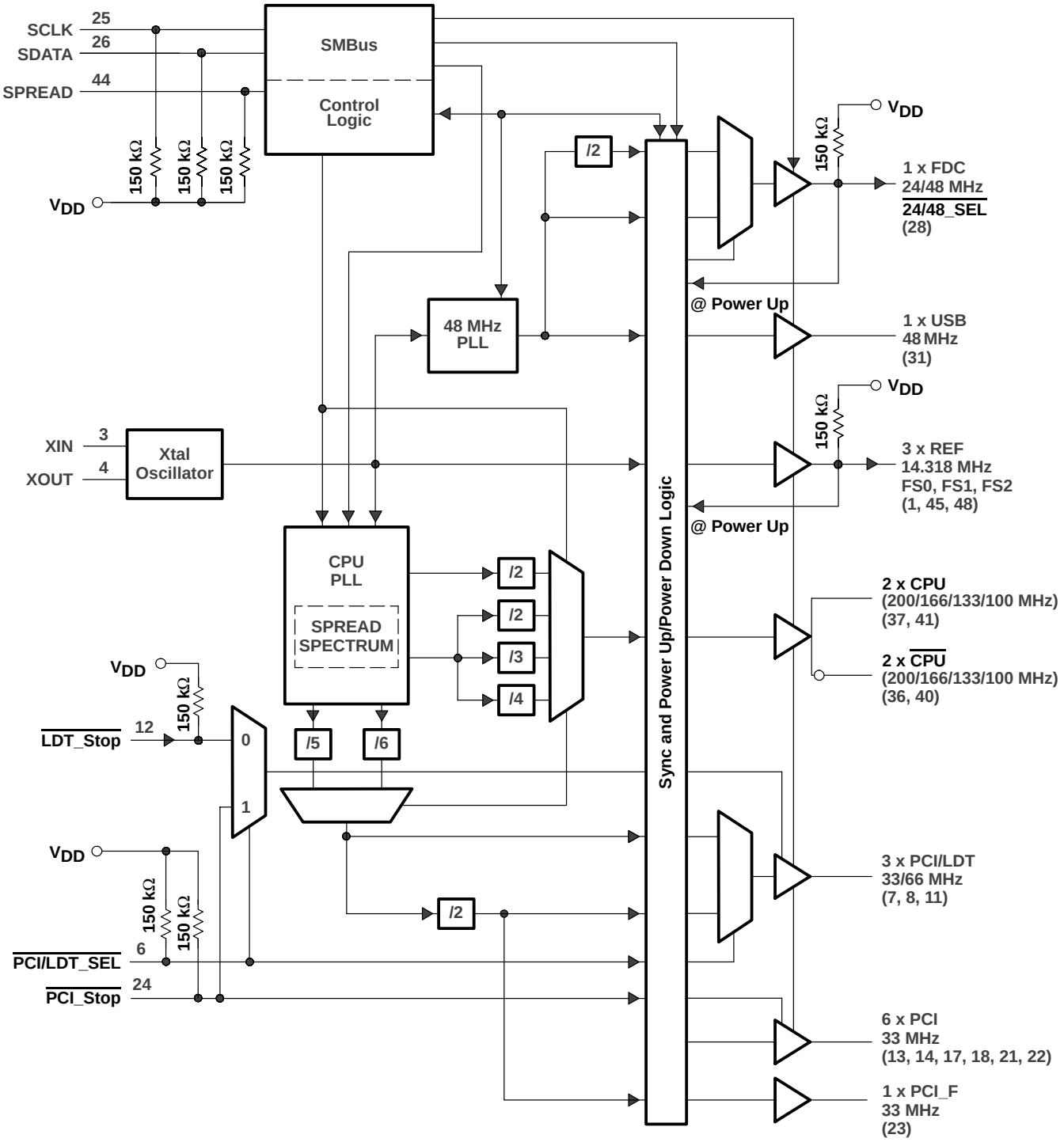
SMBus CONTROLLED		INPUTS									OUTPUTS									INTERNAL	
FS4 (Byte 0, Bit 5)	FS3 (Byte 0, Bit 4)	$\overline{\text{24/48\_SEL}}$	$\overline{\text{PCI/LDT\_SEL}}$	$\overline{\text{LDT\_Stop}}$	$\overline{\text{PCI\_Stop}}$	FS2	FS1	FS0	SPREAD	XIN	CPU	$\overline{\text{CPU}}$ ++	PCI_F	PCI	PCI/LDT	USB	FDC	REF	Comment	CRYSTAL	VCOs
L	L	X	X	X	X	L	L	L	X	Xtal	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z		Off	Off
L	X	X	H	H	H	H	X	X	X	Xtal	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓		↑↓	↑↓
L	X	X	H	H	L	H	X	X	X	Xtal	↑↓	↑↓	↑↓	L	L	↑↓	↑↓	↑↓		↑↓	↑↓
L	X	X	H	L	H	H	X	X	X	Xtal	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓		↑↓	↑↓
L	X	X	H	L	L	H	X	X	X	Xtal	↑↓	↑↓	↑↓	L	L	↑↓	↑↓	↑↓		↑↓	↑↓
L	X	X	L	H	H	H	X	X	X	Xtal	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓		↑↓	↑↓
L	X	X	L	H	L	H	X	X	X	Xtal	↑↓	↑↓	↑↓	L	↑↓	↑↓	↑↓	↑↓		↑↓	↑↓
L	X	X	L	L	H	H	X	X	X	Xtal	↑↓	↑↓	↑↓	↑↓	L	↑↓	↑↓	↑↓		↑↓	↑↓
L	X	X	L	L	L	H	X	X	X	Xtal	↑↓	↑↓	↑↓	L	L	↑↓	↑↓	↑↓		↑↓	↑↓
L	L	X	X	X	H	L	L	H	X	H	H	L	HL	HL	HL	L	L	L	PLL BYPASS MODE	Off	Off
L	L	X	H	X	H	L	L	H	X	L	L	H	HL	HL	HL	L	L	L		Off	Off
L	L	X	H	H	L	L	L	H	X	L	L	H	HL	L	L	L	L	L		Off	Off
L	L	X	L	L	H	L	L	H	X	H	H	L	HL	HL	L	L	L	L		Off	Off
L	L	X	L	H	L	L	L	H	X	L	L	H	HL	L	HL	L	L	L		Off	Off
L	L	X	H	H	L	L	H	X	X	H	H	L	HL	L	L	HL	HL	HL		Off	Off
L	L	X	H	H	L	L	H	X	X	L	L	H	HL	L	L	HL	HL	HL		Off	Off
L	L	X	H	L	H	L	H	X	X	H	H	L	HL	HL	HL	HL	HL	HL		Off	Off
L	L	X	H	L	H	L	H	X	X	L	L	H	HL	HL	HL	HL	HL	HL		Off	Off
L	L	X	L	H	L	L	H	X	X	L/H	L/H	H/L	HL	L	HL	HL	HL	HL		Off	Off
L	L	X	L	L	H	L	H	X	X	L/H	L/H	H/L	HL	HL	L	HL	HL	HL		Off	Off
L	L	X	L	L	L	L	H	X	X	L/H	L/H	H/L	HL	L	L	HL	HL	HL		Off	Off

† SMBus bits set to their reset values
‡ Hi-Z will have LOW state if external load circuit is applied, CPU and $\overline{\text{CPU}}$ are push-pull type outputs.
↑↓ Outputs toggle at the selected frequency according to the Device Frequency Select FunctionS table above.
HL device output state is undefined, either L or H. It is L if Xin is held static at L or H before the bypass mode is selected.

OUTPUT BUFFER SPECIFICATIONS

BUFFER NAME	V_{DD} RANGE (V)	IMPEDANCE (Ω)	LUMPED TEST LOAD
CPU	3.135 – 3.465	40	10 pF
PCI, PCI_F, LDT	3.135 – 3.465	25	30 pF
REF, USB, FDC	3.135 – 3.465	35	20 pF

functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CPU[0:1],$\overline{\text{CPU}}$[0:1]	41, 37 40, 36	O	3.3-V, differential CPU clock outputs CPU Clock Outputs 0 and 1: CPU push-pull true clock outputs of the differential pair $\overline{\text{CPU}}$ Clock Outputs 0 and 1: CPU push-pull complementary clock outputs of the differential pair
FS[0:2] & REF[0:2]	1, 48, 45	I/O	3.3 V, 14.318-MHz clock outputs Frequency Select inputs: Power–on strapping to set device operating frequency as described in the Device Frequency Select Functions table. These inputs have 150-kΩ internal pullup resistors. Low = 0, High = 1. 3.3-V reference clock outputs: Fixed clock output at 14.318 MHz
GND	5, 10, 15, 20, 27, 30, 34, 39, 47	G	Power Connection: Connected to V_{SS}. Used to ground digital portions of the chip
GNDA	42	G	Analog GND: Connected to VSS through filter. Used to ground the main CPU-PLL on the chip
GNDF	33	G	Analog GND for 48-MHz PLL: Connected to V_{SS} through filter. Used to ground the 48-MHz PLL on the chip
$\overline{\text{LDT\_Stop}}$	12	I	Control for 66-MHz PCI clocks: Active LOW control input to halt all 66-MHz PCI clocks except the free-running clock. This input has a 150-kΩ internal pullup resistor. Once this input has been asserted, PCI/LDT outputs if operating at 66-MHz must stop in the low state within 1 μs. Low = stop, High = running
PCI[0:5]	13, 14, 17, 18, 21, 22	O	3.3-V PCI clock outputs divided down from CPU-PLL 3.3-V PCI clock outputs: PCI clocks operate at 33 MHz.
PCI_F	23	O	3.3-V, 33-MHz clocks divided down from CPU-PLL 3.3-V Free-Running PCI clock output: The free-running PCI clock pin operates at 33 MHz. The free-running PCI clock is not turned off when PCI_Stop# is activated LOW.
PCI/LDT[0:2]	7, 8, 11	O	3.3-V PCI 33-MHz or LDT 66-MHz outputs: This group of outputs is selectable between 33 MHz and 66 MHz based upon the state of PCI/LDT_SEL. When running at 66 MHz these outputs are for use as reference clocks to LDT devices.
$\overline{\text{PCI/LDT\_SEL}}$	6	I	PCI 33-MHz/LDT 66-MHz Select: This input selects the output frequency of PCI/LDT outputs to either 33 MHz or 66 MHz. This is a dedicated input pin to avoid corruption of the input state due to PCI add-in cards that may have termination resistors on the input clocks. This input has a 150-kΩ internal pullup resistor. Low = 66-MHz outputs, High = 33-MHz outputs
$\overline{\text{PCI\_Stop}}$	24	I	3.3-V LVTTL-compatible input for $\overline{\text{PCI\_Stop}}$ active low Control for 33-MHz PCI clocks: Active LOW control input to halt all 33-MHz PCI clocks except the free-running clock. This input has a 150-kΩ internal pullup resistor. Once this input has been asserted, the PCI outputs and PCI/LDT outputs operating at 33 MHz must stop in the low state within 1 μs. Low = stop, High = running
SCLK	25	I	SMBus compatible SCLK. Clock pin for SMBus circuitry (SMBus revision 1.1). This input has an internal pull-up resistor of 150 kΩ. SCLK is a 3.6-V tolerant signal input. High impedance at power down is not supported.
SDATA	26	I/O	SMBus compatible SDATA Data pin for SMBus circuitry (SMBus revision 1.1). This output is open drain and has an internal pullup resistor of 150 kΩ. SDATA is a 3.6V tolerant signal IO. High impedance at power down is not supported.
SPREAD	44	I	Spread Spectrum Clocking Enable: Power-on strapping to set spread spectrum clocking as enabled or disabled. This input allows the default spread spectrum clocking mode to be enabled or disabled upon power up. This input has a 150-kΩ internal pullup resistor. Low = disable, High = enable. Note that all Athlon and Hammer systems are recommended to use SSC; therefore, the default of this pin is enabled and should only be turned off for debug and test purposes.
USB	31	O	3.3-V, fixed 48-MHz non-SSC clock output 3.3-V USB clock output: Fixed clock output at 48 MHz
V_{DD}	2, 9, 16, 19, 29, 35, 38, 46	P	Power Connection: Connected to 3.3-V power supply. Used to supply digital portions of the chip

Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V_{DDA}	43	P	Analog V_{DD}: Connected to 3.3-V power supply through filter. Used to supply the main CPU-PLL on the chip
V_{DDF}	32	P	Analog V_{DD} for 48-MHz PLL: Connected to 3.3-V power supply through filter. Used to supply the 48-MHz PLL on the chip
XIN	3	I	Crystal input – 14.318 MHz Crystal Connection or External Reference: Reference crystal input or external reference clock input. This pin includes an internal 36-pF load capacitance to eliminate the need for an external load capacitor.
XOUT	4	O	Crystal output – 14.318 MHz Crystal Connection: Reference crystal feedback. This output includes an internal 36-pF load capacitance to eliminate the need for an external load capacitor.
$\overline{24/48\_SEL}$ & FDC	28	I/O	3.3-V super I/O clock output: The super I/O clock can be strapped for 24 MHz or 48 MHz. This input has a 150-kΩ internal pullup resistor. Low = 48-MHz output, High = 24-MHz output

connecting SCLK and SDATA to 5-V SMBus signals

SCLK and SDATA of CDC960 have been designed to work within a 3.3-V supply voltage environment only. In order to connect SCLK and SDATA to a 5-V SMBus configuration, external circuitry is required. A simple and inexpensive solution is to use clamping diodes. Two approaches are recommended for this solution:

1. **Using Zener diode to clamp to GND in reverse-biased direction**

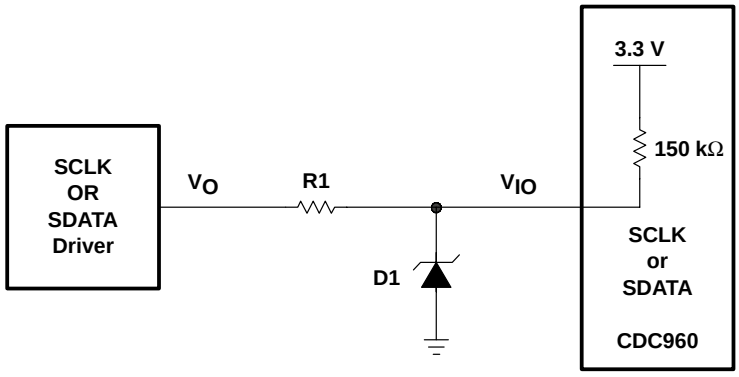


Figure 1. SCLK SDATA Connection to 5-V SMBus Using Zener Diode

Zener diode D1 in Figure 1 is chosen such that the Zener voltage (V_{ZK}) cannot exceed 300 mV above V_{DD} of the CDC960. The minimum value of V_{ZK} must be greater than 2.1 V to meet minimum requirement for V_{IH} of the CDC960. The value of R1 is chosen to satisfy requirements both for I_{OH} of the driver of SCLK and SDATA and for V_{OL} and I_{OL} of SDATA of CDC960.

$$I_{OH} \le \frac{V_O - V_{IO}}{\left(R1 + R_S\right)} \quad \text{(For the driver of SCLK and SDATA. } R_S \text{ is the source driver impedance.)} \tag{1}$$

$$2\ \text{mA} \le \frac{0.8\ \text{V}}{R1 + Z_O} \le 6\ \text{mA} \qquad \text{(For a SDATA of CDC960, } 25\ \Omega < Z_O < 47\ \Omega\text{)} \tag{2}$$

$$\left(R1 + Z_O\right) \times 1.75\ \text{mA} < 0.4\ \text{V} \quad \text{(For a SDATA of CDC960, } 25\ \Omega < Z_O < 47\ \Omega\text{)} \tag{3}$$

connecting SCLK and SDATA to 5-V SMBus signals (continued)

There are many manufacturers making Zener diodes that can be used for this application. Panasonic MA8033 and Vishay BZX84C3V3 that have 3.1 V < V_Z < 3.5 V can be used for this application. In this case R1 is recommended as 150 Ω.

The worst I_{OH} in equation (1) is 16 mA when V_{OH} = 5.5 V, R_S = 0 Ω and V_{IO} = 3.1 V.

The current in equation (2), between 4 mA and 4.6 mA, satisfies the requirement.

Equation (3) is also satisfied with the selected R1 and diode.

2. Clamping Diode to V_{DD}

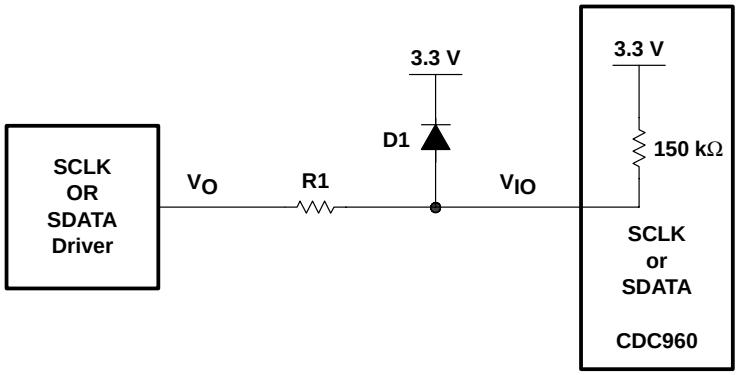


Figure 2. SCLK SDATA Connection to 5-V SMBus Using Clamping Diode to V_{DD}

Diode D1 in Figure 2 should have a small forward voltage (V_F). Ideally, we want V_F to be less than 300 mV to meet the input voltage requirement of the CDC960. International IOR Rectifier has a device (part number 10BQ015) with maximum V_F of 350 mV at 1.0 A. Using the 10BQ015 with R1 = 150 Ω, the worst-case I_{OH} is calculated using equation (4).

$$I_{OH} = \frac{5.5\ V - (3.0 - 0.35)\ V}{150\ \Omega} = 14\ mA \quad (4)$$

The calculation for equations (2) and (3) is the same as in part 1.

When using the configuration in Figure 2, the power supply is required to have a capability of sinking current. The total amount of sinking current is dependent on the overall load connected to that power supply.

Using the above interface circuitry with a high-impedance source, the available high-level voltage on the SMBus is limited to about (V*zk*) for the configuration in Figure 1 and ($VDD_{(CDC960)}$ + $V_{F(D1)}$) for the configuration in Figure 2. One has to choose which option best fits a given SMBus configuration.

Actually, the typical SMBus configuration is an open-drain configuration with pullup resistors to the corresponding power supply. It does not require a 5-V SMBus driver that has a low impedance to drive the CDC960 SMBus ports with its additional components as shown in Figure 1 and Figure 2. The external components are not needed if the pullup resistors of the SMBus are directly connected to a voltage equal to the supply voltage of the CDC960 (typically 3.3 V). This pullup resistor connection is strongly recommended.

power-up sequences

Sampled inputs are: FS0, FS1, FS2 and $\overline{24/48\_SEL}$.

State S1 is an analog controlled delay derived from internal reference voltages to ensure that a valid input state is captured. There is no specific delay in this state after power up.

Figure 3 shows the symbolic sequence of the CDC960 during power up. States S0–S4 are required to ensure proper configuration and operation of the device functions.

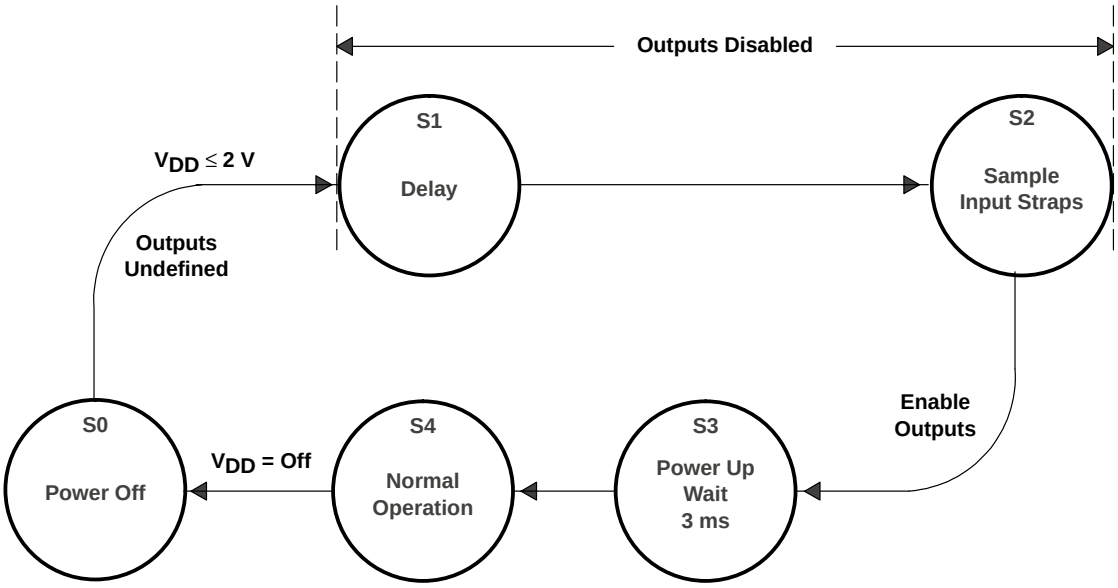


Figure 3. Power-Up State Transitions

SMBus serial interface

The following section describes the SMBus interface programming.

In general the CDC960 SMBus protocol supports only block write and block read operations.

SMBus device address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	1	0	1	0	0	1	0

0 = write to CDC960
1 = read from CDC960

writing to the SMBus interface

1. Send the address $D2_{(H)}$ and validate the acknowledge from the slave.
2. Send the dummy byte as a command code and validate the acknowledge from the slave.
3. Send the number of data bytes to write and validate the acknowledge from the slave.
4. Write the desired data bytes to registers and validate the acknowledge from the slave for each data byte.

Clock Generator Addr (7 bits)	ACK	+8 bits dummy command code	ACK	+8 bits byte count	ACK	Data byte 0	ACK	Data byte N	ACK
A(6:0) & R/$\overline{W}$									
$D2_{(H)}$									

SMBus serial interface (continued)

reading the SMBus interface, using address pre-phase

1. Send the address $D2_{(H)}$ and validate the acknowledge from the slave.
2. Send dummy byte as command code and validate the acknowledge from the slave.
3. Send repeated start condition followed by address $D3_{(H)}$ and validate the acknowledge from the slave.
4. The slave returns the number of bytes it is going to send (byte count) and validates the acknowledge from the master.
5. Read back the desired data bytes and validate the acknowledge sent by the master for each data byte.

Clock Generator Addr (7 bits)	ACK	+8 bits dummy command code	ACK	Repeated Start	Clock Generator Addr (7 bits)	ACK	+8 bit byte count	ACK by master	Data byte 0	ACK by master	Data byte N	ACK by master
A(6:0)& R/W					A(6:0)& R/W							
$D2_{(H)}$					$D3_{(H)}$							

reading the SMBus interface, using direct read

1. Send the address $D3_{(H)}$ and validate the acknowledge from the slave.
2. The slave returns the number of bytes it is going to send (byte count) and validates the acknowledge from the master.
3. Read back the desired data bytes and validate the acknowledge sent by the master for each data byte.

Clock Generator Addr (7 bits)	ACK	+8 bit byte count	ACK by master	Data byte 0	ACK by master	Data byte N	ACK by master
A(6:0)& R/$\overline{W}$							
$D3_{(H)}$							

SMBus configuration command bitmap

Byte 0: Frequency and Spread Spectrum Control Register (see Note 1) (H = Enable, L = Disable)

BIT	TYPE	PUD†	DESCRIPTION	PIN AFFECTED (WRITE OPERATION)	SOURCE PIN (READ OPERATION)
7	R/W	L	Write disable (write once). A 1 written to this bit after a 1 has been written to Byte0, Bit0 disables modification of all configuration registers until the device has been powered off.	—	Register value
6	R/W	L	Spread spectrum enable. This bit provides a software programmable control forspread spectrum clocking. The truth table for SSC is as follows:	—	Register value
5	R/W	L	FS4 (corresponds to frequency selection table)	—	Register value
4	R/W	L	FS3 (corresponds to frequency selection table)	—	Register value
3	R/W	Externally selected‡	FS2 (corresponds to frequency selection table). If write is enabled, this bit can be set differently than the power-up condition.	—	45 at power up
2	R/W	Externally selected‡	FS1 (corresponds to frequency selection table). If write is enabled, this bit can be set differently than the power-up condition.	—	48 at power up
1	R/W	Externally selected‡	FS0 (corresponds to frequency selection table). If write is enabled, this bit can be set differently than the power-up condition.	—	1 at power up
0	R/W	L	Write Enable. A 1 written to this bit after power up enables modification of all configuration registers and subsequent 0s written to this bit disable modification of all configuration registers except this single bit. Note that when a 1 has been written to Byte0, Bit 7, all modification is permanently disabled until the device power cycles. Note also, that block write transactions to the interface are completed. However, unless the interface has been previously unlocked, the writes have no effect.	—	Register value

Spread (ext. Pin)	Byte0, Bit6	SSC Function
L	L	Disabled
L	H	Enabled
H	L	Enabled
H	H	Enabled

† PUD = Power-up condition

‡ The value of this bit is according to level applied to corresponding device pin at power up.

NOTE 1: Byte0, Bit0 controls the write enable status for the device SMBus. If a 1 is written to Byte0, Bit0, the SMBus registers are write enabled. Once write has been enabled, a new block write protocol must be sent to the device to program the desired register values. Once after power up a 1 is written to Byte0, Bit0, the device functionality is according to the settings of the different registers. E.g., the device function table is according to setting of Bits[1…6] of Byte0 and other functions are according to corresponding SMBus register settings. If a 0 is written to Byte0, Bit0, write is disabled and the device function is according to the previous settings of the last write cycle.

Byte 1: PCI Clock Control Register (H = Enable, L = Disable)

BIT	TYPE	PUD†	DESCRIPTION	PIN AFFECTED (WRITE OPERATION)	SOURCE PIN (READ OPERATION)
7	R/W	H	PCI/LDT1 enable	8	Register value
6	R/W	H	PCI/LDT0 enable	7	Register value
5	R/W	H	PCI5 enable	22	Register value
4	R/W	H	PCI4 enable	21	Register value
3	R/W	H	PCI3 enable	18	Register value
2	R/W	H	PCI2 enable	17	Register value
1	R/W	H	PCI1 enable	14	Register value
0	R/W	H	PCI0 enable	13	Register value

† PUD = Power-up condition

SMBus configuration command bitmap (continued)

Byte 2: PCI Clock USB FDC and REF Control Register (H = Enable, L = Disable)

BIT	TYPE	PUD†	DESCRIPTION	PIN AFFECTED (WRITE OPERATION)	SOURCE PIN (READ OPERATION)
7	R/W	H	CPU1 enable‡	36, 37	Register value
6	R/W	H	CPU0 enable‡	40, 41	Register value
5	R/W	H	REF2 enable	45	Register value
4	R/W	H	REF1 enable	48	Register value
3	R/W	H	REF0 enable	1	Register value
2	R/W	H	FDC (24_48 MHz) enable	28	Register value
1	R/W	H	USB enable	31	Register value
0	R/W	H	PCI/LDT2 enable	11	Register value

† PUD = Power-up condition
‡ If a CPU clock is disabled by setting its control bit (bit 6 or bit 7) low, both the CPU and $\overline{\text{CPU}}$ outputs for the disabled clock are set low.

Byte 3: PCI Clock Free Running Control Register (H = Free running, L = controlled by $\overline{\text{PCI\_Stop}}$/$\overline{\text{LDT\_Stop}}$))

BIT	TYPE	PUD†	DESCRIPTION	PIN AFFECTED (WRITE OPERATION)	SOURCE PIN (READ OPERATION)
7	R/W	L	PCI/LDT1 free-running enable§	8	Register value
6	R/W	L	PCI/LDT0 free-running enable§	7	Register value
5	R/W	L	PCI5 free-running enable§	22	Register value
4	R/W	L	PCI4 free-running enable§	21	Register value
3	R/W	L	PCI3 free-running enable§	18	Register value
2	R/W	L	PCI2 free-running enable§	17	Register value
1	R/W	L	PCI1 free-running enable§	14	Register value
0	R/W	L	PCI0 free-running enable§	13	Register value

† PUD = Power-up condition
§ The above individual free-running enable/disable controls are intended to allow individual clock outputs to be made free running. A clock output that has its free-running bit enabled (set to H) is not turned off with the assertion of either $\overline{\text{PCI\_Stop}}$ or $\overline{\text{LDT\_Stop}}$. If a particular bit is disabled in Byte1, the Byte1 settings overwrite the Byte3 settings.

SMBus configuration command bitmap (continued)

Byte 4: Pin Latched/Real Time State Control Register (see Note 2) (H = Enable, L = Disable)

BIT	TYPE	PUD†	DESCRIPTION	PIN AFFECTED (WRITE OPERATION)	SOURCE PIN (READ OPERATION)
7	R/W	H	PCI_F enable	23	Register value
6	R	Externally selected‡§	SPREAD actual pin state		44
5	R	Externally selected‡	$\overline{24/48\_SEL}$ pin power up latched state		28 at power up
4	R	Externally selected‡§	$\overline{PCI/LDT\_SEL}$ actual pin state		6
3	R	Externally selected‡	FS2 power-up latched pin state		45 at power up
2	R	Externally selected‡	FS1 power-up latched pin state		48 at power up
1	R	Externally selected‡	FS0 power-up latched pin state		1 at power up
0	R/W	L	PCI/LDT2 free-running enable¶	11	Register value

† PUD = Power-up condition

‡ The value of this bit is determined by the level applied to the corresponding device pin at power up.

§ If the SMBus is in read mode, and the byte-count byte is being sent, the device input pin is sampled again at the falling edge of SCLK at the same state as the acknowledge state for the byte count that is initiated by SCLK↓.

¶ The above individual free running enable/disable controls are intended to allow individual clock outputs to be made free running. A clock output that has its free-running bit enabled (set to H) is not turned off with the assertion of either $\overline{PCI\_Stop}$ or $\overline{LDT\_Stop}$. If a particular bit is disabled in Byte2, the Byte2 settings overwrite the Byte4 settings.

NOTE 2: Byte4 holds the power-up information for pins latched at power up. In the case that an unintentional write has been made to these bits of Byte4, the SMBus write is ignored; the bits always return the power-up latched value during an SMBus read operation.
This does not relate to the bits which hold the actual (current) pin state. Those bits can not be overwritten by software in order to get the hardware setting states back via software.

Byte 5: Vendor Identification Register (H = Enable, L = Disable)

BIT	TYPE	PUD†	DESCRIPTION	PIN AFFECTED (WRITE OPERATION)	SOURCE PIN (READ OPERATION)
7	R	H	Manufacturer ID (MSB)	–	Returns H
6	R	H	Manufacturer ID	–	Returns H
5	R	H	Manufacturer ID, TI is shown for vendor ID = 111	–	Returns H
4	R	L	Device revision ID (MSB)	–	Returns L
3	R	L	Device revision ID	–	Returns L
2	R	L	Device revision ID	–	Returns L
1	R	L	Device revision ID	–	Returns L
0	R	H	Device revision ID, device revision: 00001	–	Returns H

† PUD = Power-up condition

SMBus configuration command bitmap (continued)

Byte 6: Byte Count Control Register (H = Enable, L = Disable)

BIT	TYPE	PUD†	DESCRIPTION	PIN AFFECTED (WRITE OPERATION)	SOURCE PIN (READ OPERATION)
7	R/W	L	Byte count bit, MSB	–	Register value
6	R/W	L	Byte count bit	–	Register value
5	R/W	L	Byte count bit	–	Register value
4	R/W	L	Byte count bit	–	Register value
3	R/W	L	Byte count bit	–	Register value
2	R/W	H	Byte count bit	–	Register value
1	R/W	H	Byte count bit	–	Register value
0	R/W	H	Byte count bit, LSB	–	Register value

† PUD = Power-up condition

Byte 7: Vendor Specific Register (reserved) (H = Enable, L = Disable)

BIT	TYPE	PUD†	DESCRIPTION	PIN AFFECTED (WRITE OPERATION)	SOURCE PIN (READ OPERATION)
7	R/W	L	Must be set to L during the byte write	–	Register value
6	R/W	L	Must be set to L during the byte write	–	Register value
5	R/W	L	Must be set to L during the byte write	–	Register value
4	R/W	L	Must be set to L during the byte write	–	Register value
3	R/W	L	Must be set to L during the byte write	–	Register value
2	R/W	L	Must be set to L during the byte write	–	Register value
1	R	L	Must be set to L during the byte write	–	Register value
0	R	L	Must be set to L during the byte write	–	Register value

† PUD = Power-up condition

SMBus configuration command bitmap (continued)

Byte 8: Vendor Specific Register (reserved) **(H = Enable, L = Disable)**

BIT	TYPE	PUD†	DESCRIPTION	PIN AFFECTED (WRITE OPERATION)	SOURCE PIN (READ OPERATION)
7	R/W	L	Trigger single pulse at the L-to-H transition of this bit after an SMBus write cycle completes. This bit must be written back to L in order to trigger a following pulse with a new L-to-H transition at the completion of a write protocol.	CPU, $\overline{\text{CPU}}$	Register value
6	R/W	L	Single-pulse ARM bit H = enable, L = disable single-pulse feature	–	Register value
5	R/W	L	Must set to L during the byte write	–	Register value
4	R/W	L	Must set to L during the byte write	–	Register value
3	R/W	L	Must set to L during the byte write	–	Register value
2	R/W	L	Must set to L during the byte write	–	Register value
1	R/W	L	Must set to L during the byte write	–	Register value
0	R/W	L	Must set to L during the byte write	–	Register value

† PUD = Power-up condition

Single-pulse initialization

1. Device is in normal operating mode (frequencies selected by FS[4:0] as usual).
2. Put device into SMBus mode (set write enable bit according to specification).
3. Put device into required operating mode via the SMBus.
4. Set Byte8/Bit6 to H. Byte8 is a TI control byte, Bit6 is the ARM bit.
   a. The device continues running as in the normal operating mode, but the CPUx/$\overline{\text{CPUx}}$ outputs are pulled to low/high, respectively; i.e., the clock is low.
   b. All other clocks (PCI, LDT66, USB, 48-MHz, REFCLOCK) continue running as long as they are not disabled by the SMBus or other means.
5. Set Byte8/Bit7 to H. Byte8/Bit 7 is the SHOOT bit.
   a. The device recognizes a rising edge on this bit and sends a single high pulse on CPUx. The $\overline{\text{CPUx}}$ output is complementary (low). The pulse duration depends on frequency settings for the CPU-BUS (half of the period).
   b. CPU1 or $\overline{\text{CPU0}}$ can still be enabled/disabled via the SMBus as usual.
6. Set Byte8/Bit7 back to L for the next shot.
   a. Because the device only detects L→H transitions, this bit must be reset to L.
7. Now the device is ready for the next pulse (write H to Byte8/Bit7).
8. When setting the ARM bit to L, the single-shot feature is disabled and the device runs as usual.

spread spectrum clock (SSC) implementation for CDC960

Simultaneously switching at a fixed frequency generates a significant power peak at the selected frequency, which in turn causes an EMI disturbance to the environment. The purpose of the internal frequency modulation of the CPU-PLL is to distribute the energy to many different frequencies, thus reducing the power peak.

A typical characteristic for a single-frequency spectrum and a modulated-frequency spectrum is shown in Figure 4.

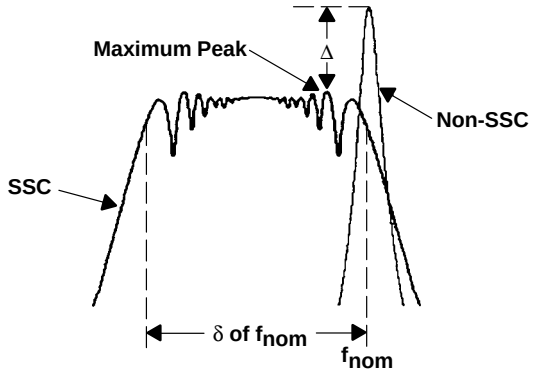


Figure 4. Frequency Power Spectrum With and Without the Use of SSC

The modulated spectrum has its distribution to the left side of the single-frequency spectrum, which indicates a *down-spread modulation*.

The peak reduction depends on the modulation scheme and modulation profile. System performance and timing requirements are the limiting factors for actual design implementations. The implementation is driven to keep the average clock frequency close to its upper specification limit. The modulation amount is set to –0.5%.

In order to allow a downstream PLL to follow the frequency modulated signal, the bandwidth of the modulation signal is limited in order to minimize SSC-induced tracking skew jitter.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 3) . . . . . –0.5 V to V_{DD} + 0.5 V
Voltage range applied to any output in the high-impedance state or power-off state,
V_O (see Note 3) . . . . . –0.5 V to V_{DD} + 0.5 V
Current into any output in the low state, I_O . . . . . 2 × rated I_{OL}
Input clamp current: I_{IK} (V_I < 0) . . . . . –18 mA
I_{IK} (V_I > V_{DD}) . . . . . 18 mA
Output clamp current: I_{OK} (V_O < 0) . . . . . –50 mA
I_{OK} (V_O > V_{DD}) . . . . . 50 mA
Package thermal impedance, θ_{JA} (see Note 4) . . . . . 95°C/W
Maximum power dissipation at T_A = 55°C (in still air) (see Note 5) . . . . . 1.0 W
Operating free-air temperature range, T_A . . . . . –0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 3. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
4. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for the through-hole packages, which use a trace length of zero. The absolute maximum power dissipation allowed at T_A = 55°C (in still air) is 1.0 W.
5. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING
DL	1.3 W	10.7 mW/°C	0.85 W

‡ This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$) and uses a board-mounted device at 95°C/W.

recommended operating conditions (see Notes 4 and 5)

		MIN	NOM†	MAX	UNIT
Supply voltages, V_{DD}	3.3 V	3.135		3.465	V
High-level input voltage, V_{IH}	$\overline{PCI\_Stop}$, $\overline{LDT\_Stop}$, PCI/$\overline{LDT\_SEL}$, $\overline{24/48\_SEL}$, FS0, FS1, FS2, SPREAD	2		V_{DD} +0.3	V
	SDATA, SCLK (see Note 6)	2.0		V_{DD} +0.3	
	XIN	2.0		V_{DD} +0.3	
Low-level input voltage, V_{IL}	$\overline{PCI\_Stop}$, $\overline{LDT\_Stop}$, PCI/$\overline{LDT\_SEL}$, $\overline{24/48\_SEL}$, FS0, FS1, FS2, SPREAD	–0.3		0.8	V
	SDATA, SCLK (see Note 6)	–0.3		1.08	
	XIN	–0.3		0.5	
Input Voltage, V_I	$\overline{PCI\_Stop}$, $\overline{LDT\_Stop}$, PCI/$\overline{LDT\_SEL}$, $\overline{24/48\_SEL}$, FS0, FS1, FS2, SPREAD	–0.3		V_{DD} +0.3	V
	SDATA, SCLK (see Note 6)	–0.3		V_{DD} +0.3	
High-level output current, I_{OH}	CPU			–18	mA
	USB, FDC, REF			–12	
	PCI, LDT			–12	
Low-level output current, I_{OL}	CPU			18	mA
	USB, FDC, REF			9	
	PCI, LDT			9	
	SDATA			4	
Input resistance to V_{DD}, R_I	$\overline{PCI\_Stop}$, $\overline{LDT\_Stop}$, PCI/$\overline{LDT\_SEL}$, $\overline{24/48\_SEL}$, FS0, FS1, FS2, SPREAD	100		220	kΩ
	SDATA, SCLK	100		220	
Reference frequency, $f_{(XIN)}$‡	PLL BY–PASS MODE	0		200	MHz
Crystal frequency, $f_{(XTAL)}$§	NORMAL MODE	10	14.31818	16	MHz
SCLK frequency, $f_{(SCLK)}$¶				100	kHz
Bus free time, $t_{(BUS)}$¶		4.7			µs
START setup time, $t_{su(START)}$¶		4.7			µs
START hold time, $t_{h(START)}$¶		4.0			µs
SCLK low pulse duration, $t_{w(SCLL)}$¶		4.7			µs
SCLK high pulse duration, $t_{w(SCLH)}$¶		4.0			µs
SDATA input rise time, $t_{r(SDATA)}$¶				1000	ns
SDATA input fall time, $t_{f(SDATA)}$¶				300	ns
SDATA setup time, $t_{su(SDATA)}$¶		250			ns
SDATA hold time, th(SDATA)		5			ns
STOP setup time, $t_{su(STOP)}$¶		4			µs
Operating free–air temperature, T_A		0		70	°C

† All typical values are measured at their respective nominal V_{DD}.
‡ Reference frequency is a test clock driven on the XIN input during the device test mode and normal mode. In test mode, XIN can be driven externally up to $f_{(XIN)}$ = 0 MHz to 200 MHz. If XIN is driven externally, XOUT is floating.
§ This is a fundamental crystal with f_O = 14.31818 MHz and 18 pF load in a parallel resonance application (Pierce-type oscillator)
¶ This conforms to SMBus Specification, Version 1.1.

NOTES: 4. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for the through-hole packages, which use a trace length of zero. The absolute maximum power dissipation allowed at T_A = 55°C (in still air) is 1.0 W.
5. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.
6. The CMOS-level inputs fall within these limits: V_{IH}min = 0.7 × V_{DD} and V_{IL}max = 0.3 × V_{DD}.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		V_{DD} = 3.135 V,	I_I = –18 mA		–0.7	–1.2	V
I_{IH}	High-level input current	XIN	V_{DD} = 3.465 V,	V_I = 2.0		2.5		µA
		$\overline{PCI/LDT\_SEL}$, $\overline{PCI\_Stop}$, $\overline{LDT\_Stop}$, SPREAD	V_{DD} = 3.465 V,	$V_I = V_{DD}$			5	
		FS0, FS1, FS2, $\overline{24/48\_SEL}$	V_{DD} = 3.465 V,	$V_I = V_{DD}$			5	
		SDATA, SCLK	V_{DD} = 3.465 V,	$V_I = V_{DD}$			5	
I_{IL}‡	Low-level input current	XIN	V_{DD} = 3.465 V,	V_I = GND		–1.5		mA
		$\overline{PCI/LDT\_SEL}$, $\overline{PCI\_Stop}$, $\overline{LDT\_Stop}$, SPREAD	V_{DD} = 3.465 V,	V_I = GND			–50	µA
		FS0, FS1, FS2, $\overline{24/48\_SEL}$	V_{DD} = 3.465 V,	V_I = GND			–50	
		SDATA, SCLK	V_{DD} = 3.465 V,	V_I = GND			–50	
I_{OZ}	High-impedance-state output current		V_{DD} = 3.465 V,	$V_O = V_{DD}$ or GND			±5	µA
I_{OZ}	High-impedance-state output current, SDATA		V_{DD} = 3.465 V,	$V_O = V_{DD}$			5	µA
I_{DD}	Static supply current	All outputs open,	All outputs = low or high, TEST MODE,	V_{DD} = 3.465 V			4.5	mA
I_{DD}	Dynamic supply current	SSC = ON/OFF, C_L = MAX, LDT = 66 MHz, CPU outputs: TEST LOAD All others loaded with corresponding load capacitance only.	CPU = 166 MHz,	V_{DD} = 3.465 V			180	mA
			CPU = 200 MHz,	V_{DD} = 3.465 V			185	
		All outputs disabled (LOW)	CPU =166 MHz/ 200 MHz, V_{DD} = 3.465 V			45	55	
$I_{DD(Z)}$	High-impedance-state supply current	All outputs open, and outputs are in 3-state	CPU = 200 MHz,	V_{DD} = 3.465 V		38	50	mA
C_I	Input capacitance to GND		V_{DD} = 3.3 V	$V_I = V_{DD}$ or GND		2.3	2.7	pF
XIN, XOUT				V_I = 1.5 V	27	29	31	pF
C_{XTAL}	Cryatal terminal capacitance (see Note 7)		V_{DD} = 3.3 V,	V_I = 1.5 V		15		pF

† All typical values are measured at their respective nominal V_{DD}.
‡ I_{IL} is caused by internal pullup resistors.
NOTE 7: This is the corresponding electrical capacitive load for the crystal in this oscillator application (Pierce-type oscillator). Parasitic pin-to-pin capacitance = 2 pF.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

CPU (200/166/133/100 MHz)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	Unit
V_{OH}	High-level output voltage		V_{DD} = MIN to MAX,	I_{OH} = –1 mA	V_{DD} – 0.1			V
			V_{DD} = 3.135 V,	I_{OH} = –18 mA	2.3			
V_{OL}	Low-level output voltage		V_{DD} = MIN to MAX,	I_{OL} = 1 mA			0.05	V
			V_{DD} = 3.135 V,	I_{OL} = 18 mA			0.6	
I_{OH}	High-level output current		V_{DD} = 3.465 V,	V_O = 2.0 V		–43		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V	–27	–43	–56	
			V_{DD} = 3.135 V,	V_O = 2.735 V		–14		
I_{OL}	Low-level output current		V_{DD} = 3.465 V,	V_O = 0.8 V		32		mA
			V_{DD} = 3.3 V,	V_O = 1.55 V	29	41	52	
			V_{DD} = 3.135 V,	V_O = 0.4 V		17		
C_O	Output capacitance		V_{DD} = 3.3 V,	V_O = V_{DD} or GND		2.7	3.0	pF
Z_O	Output impedance	High state	V_O = 0.5 V_{DD},	Z_O = V_O/I_{OH}	25	40	55	Ω
		Low state	V_O = 0.5 V_{DD},	Z_O = V_O/I_{OL}	25	40	55	

† All typical values are measured at their nominal V_{DD} values.

REF (14.318 MHz)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	Unit
V_{OH}	High-level output voltage		V_{DD} = MIN to MAX,	I_{OH} = –1 mA	V_{DD} – 0.1			V
			V_{DD} = 3.135 V,	I_{OH} = –12 mA	2.5			
V_{OL}	Low-level output voltage		V_{DD} = MIN to MAX,	I_{OL} = 1 mA			0.1	V
			V_{DD} = 3.135 V,	I_{OL} = 9 mA			0.4	
I_{OH}	High-level output current		V_{DD} = 3.465 V,	V_O = 2.0 V		–46		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V	–29	–47	–61	
			V_{DD} = 3.135 V,	V_O = 2.735 V		–15		
I_{OL}	Low-level output current		V_{DD} = 3.465 V,	V_O = 0.8 V		33		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V	30	42	52	
			V_{DD} = 3.135 V,	V_O = 0.4 V		17		
C_O	Output capacitance		V_{DD} = 3.3 V,	V_O = V_{DD} or GND		3.2	3.7	pF
Z_O	Output impedance	High state	V_O = 0.5 V_{DD},	Z_O = V_O/I_{OH}	22	35	52	Ω
		Low state	V_O = 0.5 V_{DD},	Z_O = V_O/I_{OL}	22	35	52	

† All typical values are measured at their nominal V_{DD}.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

USB (48 MHz), FDC (24 MHz or 48 MHz)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	Unit
V_{OH}	High-level output voltage		V_{DD} = MIN to MAX,	I_{OH} = –1 mA	V_{DD} – 0.1			V
			V_{DD} = 3.135 V,	I_{OH} = –16 mA	2.4			
V_{OL}	Low-level output voltage		V_{DD} = MIN to MAX,	I_{OL} = 1 mA			0.1	V
			V_{DD} = 3.135 V,	I_{OL} = 9 mA			0.4	
I_{OH}	High-level output current		V_{DD} = 3.465 V,	V_O = 2.0 V		–46		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V	–29	–47	–61	
			V_{DD} = 3.135 V,	V_O = 2.735 V		–15		
I_{OL}	Low-level output current		V_{DD} = 3.465 V,	V_O = 0.8 V		33		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V	30	42	52	
			V_{DD} = 3.135 V,	V_O = 0.4 V		17		
C_O	Output capacitance		V_{DD} = 3.3 V,	V_O = V_{DD} or GND		3.2	3.7	pF
Z_O	Output impedance	High state	V_O = 0.5 V_{DD},	Z_O = V_O/I_{OH}	22	35	52	Ω
		Low state	V_O = 0.5 V_{DD},	Z_O = V_O/I_{OL}	22	35	52	

† All typical values are measured at their nominal V_{DD}.

PCI, PCI_F (33 MHz) and LDT (33 MHz or 66 MHz)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	Unit
V_{OH}	High-level output voltage		V_{DD} = MIN to MAX,	I_{OH} = –1 mA	V_{DD} – 0.1			V
			V_{DD} = 3.135 V,	I_{OH} = –12 mA	2.4			
V_{OL}	Low-level output voltage		V_{DD} = MIN to MAX,	I_{OL} = 1 mA			0.1	V
			V_{DD} = 3.135 V,	I_{OL} = 9 mA			0.4	
I_{OH}	High-level output current		V_{DD} = 3.465 V,	V_O = 2.V		–71		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V	–40	–71	–97	
			V_{DD} = 3.135 V,	V_O = 2.735 V		–23		
I_{OL}	Low-level output current		V_{DD} = 3.465 V,	V_O = 0.8 V		38		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V	37	71	100	
			V_{DD} = 3.135 V,	V_O = 0.4 V		19		
C_O	Output capacitance		V_{DD} = 3.3 V,	V_O = V_{DD} or GND		3.2	3.7	pF
Z_O	Output impedance	High state	V_O = 0.5 V_{DD},	Z_O = V_O/I_{OH}	12	25	37	Ω
		Low state	V_O = 0.5 V_{DD},	Z_O = V_O/I_{OL}	22	25	37	

† All typical values are measured at their nominal V_{DD}.

SDATA

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	Unit
V_{OL}	Low-level output voltage, SDATA	V_{DD} = MIN to MAX,	I_{OL} = 4 mA			0.2	V
		V_{DD} = 3.135 V,	I_{OL} = 6 mA			0.4	
I_{OL}	Low-level output current, SDATA	V_{DD} = 3.465 V,	V_O = 0.8 V		35		mA
		V_{DD} = 3.3 V,	V_O = 1.65 V	33	46	57	
		V_{DD} = 3.135 V,	V_O = 0.4 V		19		
Z_O	Output impedance, low state	0.5 V_{DD},	Z_O = V_O/I_{OL}	25	36	47	Ω
$C_{I/O}$	Input/output capacitance, SDATA	V_{DD} = 3.3 V,	V_O = V_{DD} or GND		4.5	5.1	pF

† All typical values are measured at their nominal V_{DD}.

switching characteristics, V_{DD} = MIN to MAX, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$v_{(over)}/v_{(under)}$	Overshoot/undershoot	All clocks			±0.7	
$t_{su(disable)}$	$\overline{\text{PCI\_Stop}}\downarrow$ or $\overline{\text{LDT\_Stop}}\downarrow$ to PCI_F↑	$f_{(PCI/LDT)}$ = 33/66 MHz to disable PCI/LDT in next cycle (PCI/LDT = low)	10			ns
$t_{h(disable)}$	$\overline{\text{PCI\_Stop}}\downarrow$ or $\overline{\text{LDT\_Stop}}\downarrow$ to PCI_F↑	$f_{(PCI/LDT)}$ = 33/66 MHz to disable PCI/LDT in next cycle (PCI/LDT = low)	0			ns
$t_{su(enable)}$	$\overline{\text{PCI\_Stop}}\uparrow$ or $\overline{\text{LDT\_Stop}}\uparrow$ to PCI_F↑	$f_{(PCI/LDT)}$ = 33/66 MHz to enable PCI/LDT in next cycle (PCI/LDT = high)	10			ns
$t_{h(enable)}$	$\overline{\text{PCI\_Stop}}\uparrow$ or $\overline{\text{LDT\_Stop}}\uparrow$ to PCI_F↑	$f_{(PCI/LDT)}$ = 33/66 MHz to enable PCI/LDT in next cycle (PCI/LDT = high)	0			ns
SSC(midx)	SSC spread amount	$f_{(CPU)}$ = 100 MHz to 200 MHz		–0.5		%
$f_{(mod)}$	SSC modulation frequency	$f_{(CPU)}$ = 100 MHz to 200 MHz		31.4		kHz
t_{stab}	Stabilization time†	FS0, FS1, FS2 or SMBus update		0.03	3	ms
		After power up		0.13	3	

† Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at XIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics tables are not applicable. Stabilization time is defined as the time from when V_{DD} achieves its nominal operating level until the output frequency is stable and operating within specification.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 70°C

CPU, C_L = 10 pF, R_L = Test Load

PARAMETER		FROM (INPUT)		TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	Unit
t_{pd1}	Propagation delay time	XIN		CPUx	$f_{(XIN)} \geq 1$ MHz, TEST MODE	3.5		15	ns
t_{pd2}	Propagation delay time	SCLK ↑		CPUx	Test mode		18		ns
t_c	CPU clock period†				$f_{(CPU)}$ = 100 MHz	10.0		10.1	ns
					$f_{(CPU)}$ = 133 MHz	7.5		7.60	
					$f_{(CPU)}$ = 166 MHz	6.0		6.08	
					$f_{(CPU)}$ = 200 MHz	5.0		5.1	
$t_{jit(cc)}$	Cycle to cycle jitter	Synthesizer mode			$f_{(CPU)}$ = 100 to 200 MHz			160	ps
odc	Duty cycle				$f_{(CPU)}$ = 100 to 200 MHz	47		53	%
$t_{jit(acc)}$	Accumulated jitter, SSC = ON, see Note 8				f(CPU) = 100 to 200 MHz	–150		150	ps
tsk(b)	CPU bank skew ↑ edges	CPUx		CPUx	$f_{(CPU)}$ = 100 to 200 MHz			70	ps
$tsk_{(ow)}$	CPU x-point to ↑ edges Output skew window time independent (3.3 V)	↑ CPU 200 MHz	CPUx	PCIx	$f_{(PCI)}$ = 33.3 MHz			500	ps
			CPUx	LDTx	$f_{(LDT)}$ = 66.7 MHz			500	
	CPU x-point to ↑ edges Output skew window time variant skew	↑ CPU 200 MHz	CPUx	PCIx	$f_{(PCI)}$ = 33.3 MHz			200	
			CPUx	LDTx	$f_{(LDT)}$ = 66.7 MHz			200	
t_r	Rise time	Test load at the ac coupling node including CPU load.			V_{ref} = 0V ±400 mV differential measured	100 2.5		300 8.0	ps V/ns
t_f	Fall time					100 2.5		300 8.0	ps V/ns
v_r	Edge rate rising edge (maintained during total transition)	Test load at the ac coupling node including CPU load.			V_{ref} = 0V ±400 mV differential measured	2.0		8.0	V/ns
v_f	Edge rate falling edge (maintained during total transition)	Test load at ac coupling node				2.0		8.0	V/ns

† All typical values are measured at their nominal V_{DD} values.

NOTE 8: Accumulated jitter is the sum of individual consecutive cycle-to-cycle jitter reads added for a at least 32 µs (one SSC modulation period). The limit corresponds to the w/c cumulative shortest and longest jitter number found during evaluation time.

CPU C_L = 10 pF, R_L = Test Load (see Note 9) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	Unit
VOD	Differential output voltage	Test load at ac coupling node including CPU load.	CPU to $\overline{\text{CPU}}$	1.3		1.7	V
ΔV_{OD_DC}	Change in dc differential output voltage		CPU to $\overline{\text{CPU}}$	–15		15	mV
V_{OCM}	Common mode voltage		CPU to $\overline{\text{CPU}}$	1.3		1.4	V
ΔV_{OCM}	Change in common mode voltage		CPU to $\overline{\text{CPU}}$	–10		10	mV
V_{CM_AC}	Common mode voltages (MIN/ MAX)		CPU to $\overline{\text{CPU}}$	1.0		1.4	V
v_{cross}	Absolute cross point voltages crosspoint (low and high)	Test load at ac coupling node including CPU load.	CPU and $\overline{\text{CPU}}$	1.0		1.2	V
Δv_{cross}	Variation of V_{cross}, rising edge		At ↑ CPU(x…n), (max-min)			90	mV
$T\Delta v_{cross}$	Total variation V_{cross}, all edges		At ↑ or ↓ CPU(x…n),(max-min)			140	mV

† The average over any 1-µs period of time is greater than the minimum specified period

NOTES: 9. This specification does not include variations caused by K8 input resistor network or K8 $_{VDD}$ voltage variations. The common mode voltage is calculated as: $(V_{OH}+V_{OL})/2$. See the measurement information section for details.

10. This applies also to $\overline{\text{CPU}}$ outputs.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 70°C (continued)

USB, FDC (48 MHz) and FDC (24 MHz), C_L = 20 pF, (USB) R_L = 500 Ω

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd1}	Propagation delay time	XIN	USB/FDC	$f_{(XIN)} \geq$ 1 MHz, TEST MODE	2		15	ns
t_{pd2}	Propagation delay time	SCLK↑	USB/FDC	TEST MODE		18		ns
t_c	USB/FDC (48 MHz) clock period‡			$f_{(USB/FDC)}$ = 48 MHz	20.8		20.84	ns
	FDC (24 MHz) clock period‡			$f_{(FDC)}$ = 24 MHz	41.6		41.68	
$t_{jit(cc)}$	Cycle to cycle jitter FDC (48 MHz) or FDC (24 MHz)			$f_{(CPU)}$ = 100 to 200 MHz			200	ps
	Cycle to cycle jitter USB (48 MHz), FDC=24 or 48 MHz			$f_{(CPU)}$ = 100 to 200 MHz			180	
$t_{jit(acc)}$	Accumulated jitter USB (48 MHz), FDC=24 or 48 MHz			$f_{(CPU)}$ = 100 to 200 MHz	–160		160	ps
odc	Duty cycle USB/FDC			$f_{(USB/FDC)}$ = 48 MHz	45		55	%
	Duty cycle FDC			$f_{(FDC)}$ = 24 MHz	45		55	
$t_{sk(ow)}$	USB to FDC skew ↑ edges time-independent and time-variant skew combined	USB	FDC	$f_{(USB/FDC)}$ = 48 MHz			500	ps
				$f_{(USB/FDC)}$ = 48 / 24 MHz			500	
$t_{sk(p)}$	USB/FDC pulse skew	USB/FDC	USB/FDC	$f_{(USB/FDC)}$ = 48 MHz	2		6.5	ns
	FDC pulse skew	FDC	FDC	$f_{(FDC)}$ = 24 MHz	2		6.5	
$t_{w(H)}$	Pulse duration, high			$f_{(USB/FDC)}$ = 48 MHz	7.5			ns
				$f_{(FDC)}$ = 24 MHz	18			
$t_{w(L)}$	Pulse duration, low			$f_{(USB/FDC)}$ = 48 MHz	11.5			ns
				$f_{(FDC)}$ = 24 MHz	22			
t_r	Rise time		USB	V_{ref} = 20% to 80% of V_O	1.1		2.5	ns
			FDC		2		0.7	V/ns
t_f	Fall time		USB	V_{ref} = 20% to 80% of V_O	1.1		2.5	ns
			FDC		2		0.7	V/ns
v_r	Edge rate, rising edge (maintained during total transition)		USB	V_{ref} = 20% to 60% of V_{DD}	0.25		1.1	V/ns
			FDC					
v_f	Edge rate falling edge (maintained during total transition)		USB	V_{ref} = 20% to 60% of V^{DD}	0.25		1.1	V/ns
			FDC					

† All typical values are measured at their nominal V_{DD} values.
‡ The average over any 1-µs period of time is greater than the minimum specified period

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 70°C (continued)

PCI, LDT (33 MHz), PCI_F and LDT (66 MHz), C_L = 30 pF, R_L = 500 Ω

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd1}	Propagation delay time	XIN	PCIx,LDT	$f_{(XIN)} \geq 1$ MHz, Test mode	2.0		15	ns
t_{pd2}	Propagation delay time	SCLK↑	PCIx, LDT	Test mode		18		ns
t_c	PCI clock period†			$f_{(PCI)}$ = 33.3 MHz	29.95		30.3	ns
				$f_{(LDT)}$ = 66.7MHz	14.95		15.15	
$t_{jit(cc)}$	Cycle-to-cycle jitter PCI/LDT (33 MHz), LDT (33 MHz)			$f_{(CPU)}$ = 100 to 200 MHz			170	ps
	Cycle-to-cycle jitter LDT (66 MHz), PCI (33 MHz)						290	
$t_{jit(acc)}$	Accumulated jitter PCI/LDT (33 MHz), LDT (66 MHz)			$f_{(CPU)}$ = 100 to 200 MHz	–300		300	ps
odc	Duty cycle PCI (33 MHz)			$f_{(PCI)}$ = 33.3 MHz	45		55	%
t_{dc}	Duty cycle LDT (66MHz)			$f_{(LDT)}$ = 66.7 MHz	45		55	%
$t_{sk(b)}$	PCI bank skew ↑ edges time-independent (3.3 V)	PCIx	PCIx	$f_{(PCI)}$ = 33.3 MHz			500	ps
	PCI bank skew ↑ edges time-variant skew						200	
$t_{sk(ow)}$	↑ edges to CPU x-point time-independent (3.3 V)	PCIn	CPUx	$f_{(PCI)}$ = 33.3 MHz			500	ps
	↑ edges to CPU x-point time-variant skew						200	
$t_{sk(b)}$	LDT bank skew ↑ edges time-independent (3.3 V)	LDTx	LDTx	$f_{(LDT)}$ = 66.7 MHz			500	ps
	LDT bank skew ↑ edges time-variant skew						200	
$t_{sk(ow)}$	↑ edges to CPU x-point time-independent (3.3 V)	LDTx	CPUx	$f_{(LDT)}$ = 66.7 MHz			500	ps
	↑ edges to CPU x-point tim-variant skew	LDTx	CPUx				200	

† All typical values are measured at their nominal V_{DD} values.
‡ The average over any 1-μs period of time is greater than the minimum specified period

PCI, LDT (33 MHz), PCI_F and LDT (66 MHz), C_L = 30 pF, R_L = 500 Ω (continued)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	Unit
$t_{sk(ow)}$	↑ edges to LDT time independent (3.3 V)	PCIx	LDTx	$f_{(PCI/LDT)}$ = 33.3 MHz			500	ps
	↑ edges to LDT time variant skew	PCIx	LDTx				200	
	↑ edges to LDT time independent (3.3)	PCIx	LDTx	$f_{(PCI/LDT)}$= 33.3 MHz/66.7 MHz			500	
	↑ edges to LDT time variant skew	PCIx	LDTx				200	
$t_{sk(p)}$	PCI pulse skew	PCIn	PCIn	$f_{(PCI)}$ = 33.3 MHz	1.5		3.7	ns
	LDT pulse skew	LDTn	LDTn	$f_{(LDT)}$ = 66.7 MHz	1.4		3.6	
$t_{w(H)}$	Pulse duration, high PCI (33 MHz)			$f_{(PCI)}$ = 33.3 MHz	13.6			ns
	Pulse duration, high LDT (66 MHz)			$f_{(LDT)}$ = 66.7 MHz	6.2			
$t_{w(L)}$	Pulse duration, low PCI (33 MHz)			$f_{(PCI)}$ = 33.3 MHz	16.0			ns
	Pulse duration, low LDT (66 MHz)			$f_{(LDT)}$ = 66.7 MHz	8.4			
t_r	Rise time PCI/LDT (33 MHz), LDT (66 MHz)			V_{ref} = 20% to 80% of V_O	0.7 2.9		1.6 1.2	ns V/ns
t_f	Fall time PCI/LDT (33 MHz), LDT (66 MHz)			V_{ref} = 20% to 80% of V_O	0.6 3.5		1.6 1.2	ns V/ns
v_r	Edge rate rising edge (maintained during total transition)			V_{ref} = 20% to 60% of V_{DD}	0.3		1.7	V/ns
v_f					0.4		1.7	

† All typical values are measured at their nominal V_{DD} values.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 70°C (continued)

REF, C_L = 20 pF, R_L = 500 Ω

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd1}	Propagation delay time	XIN	REF	$f_{(XIN)} \geq$ 1 MHz, TEST MODE	2		10.0	ns
t_{pd2}	Propagation delay time	SCLK↑	REF	TEST MODE		18		ns
t_c	REF clock period†			$f_{(REF)}$ = 14.318 MHz	69.8		69.84	ns
$t_{jit(cc)}$	Cycle to cycle jitter			$f_{(CPU)}$ = 100 to 200 MHz			250	ps
$t_{jit(acc)}$	Accumulated jitter			$f_{(CPU)}$ = 100 to 200 MHz	–200		200	ps
$t_{jit(\varnothing)}$	Phase jitter			$f_{(CPU)}$ = 100 to 200 MHz			300	ps
odc	Duty cycle			$f_{(REF)}$ = 14.318 MHz	45		55	%
$t_{sk(b)}$	REF bank skew ↑ edges	REFx	REFx	$f_{(REF)}$ = 14.318 MHz			500	ps
$t_{sk(p)}$	REF pulse skew	REF	REF	$f_{(REF)}$ = 14.318 MHz	2		5.8	ps
$t_{w(H)}$	Pulse duration width, high			$f_{(REF)}$ = 14.318 MHz	27			ns
$t_{w(L)}$	Pulse duration width, low			$f_{(REF)}$ = 14.318 MHz	32			ns
t_r	Rise time			V_{ref} = 20% to 80% of Vo	1.1 2		2.7 0.7	ns V/ns
t_f	Fall time			V_{ref} = 20% to 80% of Vo	1.1 2		2.7 0.7	ns V/ns
v_r	Edge rate rising edge (maintained during total transition)			V_{ref} = 20% to 60% of VDD	0.25		1.1	V/ns
v_f	Edge rate falling edge (maintained during total transition)				0.25		1.1	V/ns

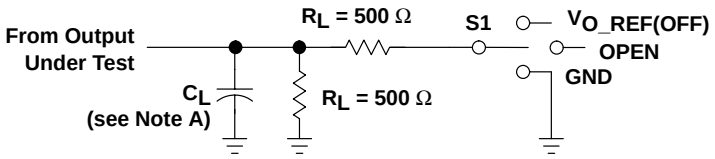
† All typical values are measured at their nominal V_{DD} values.
‡ The average over any 1-μs period of time is greater than the minimum specified period

SDATA, C_L = 10 pF to 400 pF, R_L = 1 kΩ

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time‡	SCLK↓	Data acknnowledge	See Figure 6	0.375		2	μs
t_{PLH}	Propagation delay time‡	SCLK↓	Data valid	See Figure 6	0.375		2	μs
t_{PHL}	Propagation delay time‡	SCLK↓	Data valid	See Figure 6	0.375		2	μs
t_f	Fall time			C_L = 10 pF		86	250	ns
				C_L = 400 pF		115	250	

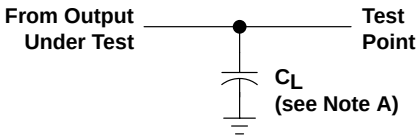
† All typical values are measured at their nominal V_{DD} values.
‡ This is a digital controlled delay. It equals to 6 REF clock cycles plus the internal gate delay (20 ns).

PARAMETER MEASUREMENT INFORMATION

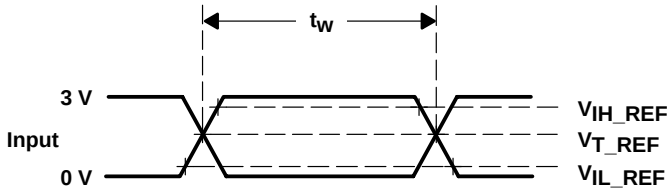


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$V_{O\_REF(OFF)}$
t_{PHZ}/t_{PZH}	GND

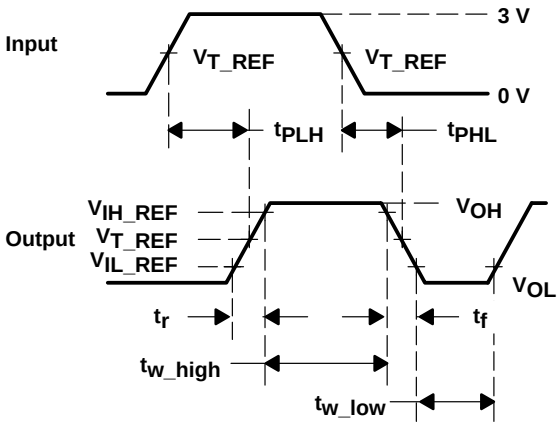
LOAD CIRCUIT for t_{pd} and t_{sk}



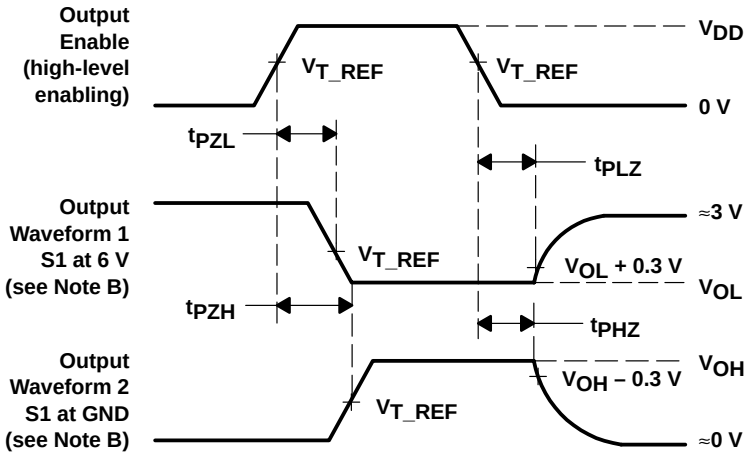
LOAD CIRCUIT FOR t_r and t_f



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



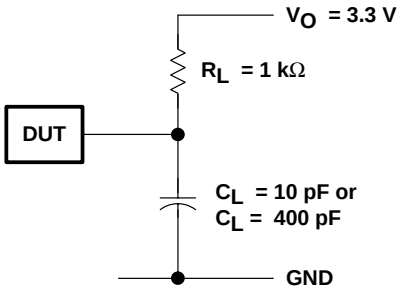
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance. C_L = 10 pF (CPU), C_L = 20 pF (USB, FDC, REF), C_L = 30 pF (PCI, LDC)
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 14.318 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

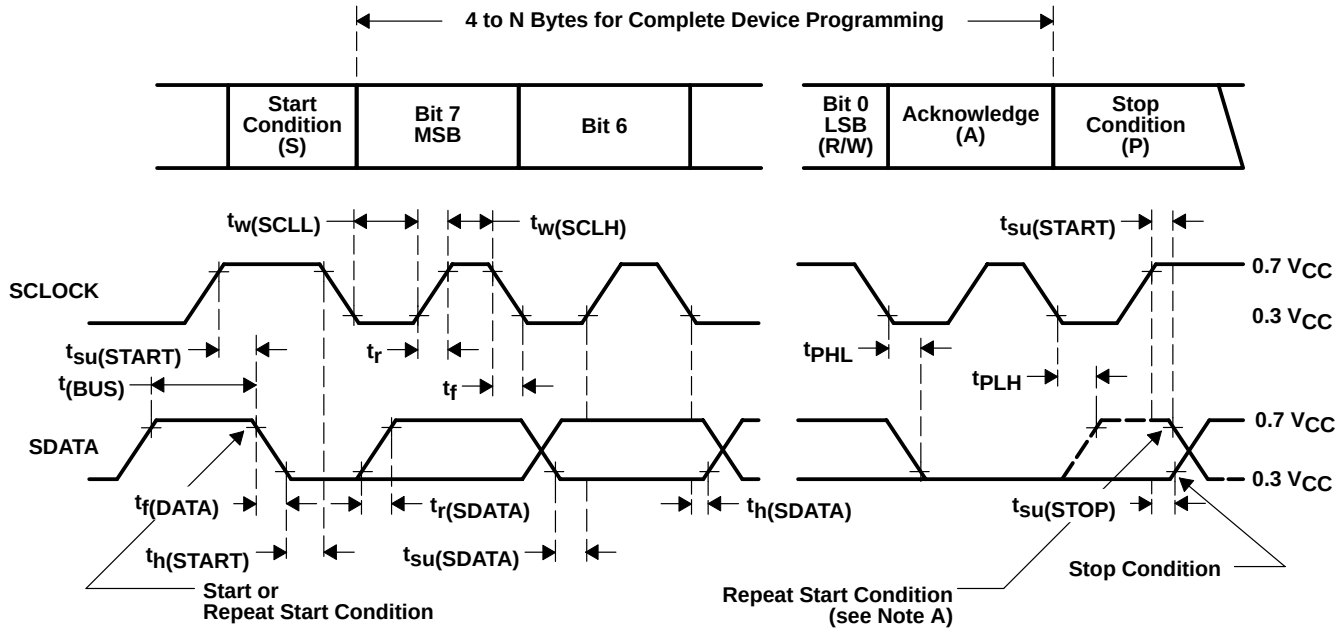
PARAMETER		3.3-V INTERFACE	UNIT
V_{IH_REF}	High-level reference voltage	2.4	V
V_{IL_REF}	Low-level reference voltage	0.4	V
V_{T_REF}	Input threshold reference voltage	1.5	V
V_{O_REF}	Off-state reference voltage	6	V

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



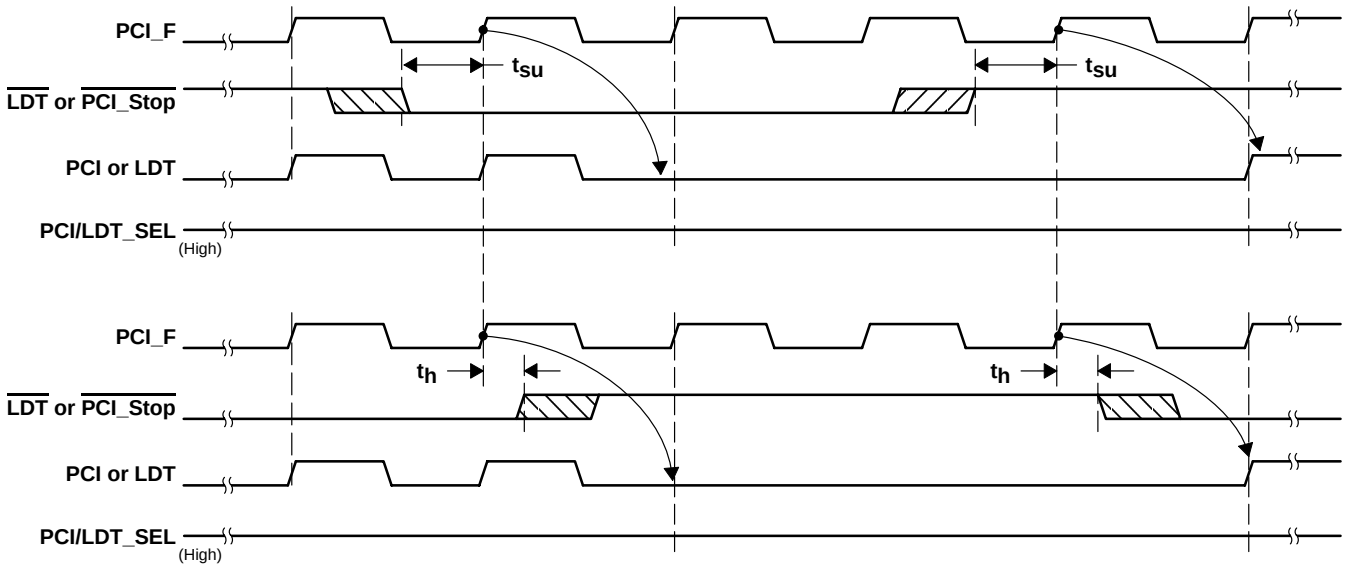
VOLTAGE WAVEFORMS

NOTE A: The repeat start condition is supported, but not clock stretching.

BYTE	DESCRIPTION
1	SMBus address
2	Command (dummy value, ignored)
3	Byte count
4	SMBus data byte 0
5 – N	SMBus data byte 1 – N

Figure 6. Propagation Delay Times, t_r and t_f

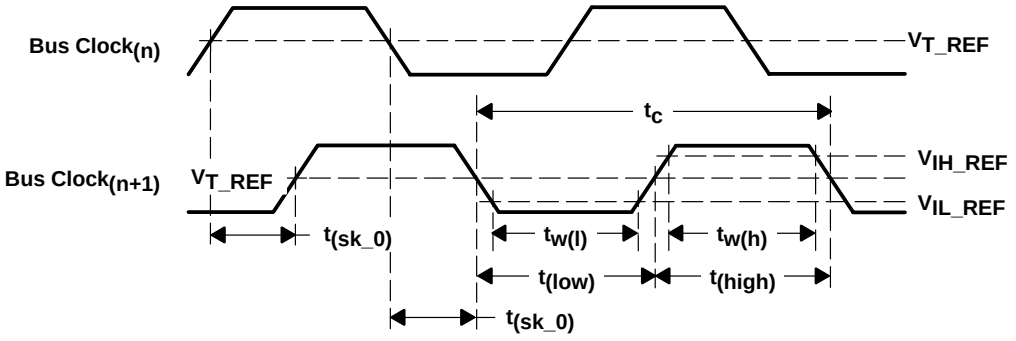
PARAMETER MEASUREMENT INFORMATION



NOTE: Assertion and deassertion of $\overline{\text{PCI\_STOP}}$ or $\overline{\text{LDT\_STOP}}$ maintain signals duty cycle.
$t_{su(disable)}$ is the time at which no pulse exists in following period.
$t_{su(enable)}$ is the time at which a pulse exists in following period.

Figure 7. $\overline{\text{PCI\_Stop}}$ or $\overline{\text{LDT\_Stop}}$ ↓↑ to PCI (LDT)

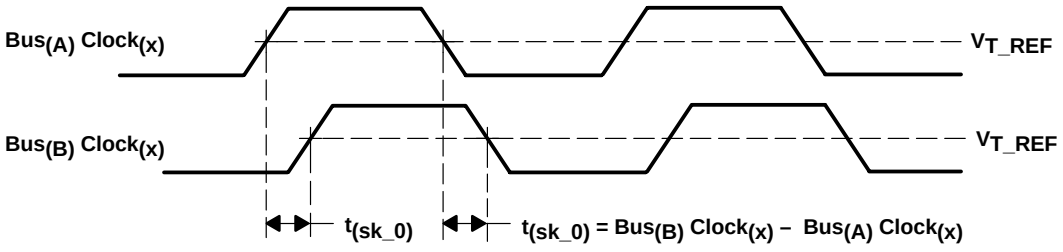
PARAMETER MEASUREMENT INFORMATION



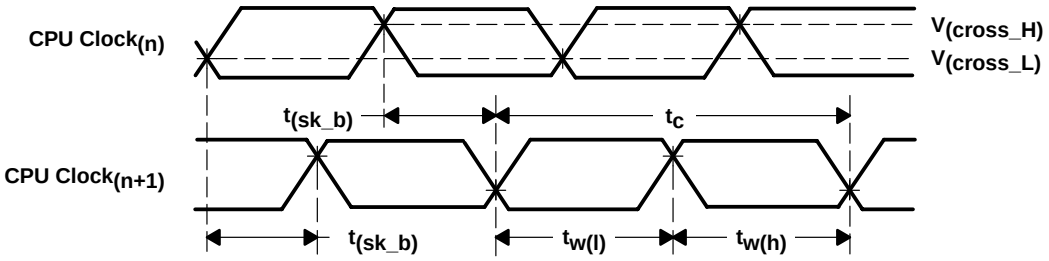
$$t_{(sk\_p)} = \left| t_{w(l)} - t_{w(h)} \right|$$

$$\text{Duty Cycle} = \frac{t_{(\text{low or high})}}{t_c} \times 100$$

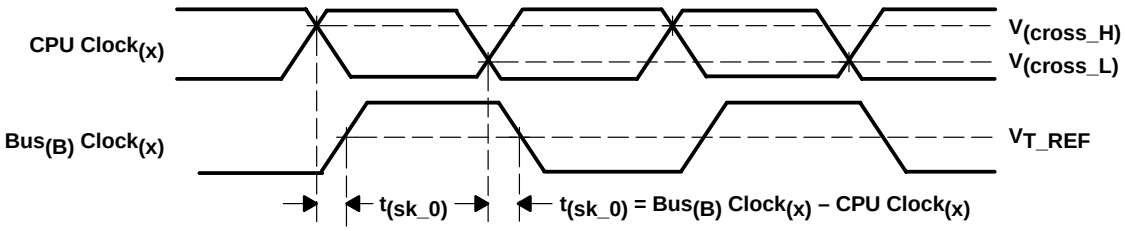
Refer to Figure 4



a) Single-Ended Outputs



$$\text{Duty Cycle} = \frac{t_{w(\text{Low or High})}}{t_c} \quad \text{x } 100$$



b) Differential Ouput

Figure 8. Waveforms for Calculation of Skew and Offset

PARAMETER MEASUREMENT INFORMATION

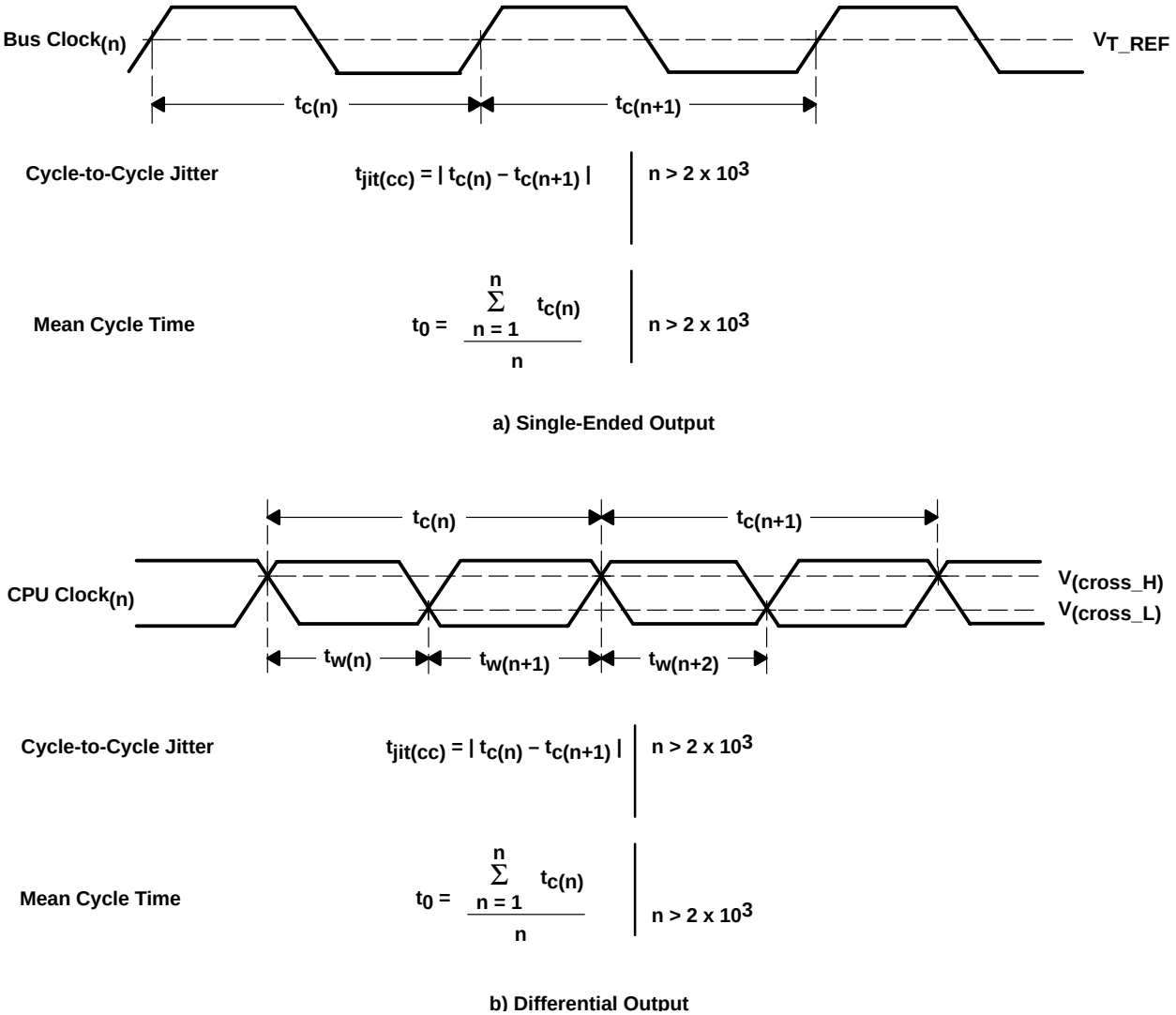


Figure 9. Waveforms for Calculation of Jitter

PARAMETER MEASUREMENT INFORMATION

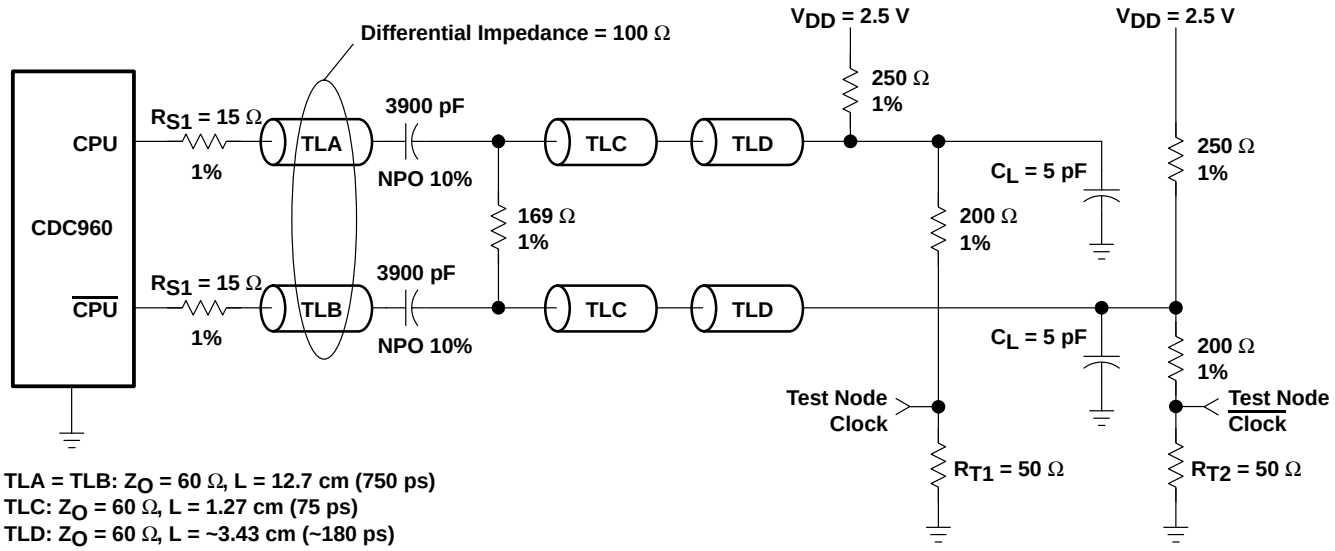


Figure 10. Load Circuit and Voltage Waveforms for CPU Bus

correction for measurements at 50 Ω nodes

Voltage levels and readings are scaled for the voltage divider 200 Ω to 50 Ω versus all reads and reference levels must be multiplied/divided by the fixed scale of five.

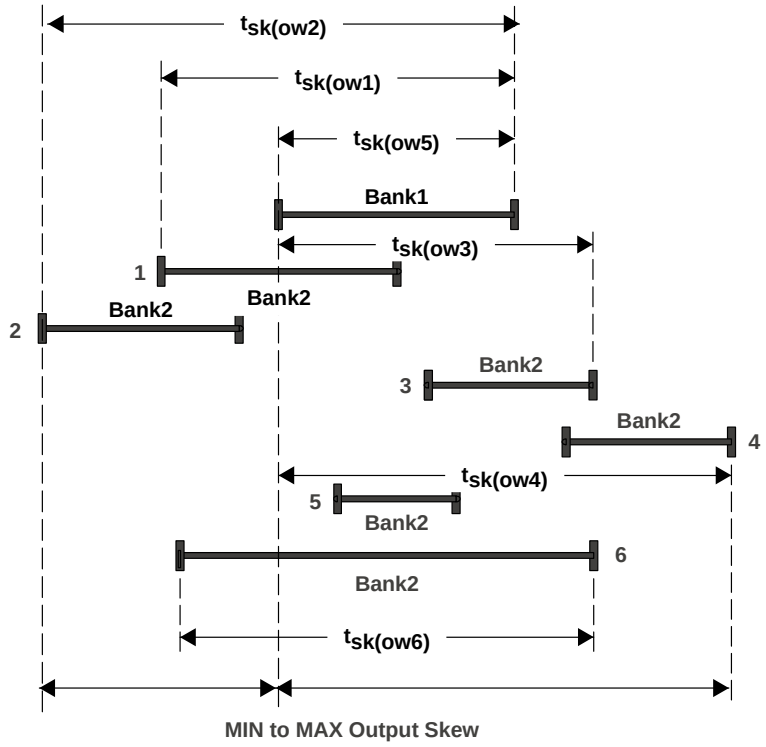
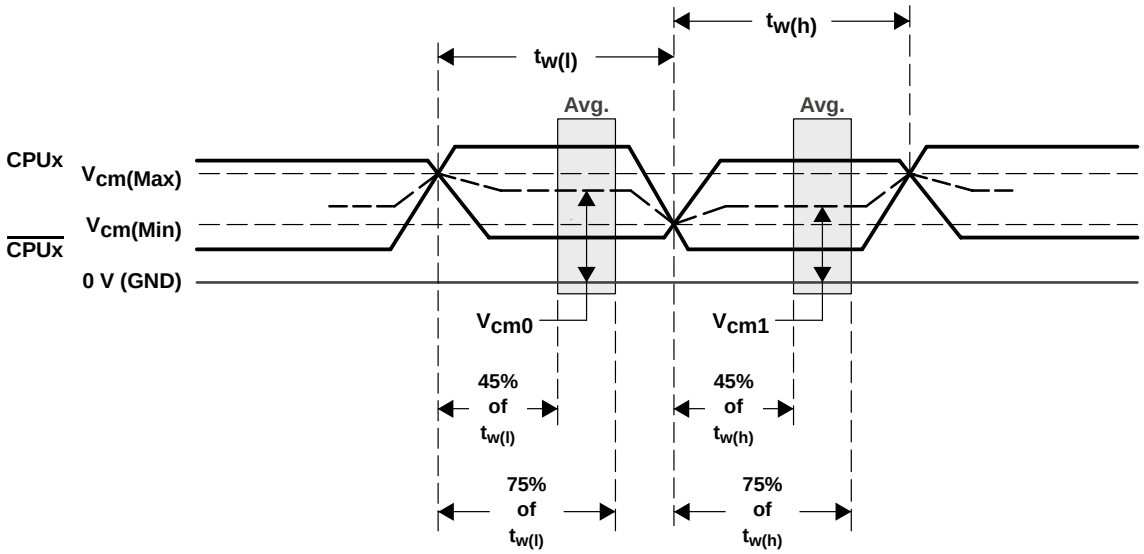


Figure 11. Bank and Output Skew; $t_{sk(owx)}$: Output Skew Window and MIN-to-MAX Phase

PARAMETER MEASUREMENT INFORMATION

The common mode voltage is measured single-ended and is the result of the following calculation:

$Vocm_{(t)} = [Vo(CPUT)_{(t)} + Vo(CPUC)_{(t)}]/2$



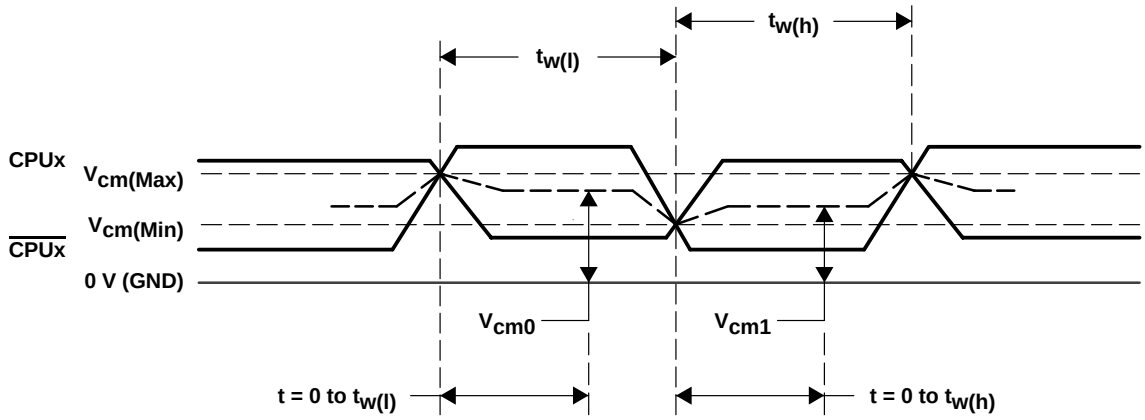
V_{cm0} is calculated from the average of Vocm within 45%–75% (region without switching noise) of the pulse while CPUx is in the LOW state.

V_{cm1} is calculated from the average of Vocm within 45%–75% (region without switching noise) of the pulse while CPUx is in the HIGH state.

$V_{ocm} = (V_{cm0} + V_{cm1})/2$

$\Delta V_{ocm} = V_{cm0} - V_{cm1}$

a) Static



$\Delta V_{ocm(t)} = MAX (V_{cm0(t)}) - MIN (V_{cm1(t)})$ and
$\Delta V_{ocm(t)} = MIN (V_{cm0(t)}) - MAX (V_{cm1(t)})$

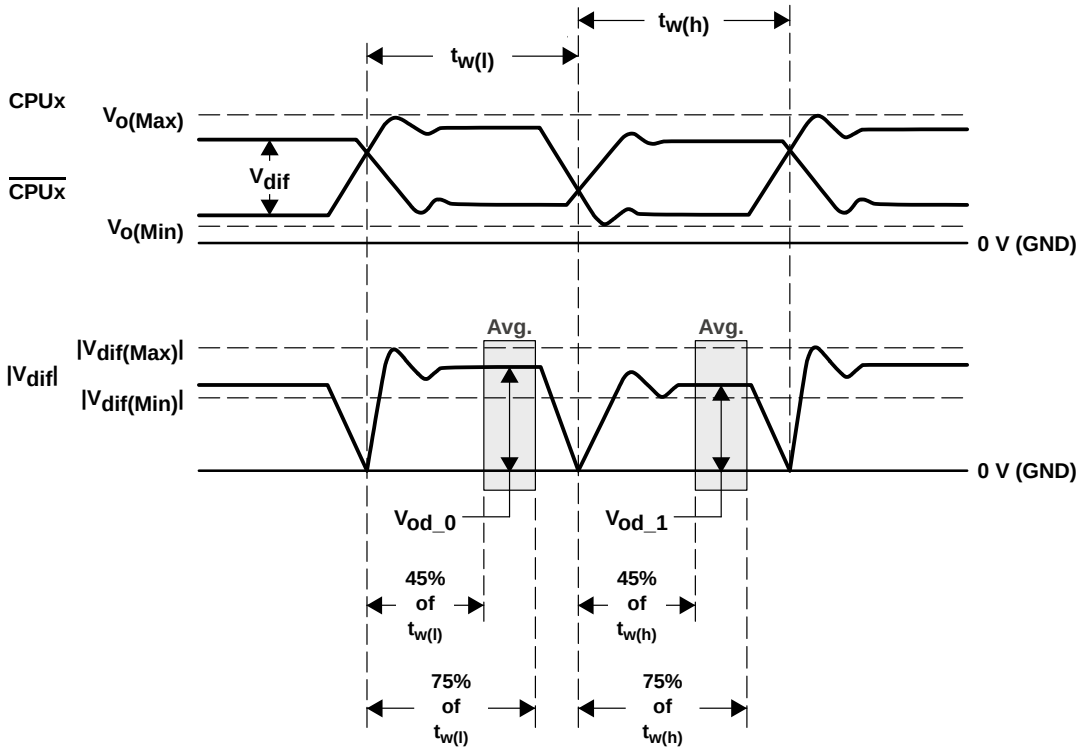
b) Dynamic

Figure 12. Common Mode Voltage

PARAMETER MEASUREMENT INFORMATION

The differential voltage is measured single-ended and is the result of the following calculation:

$Vod_{(t)} = Vo(CPUx)_{(t)} – Vo(\overline{CPUx})_{(t)}$



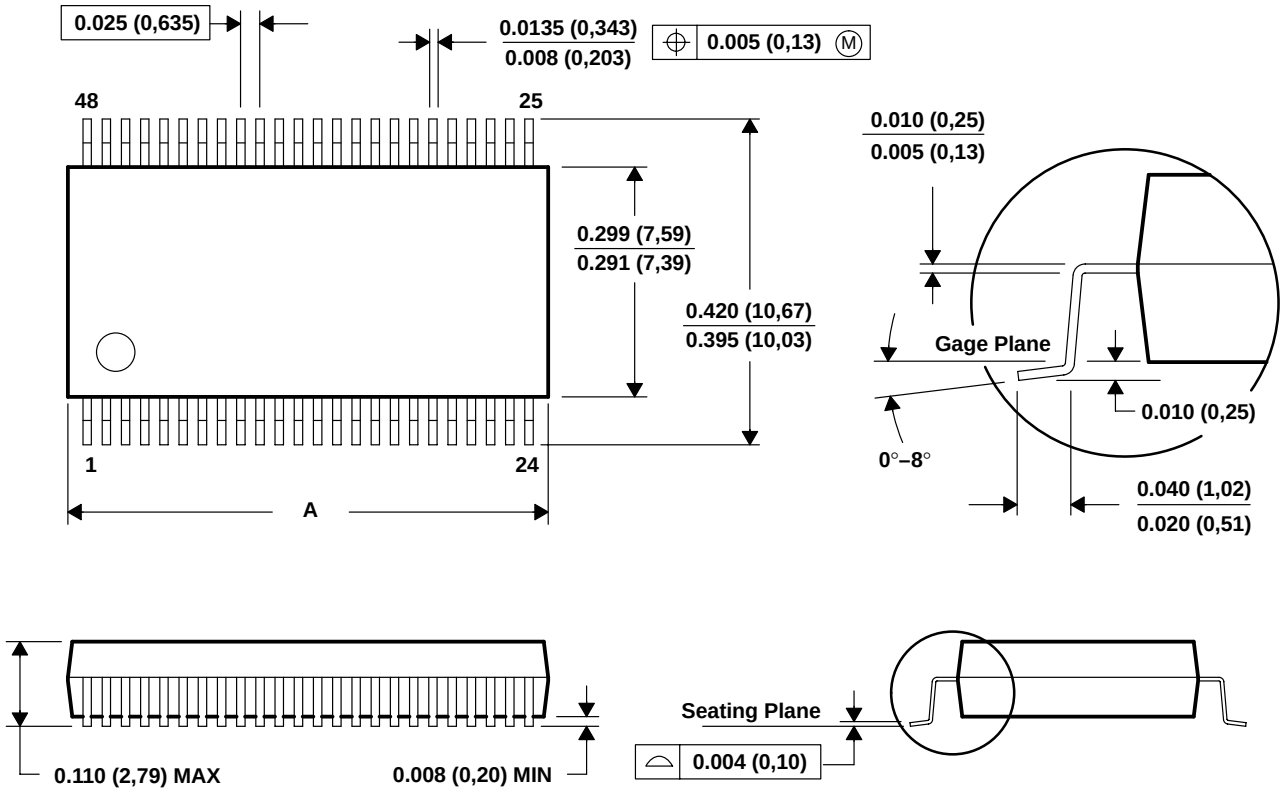
Vod_0 is calculated from the average of Vod within 45%–75% (region without switching noise) of the pulse while CPUx is in the LOW state.
Vod_1 is calculated from the average of Vod within 45%–75% (region without switching noise) of the pulse while CPUx is in the HIGH state.
Vod = (Vod_0 + Vod_1/2
∆Vod_DC = Vod_0 – Vod_1
∆Vod_AC = |Vdif(max0| – |Vdif(min)|

Figure 13. Differential Output Voltage

MECHANICAL DATA

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

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