ISL88021, ISL88022

Triple Voltage Monitor with Adjustable Power-On-Reset and Undervoltage/Overvoltage Monitoring Capability

FN8226
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The ISL88021 and ISL88022 family of devices are customizable triple voltage-monitoring supervisors that assert a reset if any of the monitored voltages becomes non-compliant. They offer popular functions such as Power-On-Reset timing control with both RESET and $\overline{\text{RESET}}$ outputs, Supply Voltage Supervision, both under or overvoltage detection, and Manual Reset assertion. By offering these features in a small 8 Ld MSOP package, the ISL88021 and ISL88022 can lower system cost, reduce board space requirements and increase the reliability of systems.

Applying a voltage to V_{DD} activates the Power-On-Reset circuit which holds $\overline{\text{RESET}}$ low for an adjustable period of time. This allows the power supply and system oscillator to stabilize before the processor can execute code.

Low V_{DD} detection circuitry protects the user's system from low voltage conditions, resetting the system when V_{DD} falls below its minimum preset voltage threshold V_{TH1}. Reset remains asserted until V_{DD} returns to its proper operating level and stabilizes. Two additional voltage monitoring inputs, V2MON (preset) and V3MON (adjustable), monitor other supplies to provide reliable system operation.

The ISL88021 V3MON input monitors for undervoltage (UV) conditions whereas the ISL88022 V3MON input allows monitoring for overvoltage (OV) conditions. The monitored voltage on V3MON on either device is compared via a resistor divider to a 600mV internal reference. Hence, any voltage more or less positive than this reference can be accurately monitored to meet specific system level requirements or to fine-tune the threshold for applications requiring higher precision.

These devices also let users increase the Power-On-Reset time-out delay by connecting a capacitor between C_{POR} and ground. This lengthens the period of an internal clock counter thereby increasing the time between voltage compliance and reset outputs signaling.

A manual reset input provides debounce circuitry for minimum reset component count.

Features

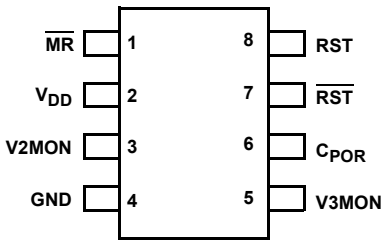
- Triple Voltage Monitor and Reset Assertion
- Low V_{DD} Detection and Reset Assertion
  - Adjustable Reset Threshold Voltages
  - 0.6V ±6mV Over -40°C to +85°C
  - Reset Signal Valid to V_{DD} = 1V
- 140ms Minimum Reset Pulse Delay that is Customizable Using an External Capacitor
- Both RST and $\overline{\text{RST}}$ Outputs Available
- Undervoltage/Overvoltage Monitoring Capability
- Low 20µA Consumption
- Small 8 Ld MSOP Package
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Process Control Systems
- Intelligent Instruments
- Embedded Control Systems
- Computer Systems
- Portable/Battery-Powered Equipment
- Multi-Voltage Systems

Pinout

ISL88021, ISL88022
(8 LD MSOP)
TOP VIEW



Ordering Information (See Notes)

PART NUMBER	PART MARKING	V_{DD} V_{TRIP1}	V2MO V_{TRIP2}	V3MON TYPE	PACKAGE
ISL88021IU8FAZ	**ANM**	**3.09V**	**1.69V**	**UV**	**8 Ld MSOP**
ISL88021IU8FCZ	**ANL**	**3.09V**	**2.32V**	**UV**	**8 Ld MSOP**
ISL88021IU8FEZ		3.09V	2.92V	UV	8 Ld MSOP
ISL88021IU8FFZ		3.09V	3.09V	UV	8 Ld MSOP
ISL88021IU8HAZ		4.64V	1.69V	UV	8 Ld MSOP
ISL88021IU8HCZ		4.64V	2.32V	UV	8 Ld MSOP
ISL88021IU8HEZ	**ANK**	**4.64V**	**2.92V**	**UV**	**8 Ld MSOP**
ISL88021IU8HFZ	**ANJ**	**4.64V**	**3.09V**	**UV**	**8 Ld MSOP**
ISL88022IU8FAZ	**ANQ**	**3.09V**	**1.69V**	**OV**	**8 Ld MSOP**
ISL88022IU8FCZ	**ANP**	**3.09V**	**2.32V**	**OV**	**8 Ld MSOP**
ISL88022IU8FEZ		3.09V	2.92V	OV	8 Ld MSOP
ISL88022IU8FFZ		3.09V	3.09V	OV	8 Ld MSOP

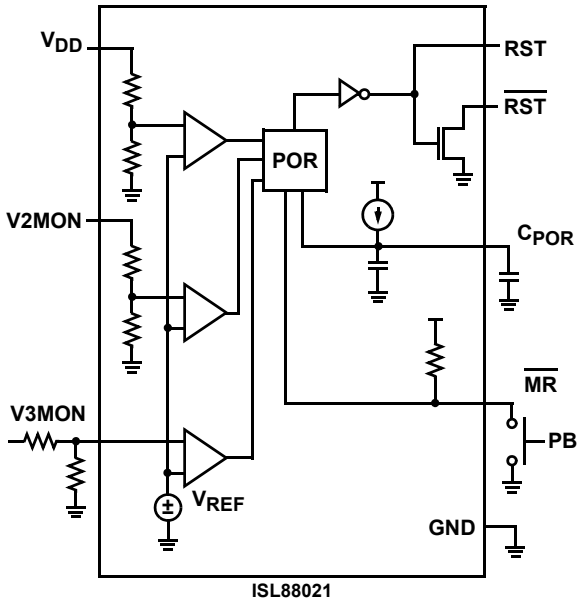
Ordering Information (See Notes) (Continued)

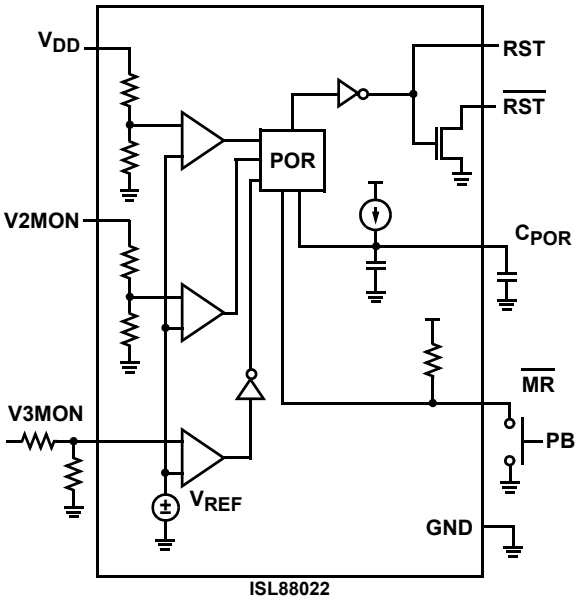
PART NUMBER	PART MARKING	V_{DD} V_{TRIP1}	V2MO V_{TRIP2}	V3MON TYPE	PACKAGE
ISL88022IU8HAZ		4.64V	1.69V	OV	8 Ld MSOP
ISL88022IU8HCZ		4.64V	2.32V	OV	8 Ld MSOP
ISL88022IU8HEZ	**ANO**	**4.64V**	**2.92V**	**OV**	**8 Ld MSOP**
ISL88022IU8HFZ	**ANN**	**4.64V**	**3.09V**	**OV**	**8 Ld MSOP**

NOTES:

1. Standard versions are shown in bold. For non-standard versions, please contact factory for availability.
2. Add “-TK” suffix for Tape and Reel.
3. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagrams





Pin Descriptions

ISL88021	ISL88022	NAME	FUNCTION
1	1	$\overline{MR}$	Active-Low Open Drain Manual Reset Input
2	2	V_{DD}	Power Supply Input
3	3	V2MON	Second Undervoltage Monitor Input
4	4	GND	Ground
5		V3MON	Undervoltage Monitor Input
	5	V3MON	Overvoltage Monitor Input
6	6	C_{POR}	Set Power-On-Reset Timeout Delay
7	7	$\overline{RST}$	Active-Low Open Drain Reset Output
8	8	RST	Active-High Push-Pull Reset Output

Absolute Maximum Ratings

Temperature Under Bias . . . . . .-40°C to +85°C
Voltage on Any Pin with Respect to GND . . . . . .-1.0V to +7V
D.C. Output Current. 5mA

Recommended Operating Conditions

Industrial . . . . . .-40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
MSOP Package	145

Maximum Junction Temperature (Plastic Package) . . . . . .+150°C
Maximum Storage Temperature Range. . . . . .-65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .+300°C
(MSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage Range		2.0		5.5	V
I_{DD1}	V_{DD} Supply Current	V_{DD} = 5.0V		12.5	15	µA
I_{DD2}	V2MON Input Current	V2MON = 3.3V		5.5	6	µA
I_{DDA}	V3MON Input Current	V3MON = 1.0V		19	100	nA
VOLTAGE THRESHOLDS						
V_{TH1}	Fixed Voltage Trip Point for V_{DD}	ISL88021/22IU8**H**xZ	4.565	4.649	4.733	V
		ISL88021/22IU8**F**xZ	3.029	3.085	3.141	V
$V_{TH1HYST}$	Hysteresis of V_{TH1}	V_{TH1} = 4.64V		46		mV
		V_{TH1} = 3.09V		37		mV
V_{TH2}	Fixed Voltage Trip Point for V2MON	ISL88021/22IU8x**F**Z	3.034	3.090	3.146	V
		ISL88021/22IU8x**E**Z	2.894	2.947	3.000	V
		ISL88021/22IU8x**C**Z	2.290	2.332	2.374	V
		ISL88021/22IU8x**A**Z	1.660	1.690	1.720	V
$V_{TH2HYST}$	Hysteresis of V_{TH2}	V_{TH2} = 3.09V		37		mV
		V_{TH2} = 2.92V		29		mV
		V_{TH2} = 2.32V		23		mV
		V_{TH2} = 2.19V		22		mV
		V_{TH2} = 1.69V		17		mV
V_{TH3}	V3MON Threshold Voltage	V_{TH} for V3MON on ISL88021	0.594	0.605	0.616	V
		V_{TH} for V3MON on ISL88022	0.587	0.595	0.603	V
$V_{REFHYST}$	Hysteresis Voltage			3		mV
RESET						
V_{OL}	Reset Output Voltage Low	$V_{DD} \geq$ 3.3V, Sinking 2.5mA		0.05	0.40	V
		V_{DD} < 3.3V, Sinking 1.5mA		0.05	0.40	V
V_{OH}	RST Output Voltage High	$V_{DD} \geq$ 3.3V, Sourcing 2.5mA	V_{DD}-0.6	V_{DD}-0.4		V
		V_{DD} < 3.3V, Sourcing 1.5mA	V_{DD}-0.6	V_{DD}-0.4		V
t_{RPD}	V_{TH} to Reset Asserted Delay			10		µs
t_{POR}	POR Timeout Delay	C_{POR} is open	140	200		ms
C_{LOAD}	Load Capacitance on Reset Pins			5		pF

Electrical Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MANUAL RESET						
V_{MRL}	$\overline{MR}$ Input Voltage Low				0.8	V
V_{MRH}	$\overline{MR}$ Input Voltage High		V_{DD}-0.6			V
t_{MR}	$\overline{MR}$ Minimum Pulse Width		550			ns
R_{PU}	Internal Pull-Up Resistor			20		kΩ

Functional Description

The ISL88021 and ISL88022 devices incorporate such features as Power-On-Reset control, Supply Voltage Supervision, Undervoltage or Overvoltage Monitoring, and Manual Reset Assertion.

The ISL88021 and ISL88022 devices provide common preset threshold voltages on both V_{DD} and V2MON and for an optional resistor divider network on V3MON to provide custom voltage monitoring of voltages greater than 0.6V. An optional capacitor can be connected between the C_{POR} pin and GND to increase the nominal 200ms t_{POR} delay. Figure 7 illustrates operational functionality with a timing diagram.

Voltage Monitoring

During normal operation, the ISL88021 and ISL88022 monitor the voltage levels on V_{DD}, V2MON and V3MON. The ISL88021 asserts reset if any one of these voltages fall below their respective voltage trip points and in the case of ISL88022 above the voltage trip point on the V3MON input. The reset signal effectively prevents the microprocessor from operating during a power failure, brownout or over voltage condition. This signal remains active until all monitored voltages meet all voltage threshold requirements for the reset time delay period t_{POR}. Note that both RESET and $\overline{RESET}$ signals are provided for design flexibility. Figure 1 illustrates the VDD, V2MON and V3MON input threshold voltages for the various available options.

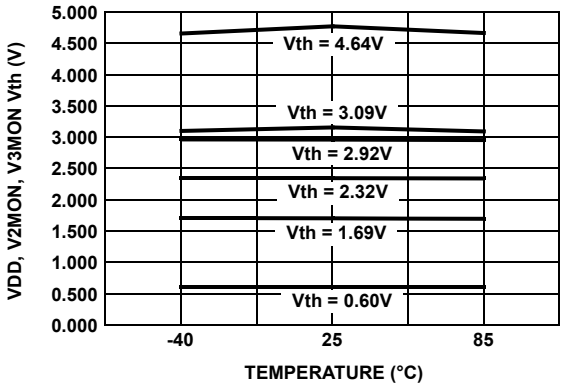


FIGURE 1. VDD, V2MON, V3MON VTH vs TEMP

Power-On-Reset (POR)

Applying power to the ISL88021 and ISL88022 devices activates a POR circuit which holds the $\overline{RESET}$ pin low once V_{DD} > 1V. This signal provides several benefits:

- It prevents the system microprocessor from starting to operate with insufficient voltage.
- It prevents the processor from operating prior to stabilization of the oscillator.
- It ensures that the monitored device is held out of operation until internal registers are properly loaded.
- It allows time for an FPGA to download its configuration prior to initialization of the circuit.

When all of the monitored voltages meet their respective input voltage requirements for the specified reset timeout delay t_{POR}, the POR circuit simultaneously pulls the RST output low and releases the $\overline{RST}$ output to allow the system to begin operation.

Adjusting t_{POR}

On the ISL88021 and ISL88022, users can adjust the Power-On-Reset timeout delay (t_{POR}) to many times the nominal t_{POR}. Figure 2 illustrates the effect of capacitance on the C_{POR} pin to ground, showing changing t_{POR} with a graph normalized to 175ms for an open C_{POR} pin. The maximum recommended capacitance that should be placed on the C_{POR} pin is 50pF. **NOTE:** Care should be taken in PCB layout and capacitor placement in order to eliminate stray capacitance as much as possible, which contributes to t_{POR} error.

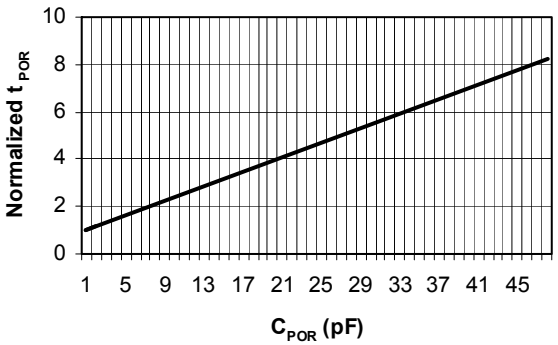


FIGURE 2. NORMALIZED t_{POR} vs C_{POR} GRAPH

Manual Reset

The manual reset input ($\overline{MR}$) allows the user to trigger a reset by using a push-button switch or by signaling that pin low. The $\overline{MR}$ input is an active low debounced input. By connecting a push-button directly from $\overline{MR}$ to ground, the designer adds manual system reset capability. Reset is asserted if the $\overline{MR}$ pin is pulled low to less than 100mV for 1µs or longer while the push-button is closed or a reset is signaled. After $\overline{MR}$ is released, the reset outputs remain asserted for t_{POR}. $\overline{MR}$ input has an internal 20kΩ pull up resistor provided.

Figure 3 illustrates a typical application diagram for either IC showing both reset outputs being used along with both a manual and signalled reset configuration. The V_{DD} and V2MON thresholds are preset whereas the V3MON is capable of UV (ISL88021) or OV (ISL88022) monitoring of a voltage greater than or less than 0.6V, respectively.

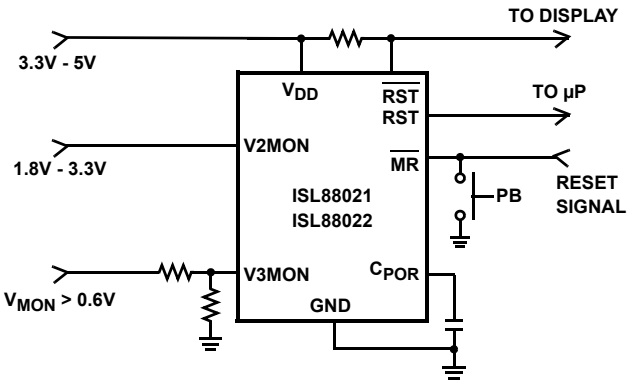


FIGURE 3. TYPICAL APPLICATION DIAGRAM

Application Considerations

Follow good decoupling practices to prevent transients from causing unwanted reset signaling due to switching noises and short duration droops.

When using the C_{POR} pin, reduce layout stray capacitance on this pin to minimize effect on t_{POR} timing. If no PCB C_{POR} pad is patterned, the t_{POR} can be 160ms.

Using the ISL88021_22EVAL1 Platform

The ISL88021_22EVAL1 board is designed to provide both immediate functional assessment and flexibility to the user. Both ICs are the 'HF' variant having a V_{DD} Vth of 4.64V, a V2MON Vth of 3.09V and V3MON Vth of 0.6V. The top IC position is the ISL88021 and is configured to monitor for undervoltage (UV) compliance of a 5V, 3.3V and a 2.5V and signaling the RESET and $\overline{RESET}$ outputs. The bottom position is the ISL88022 variant, which is configured to measure a 3.3V overvoltage (OV) in addition to UV on both the 5V and 3.3V supplies. RESET and $\overline{RESET}$ is asserted for at least t_{POR} when these voltage go out of range. In both cases V3MON interfaces with the monitored supply via a simple resistor divider for comparison to the internal 0.6V reference. A Manual Reset ($\overline{MR}$) input is provided on both ICs and is invoked by pulling this input LOW.

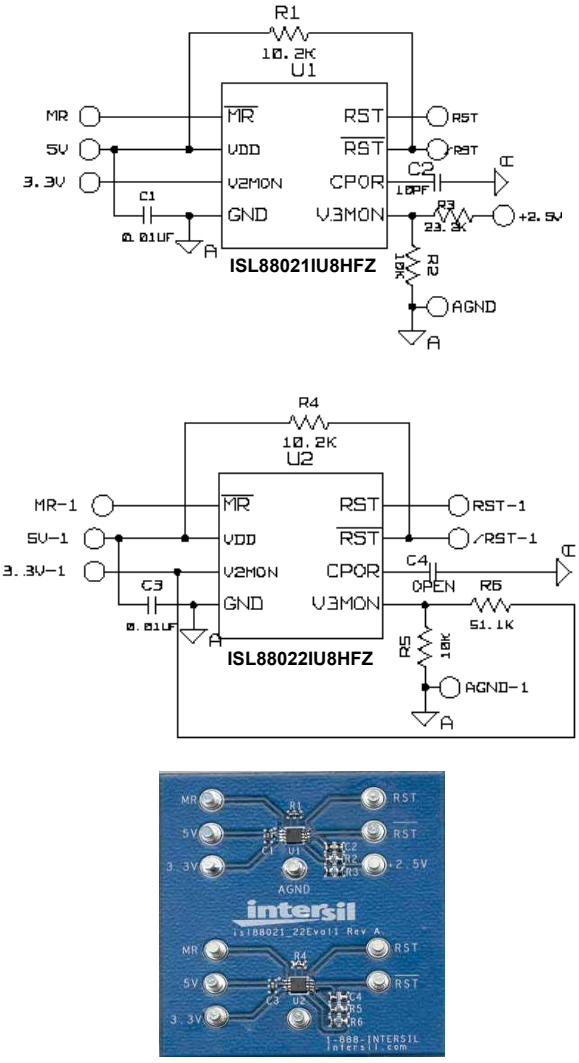


FIGURE 4. ISL88021_22EVAL1 SCHEMATIC AND PHOTO

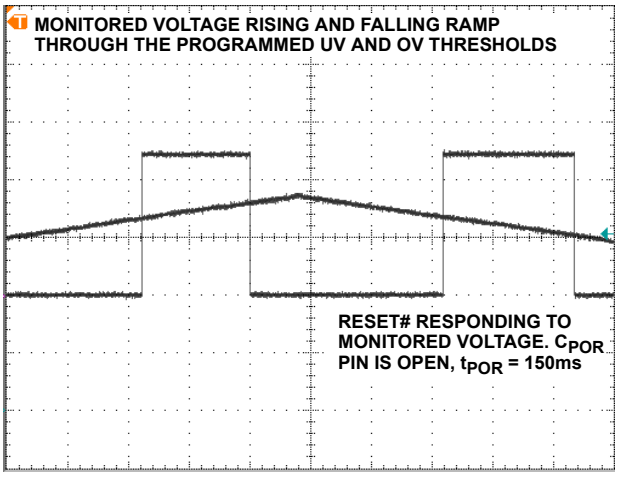


FIGURE 5. ISL88022EVAL1 3.3V UV AND OV DETECTION

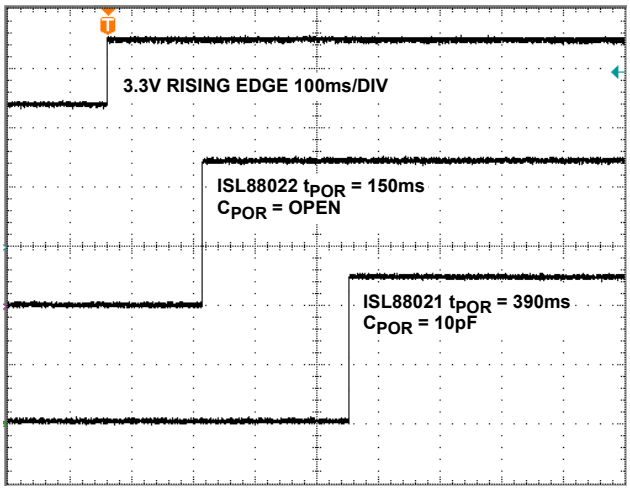


FIGURE 6. ISL88021_22EVAL1 t_{POR} COMPARISON

Operational Timing Diagrams

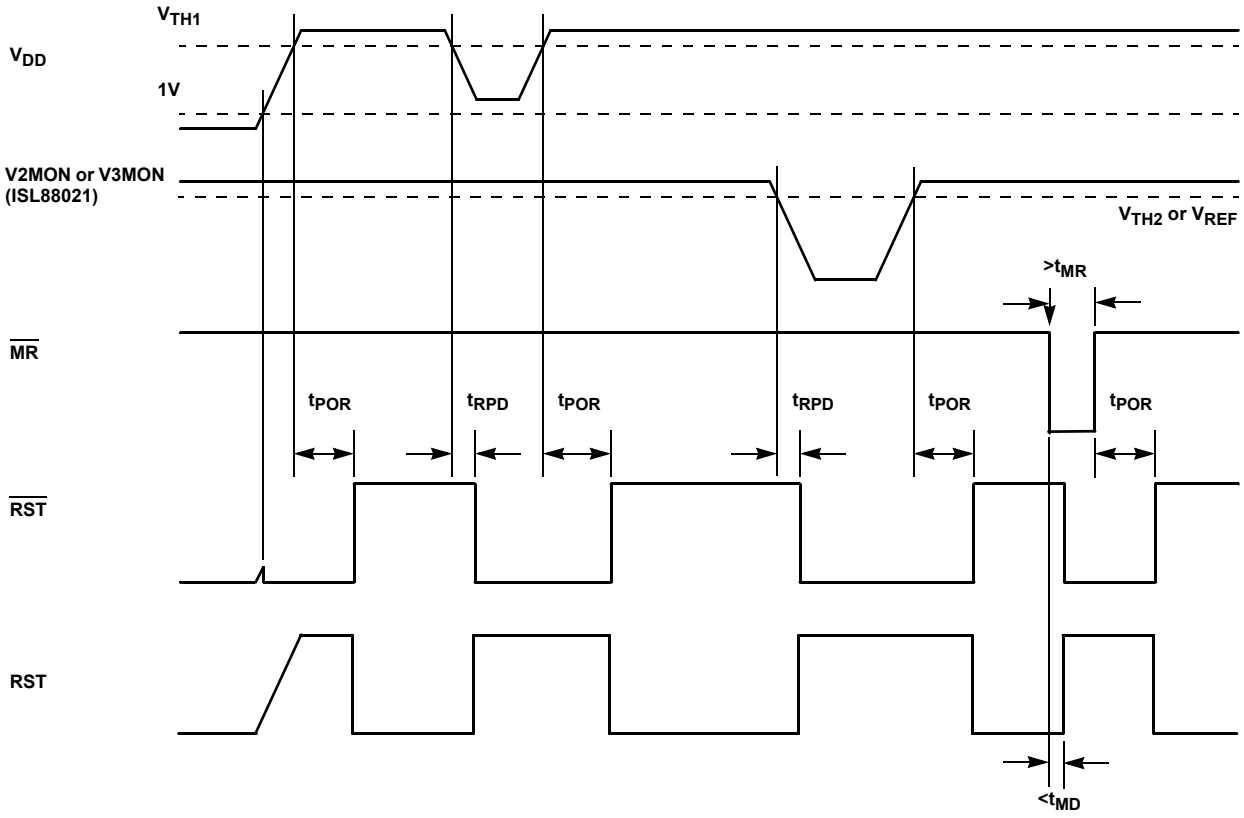


FIGURE 7. ISL88021 AND ISL88022 TIMING DIAGRAM

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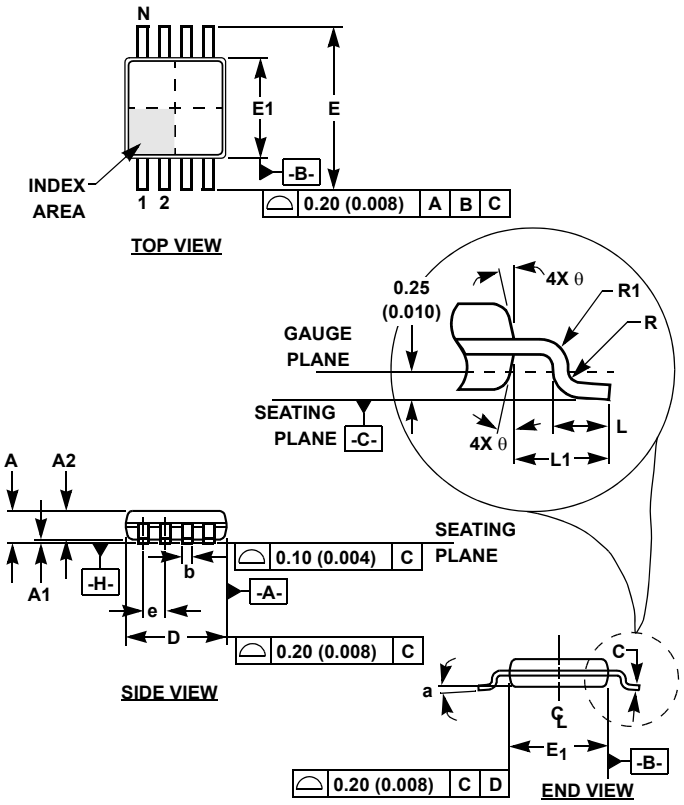
Mini Small Outline Plastic Packages (MSOP)



M8.118 (JEDEC MO-187AA)

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
0	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

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NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.