# PRIMARY CONTROLLER

PRODUCT PREVIEW

- CURRENT-MODE CONTROL PWM
- SWITCHING FREQUENCY UP TO 1MHz
- LOW START-UP CURRENT < 0.5mA
- HIGH-CURRENT OUTPUT DRIVE SUITABLE FOR POWER MOSFET (1A)
- FULLY LATCHED PWM LOGIC WITH DOUBLE PULSE SUPPRESSION
- PROGRAMMABLE DUTY CYCLE
- 100% AND 50% MAXIMUM DUTY CYCLE LIMIT
- PROGRAMMABLE SOFT START
- PRIMARY OVERCURRENT FAULT DETECTION WITH RE-START DELAY
- PWM UVLO WITH HYSTERESIS
- IN/OUT SYNCHRONIZATION
- DISABLE LATCHED
- INTERNAL 100ns LEADING EDGE BLANKING OF CURRENT SENSE
- PACKAGE: DIP16 AND SO16W
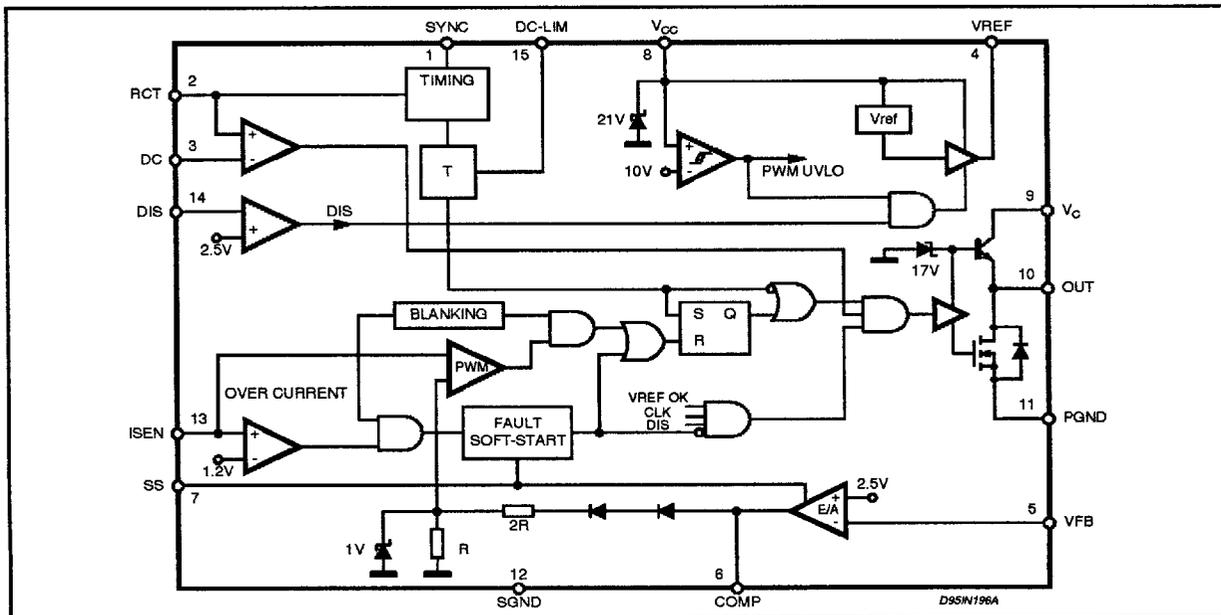
MULTIPOWER BCD TECHNOLOGY
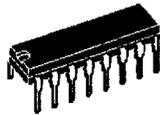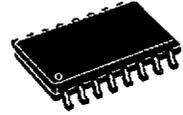
DIP16   SO16W

ORDERING NUMBERS: L4990/L4990A(DIP16)
L4990D/L4990AD (SO16W)

DESCRIPTION

This primary controller I.C., developed in BCD60II technology, has been designed to implement off line or DC-DC power supply applications using a fixed frequency current mode control.

Based on a standard current mode PWM controller this device includes some features as programmable soft start, IN/OUT synchronization, disable (to be used for over voltage protection and for power management), precise maximum Duty Cycle Control, 100ns (typ) leading edge blanking on current sense, pulse by pulse current limit and overcurrent protection with soft start intervention.

BLOCK DIAGRAM

D95IN196A

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage ($I_{CC} < 50mA$) (*)	selflimit	V
I_{OUT}	Output Peak Pulse Current	1.5	A
	Analog Inputs & Outputs (6,7)	-0.3 to 8	V
	Analog Inputs & Outputs (1,2,3,4,5,15,14 13)	-0.3 to 6	V
P_{tot}	Power Dissipation @ $T_{amb} = 70°C$	1	W
T_j	Junction Temperature, Operating Range	-25 to 125	°C
T_{stg}	Storage Temperature, Operating Range	-55 to 150	°C

(*) maximum package power dissipation limits must be observed

PIN CONNECTION


```
SYNC  [ 1        16 ]  N.C.
RCT   [ 2        15 ]  DC-LIM
DC    [ 3        14 ]  DIS
VREF  [ 4        13 ]  ISEN
VFB   [ 5        12 ]  SGND
COMP  [ 6        11 ]  PGND
SS    [ 7        10 ]  OUT
Vcc   [ 8         9 ]  Vc
          D95IN197
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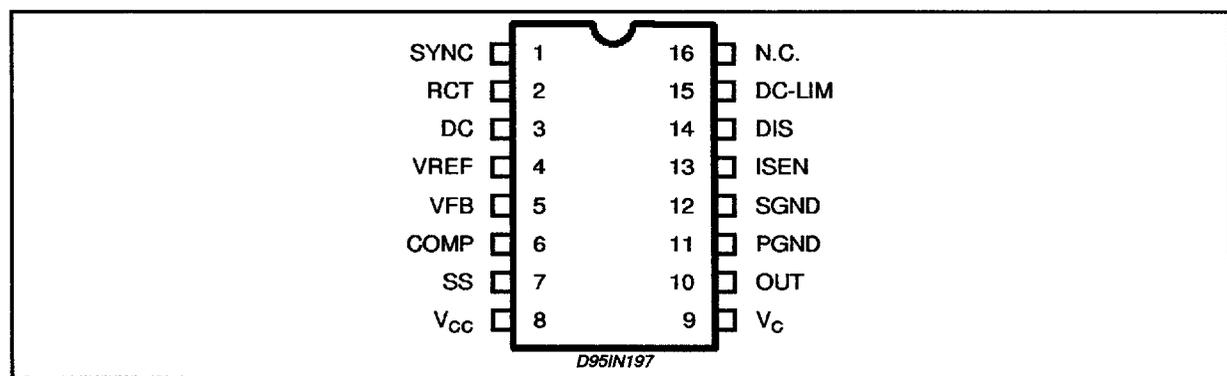
THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j-pins}$	Thermal Resistance Junction -Pins	50	°C/W
$R_{th\ j-amb}$	Thermal Resistance Junction -Ambient	80	°C/W

PIN FUNCTIONS

N.	Name	Function
1	SYNC	Synchronization. A synchronization pulse terminates the PWM cycle and discharge Ct
2	RCT	Oscillator pin for external C_t, R_t components
3	DC	Duty Cycle control
4	VREF	5.0V +/-2% reference voltage
5	VFB	Error Amplifier Inverting input
6	COMP	Error Amplifier Output
7	SS	Soft start pin for external capacitor Css
8	Vcc	Supply for internal "Signal" circuitry
9	V_C	Supply for Power section
10	OUT	High current totem pole output
11	PGND	Power ground
12	SGND	Signal ground
13	ISEN	Current sense
14	DIS	Disable
15	DC-LIM	Connecting this pin to Vref, DC is limited to 50% if it is left floating or grounded no limitation is imposed
16	NC	Not connected

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ELECTRICAL CHARACTERISTICS (V_{CC} = 15V; T_{amb} = 0 to 70°C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
REFERENCE SECTION						
V_O	Output Voltage	T_j = 25°C; I_O = 1mA	4.9	5.0	5.1	V
	Line Regulation	V_{CC} = 12 to 20V		2.0	20	mV
	Load Regulation	I_O = 1 to 20mA		5.0	20	mV
T_S	Temperature Stability			0.4		mV/°C
	Total Variation	Line, Load, Temperature	4.82		5.18	V
I_{OS}	Short Circuit Current	Vref = 0V	30		150	mA
	Power Down/UVLO	V_{CC} = 8.5V; I_{sink} = 0.5mA		0.2	0.5	V
OSCILLATOR SECTION						
	Initial Accuracy	T_j = 25°C; R_T = 4.42KΩ; C_T = 1nF; pin 15 Vref	285	300	315	KHz
	Initial Accuracy	R_T = 4.42KΩ; V_{CC} = 12 to 20V; C_T = 1nF; pin 15 = Vref	279	300	321	KHz
	Initial Accuracy	T_j = 25°C; R_T = 4.42KΩ; C_T = 1nF; pin 15 OPEN	280	295	310	KHz
	Initial Accuracy	R_T = 4.42KΩ; V_{CC} = 12 to 20V; C_T = 1nF; pin 15 OPEN	275	295	315	KHz
	Duty Cycle Accuracy	pin 3 = 0,7V, pin 15 = Vref pin 3 = 0.7V, pin 15 = open			0 0	% %
	Duty Cycle Accuracy	pin 3 = 3.2V, pin 15 = Vref pin 3 = 3.2V, pin 15 = open	40 85			% %
	Duty Cycle Accuracy	pin 3 = 2.02V, pin 15 = open	37	40	43	%
	Oscillator Ramp Peak			3.0		V
	Oscillator Ramp Valley			1.0		V
ERROR AMPLIFIER SECTION						
	Input Bias Current	V_{FB} to GND		0.2	1.0	µA
V_I	Input Voltage	V_{COMP} = V_{FB}	2.4	2.5	2.6	V
G_{OPL}	Open Loop Gain	V_{COMP} 2 to 4V	60	90		dB
SVR	Supply Voltage Rejection	V_{CC} = 12 to 20V		85		dB
V_{OL}	Output Low Voltage	Isink = 2mA			1.1	V
Io	Output Source Current	V_{COMP} > 4V	0.5	1.3		mA
	Unit Gain Bandwidth		2	4		MHz
S_R	Slew Rate			8		V/µA
PWM CURRENT SENSE SECTION						
I_b	Input Bias Current	I_{sen} = 0		3	15	µA
I_s	Maximum Input Signal	V_{COMP} = 5V	0.92	1.0	1.08	V
	Delay to Output			100		ns
	Gain		2.8	3	2.3	V/V
SOFT START						
I_{SSC}	SS Charge Current		14	20	26	µA
I_{SSD}	SS Discharge Current	VSS = 0.6V		200		µA
LEADING EDGE BLANKING						
	Internal Masking Time			100		ns

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ELECTRICAL CHARACTERISTICS (continued.)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
OUTPUT SECTION							
V_{OL}	Output Low Voltage	$I_O = 250mA$				1.0	V
V_{OH}	Output High Voltage	$I_O = 20mA$; $V_{CC} = 12V$		10	10.5		V
		$I_O = 200mA$; $V_{CC} = 12V$		9	10		V
	Collector Leakage	$V_{CC} = 20V$ $V_C = 24V$			100	200	μA
	Fall Time	$C_O = 1nF$ $C_O = 2.5nF$			20 35	60	ns ns
	Rise Time	$C_O = 1nF$ $C_O = 2.5nF$			50 70	100	ns ns
Out Leak	Output Leakage Sink	$V_{CC} = 3V$; $I_{sink} = 2mA$				1.0	V
UNDER VOLTAGE LOCKOUT SECTION							
	Start Threshold		L4990	15	16	17	V
			L4990A	7.8	8.4	9	V
op	Minimum Operating		L4990	9	10	11	V
			L4990A	7	7.6	8.2	v
V_{hys}	Voltage After Turn-on Hysteresis		L4990	5.5	6		V
			L4990A	0.5	0.8		v
SUPPLY CURRENT SECTION							
I_S	Start Up Current	$V_{CC} <$ Start Threshold			270	500	μA
I_{op}	Operating Current	$f_S = 300KHz$, $C_O = 1nF$			12	20	mA
I_q	Quiescent Current	(After turn on)			7.0	12	mA
I_{SH}	Shutdown Current				270	500	μA
V_Z	Zener Voltage	$I_8 = 20mA$		21	25	30	V
SINCHRONIZATION SECTION							
V_{ILt}	Low Input Voltage Threshold			1.0			V
V_{IHt}	High Input Voltage Threshold					3.5	V
V_{OH}	High Output Voltage	$I_{SOURCE} = 250μA$		4.2	4.7		V
OVER CURRENT PROTECTION							
V_t	Fault Threshold Voltage			1.1	1.2	1.3	V
DISABLE SECTION							
	Shutdown threshold			2.4	2.5	2.6	V

FUNCTIONAL DESCRIPTION

PWM Section

The I.C. contains a standard PWM control section with improved performance relative to the UC3842.
Enhanced features include start-up bias current reduced to < 300μA (typ), improved E/A performance (4MHz B/W, 1.3mA Source Current, hi-slew rate) accurate 1MHz oscillator, and also reduced propagation delays in the speed critical path from Current Sense to Output.

ADDED FEATURES

Soft Start (SS)

An external capacitor is charged by an internal constant current source (20μA) to generate a SS signal which clamps the E/A output
The SS pin doubles as a Fault Reset Delay function as described below.

Current Limit / Reset Delay

An internal hi-speed current limit comparator referenced to 1.2V detects primary over-current conditions. On detection of an overcurrent fault the output is immediately shutdown and the fault is also latched. A Fault Reset Delay is implemented by discharging the external Soft Start (SS) timing capacitor before resetting the fault latch and initiating a softstart cycle.
In the case of a continuous fault condition the SS capacitor is charged to 5V before being dis-

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charged again, to ensure that the fault frequency does not exceed the programmed soft start frequency.

Duty Cycle Limit

A simple connection between the DC-LIM and the available Vref actives the internal T- FlipFlop limiting the DC with accuracy of 50%. If this pin is not connected or grounded, the limit of the duty cycle is imposed by externally programmed voltage on pin 3 (DC)

Duty Cycle Control

Duty Cycle DC is externally programmed by setting a voltage between 1V (0% DC) and 3V (100% DC) at the DC pin. The programmed voltage is compared with the oscillator Ct capacitor charging waveform to determine the maximum ON-time in any one period. This function gives a flexible way of controlling DC and is convenient in TV applications where synchronisation is required.
If this pin is floating the duty cycle is not limited.

Synchronization

A SYNC pin eases Synchronization of the IC to the external world albeit to another IC working in parallel or to a TV/monitor.

In TV/monitor applications the timing components Rt, Ct are set for a frequency lower than the eventual TV sync frequency. When the TV circuit has powered-up it takes over and the system frequency is that of the SYNC. Duty Cycle is controllable using the DC function.
In parallel operation of several IC's no Master/Slave designation is required as the higher frequency IC is automatically the master. Controllers to be synchronized have their SYNC pins tied together and each SYNC pin operates as a bidirectional circuit. The first IC to drive its SYNC pin is the master and it initiates a discharge of the Ct timing capacitor of every controller. The Sync input signal is edge-triggered and sets an internal "sync latch" which ensures full discharge of Ct.

Disable Function

The DIS pin performs a logic level latched-shutdown function. When pulled above 2.5V it shuts down the complete IC with a standby current of <300µA (typ).
To reset the IC the V_{CC} pin must be pulled-down below the lower UVLO threshold (10V).

Leading Edge Blanking (LEB)

An LEB interval of 100ns has been incorporated into the IC to blank out the current sense signal during the first 100ns from switch turn-on.
This provides noise immunity to turn-on spikes and reduces external RC filtering requirements on the current-sense signal.
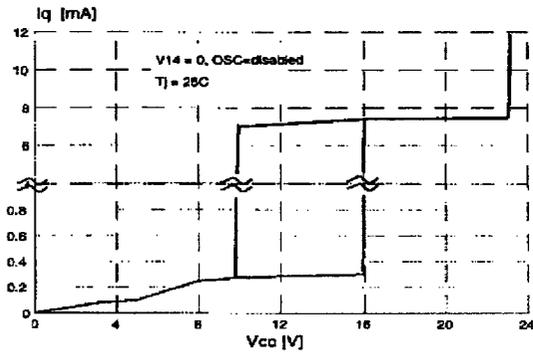
Figure 1: Quiescent current vs. input voltage.

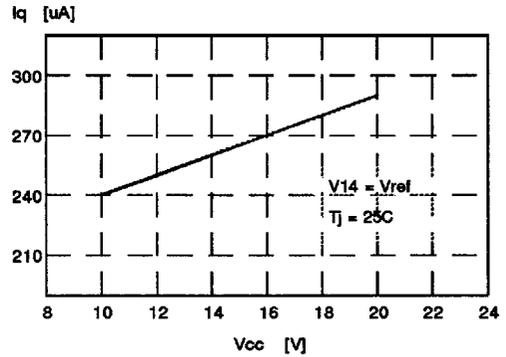**Figure 2:** Quiescent current vs. input voltage (after disable).
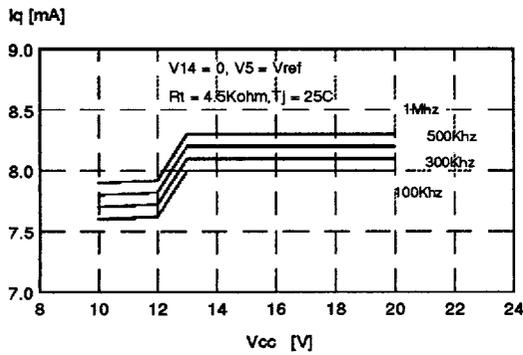

Figure 3: Quiescent current vs. input voltage.
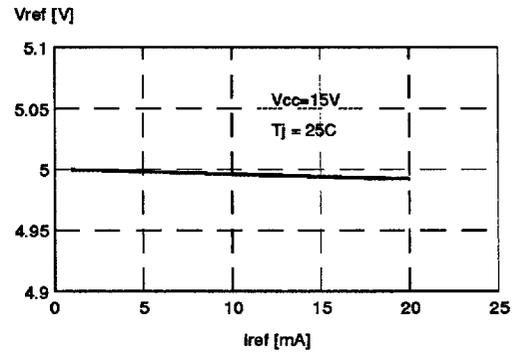

Figure 4: Reference voltage vs. load current.

Figure 5: Output saturation.

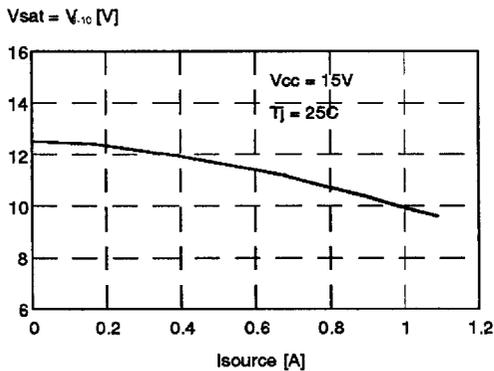**Figure 6:** Output saturation.

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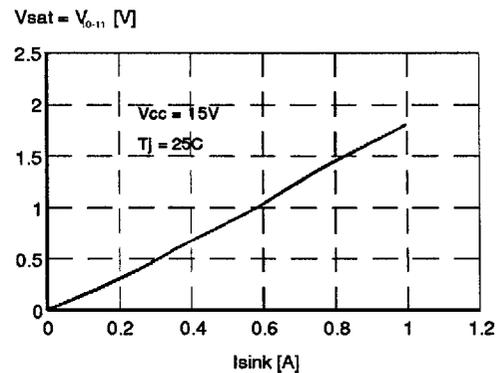
Figure 7: Vref vs. junction temperature.
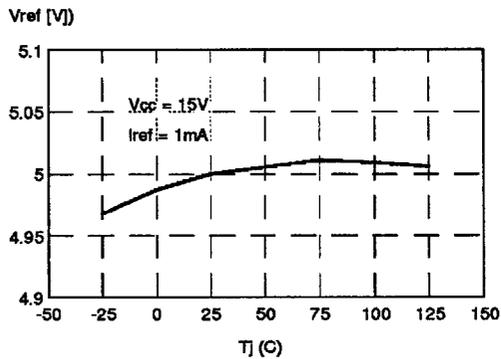
Figure 8: Vref vs. junction temperature.
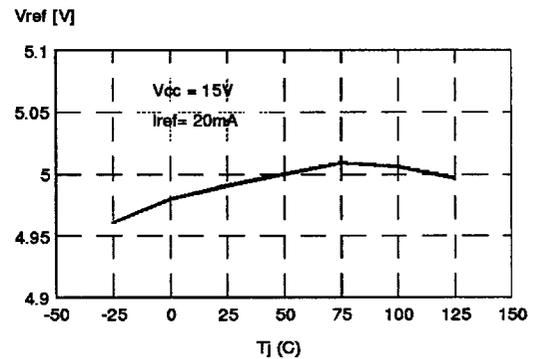
Figure 9: Switching frequency vs. temperature.
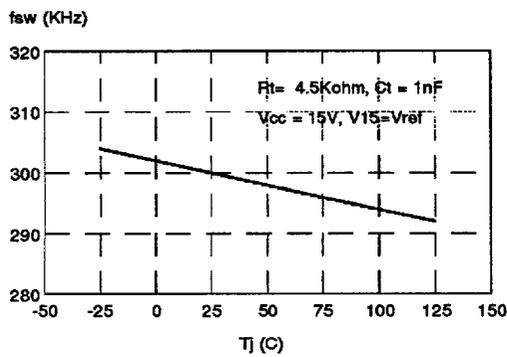
Figure 10: Switching frequency vs. temperature.
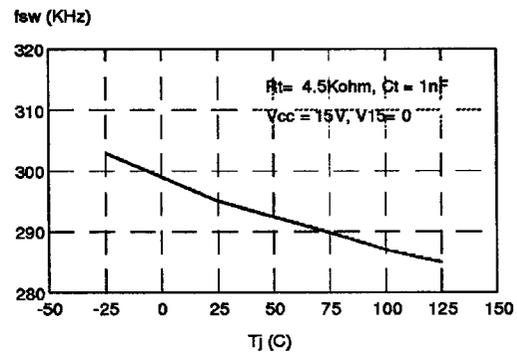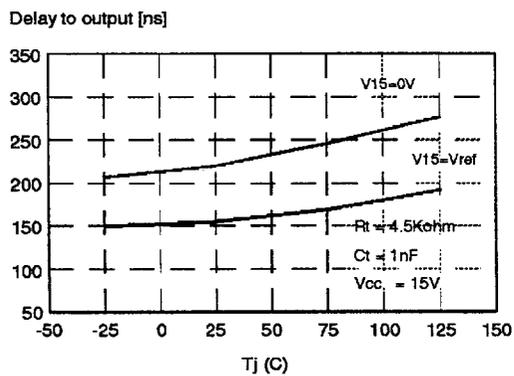

Figure 11: Delay to output vs junction temperature.

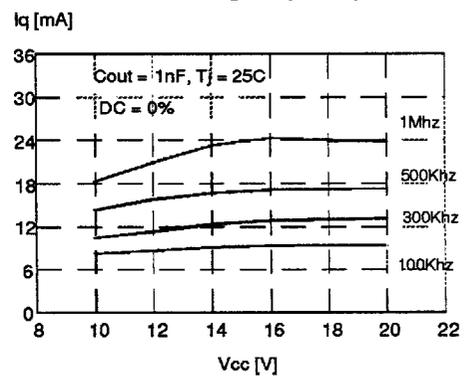**Figure 12:** Quiescent current vs. input voltage and switching frequency.

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Figure 13: Quiescent current vs. input voltage and switching frequency.
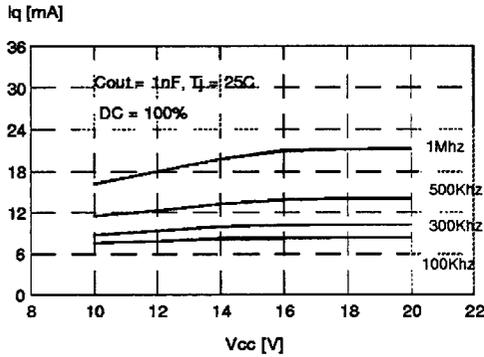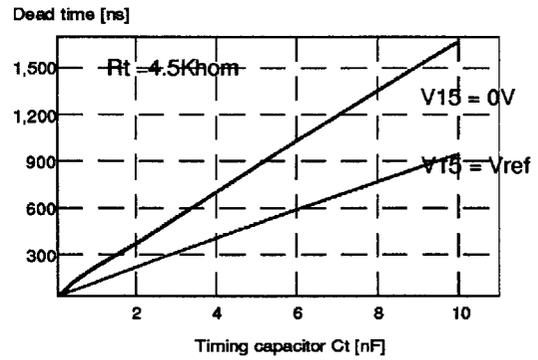

Figure 14: Dead time vs Ct.
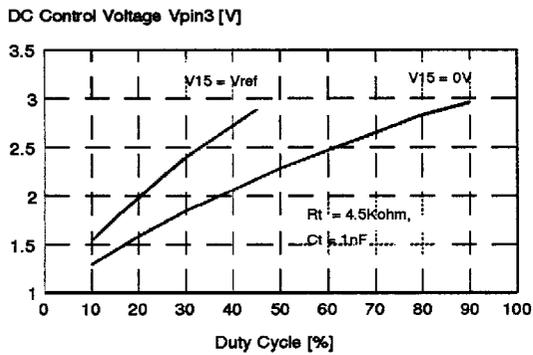

Figure 15: Maximum Duty Cycle vs Vpin3.

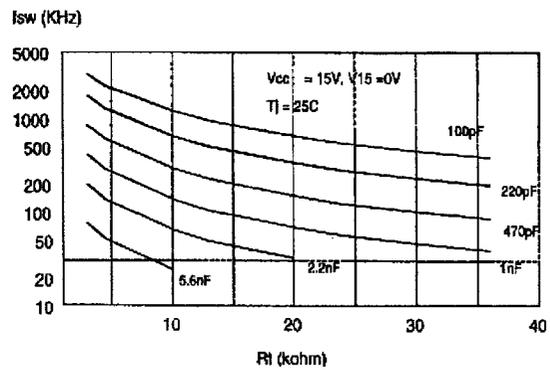**Figure 16:** Timing resistor vs. switching frequency.
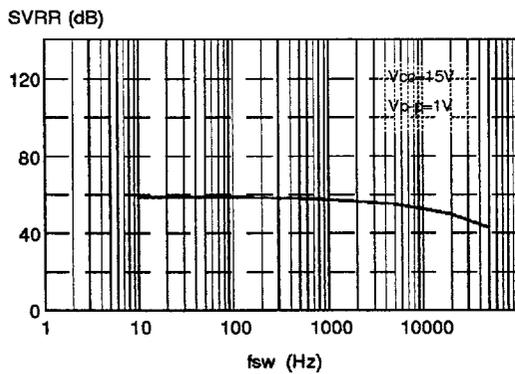

Figure 17: Vref SVRR vs. switching frequency.

Figure 18: E/A frequency response.

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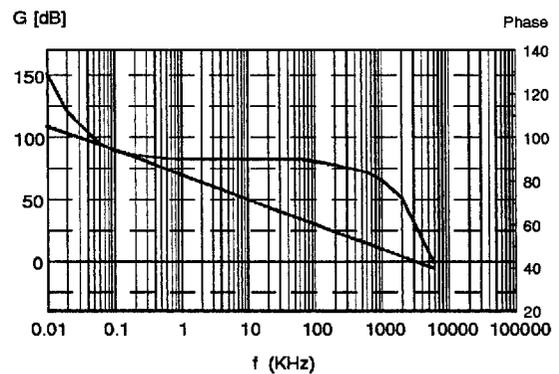## Main specs and performant

Topology: Flyback off-line discontinuous mode

Frequency: 200KHz

Input Voltage Range: 85 to 270Vac (50/60Hz)

Output Voltage: 15V

Nominal Output Power: 30W

Maximum Output Power: 40W

Lp 165uH (46litz wire 20x0.1mm)

Ls = 3uH (6T litz wire 4x20x0.1mm)

CORE = EFD25, 3F3, gap=1.5mm

Typical efficiency: 80%

Note: Fedback on primary side only (no optocoupler on the secondary)

$V_{in} = 85V$	$I_{out} = 0.5A$	$V_{out} = 15.484V$	u = 78.0%
	$I_{out} = 1.0A$	$V_{out} = 14.832V$	u = 82.4%
	$I_{out} = 2.0A$	$V_{out} = 14.244V$	u = 83.4%
$V_{in} = 180V$	$I_{out} = 0.5A$	$V_{out} = 15.494V$	u = 73.0%
	$I_{out} = 1.0A$	$V_{out} = 14.829V$	u = 82.6%
	$I_{out} = 2.0A$	$V_{out} = 14.249V$	u = 84.7%
$V_{in} = 270V$	$I_{out} = 0.5A$	$V_{out} = 15.472V$	u = 78.0%
	$I_{out} = 1.0A$	$V_{out} = 14.830V$	u = 74.7%
	$I_{out} = 2.0A$	$V_{out} = 14.240V$	u = 80.5%

Figure 19: 30W/200kHz off-line flyback with L4990

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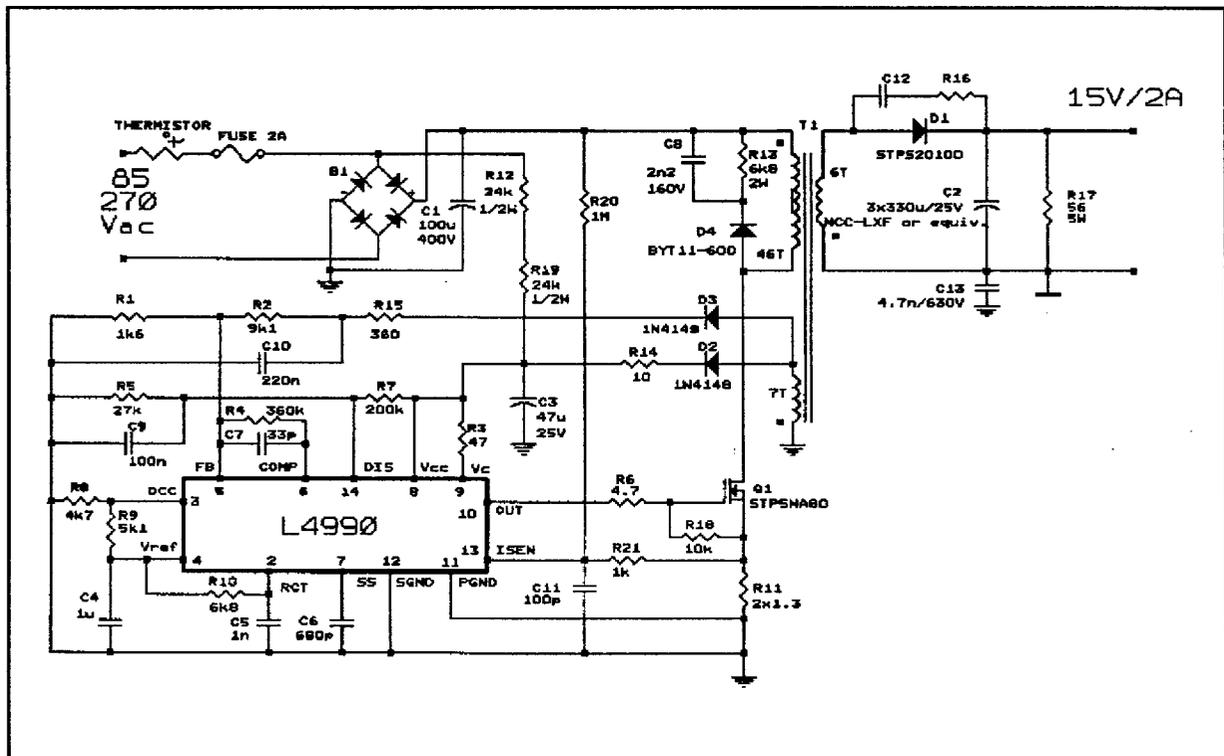
DIP16 PACKAGE AND MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

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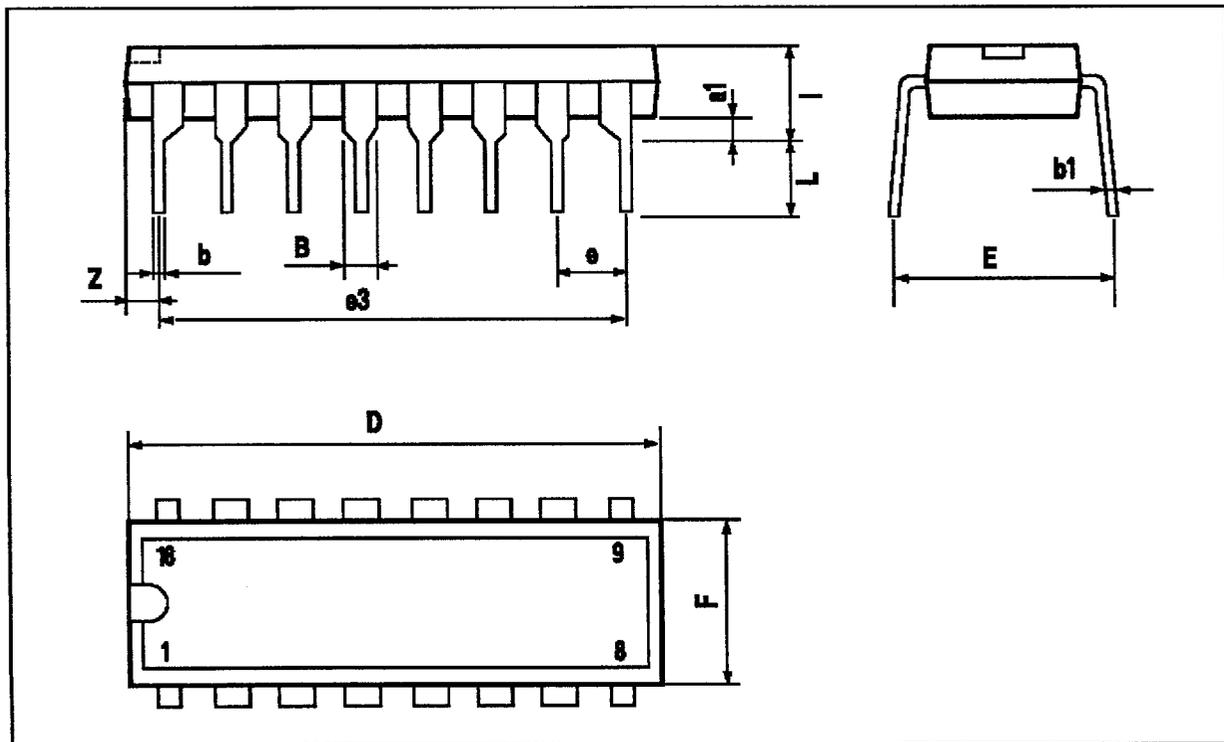
SO16 PACKAGE AND MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	10.1		10.5	0.398		0.413
E	10.0		10.65	0.394		0.419
e		1.27			0.050	
e3		8.89			0.350	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

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