

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288 WORDS × 8 BIT STATIC RAM

DESCRIPTION

The TC554001AFI/AFTI/ATRI is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.7 to 5.5V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 10mA/MHz(typ) and minimum cycle time of 70 ns. It is automatically placed in low-power mode at 2 μ A standby current (typ) when chip enable ($\overline{CE}$) is asserted high. There are two control inputs. $\overline{CE}$ is used to select the device and for data retention control, and output enable ($\overline{OE}$) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of -40° to 85°C, the TC554001AFI/AFTI/ATRI can be used in environments exhibiting extreme temperature conditions. The TC554001AFI/AFTI/ATRI is available in a standard plastic 32-pin small-outline package(SOP) and 32-pin thin-small-outline package(TSOP).

FEATURES

- Low-power dissipation
Operating: 55 mW/MHz (typical)
- Standby current of 5 μ A (maximum) at
Ta = 25°C
- Single power supply voltage of 2.7 to 5.5 V
- Power down features using $\overline{CE}$
- Data retention supply voltage of 2.0 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to 85°C

• Access Time (maximum)

	5V $\pm$ 10%			2.7 to 5.5 V
	-70 V	-85 V	-10 V	-70 V/-85 V/-10 V
Access Time	70 ns	85 ns	100 ns	150 ns
$\overline{CE}$ Access Time	70 ns	85 ns	100 ns	150 ns
$\overline{OE}$ Access Time	35 ns	45 ns	50 ns	75 ns

• Package:

SOP32-P-525-1.27 (AFI) (Weight: g typ)
 TSOP II 32-P-400-1.27 (AFTI) (Weight: g typ)
 TSOP II 32-P-400-1.27A (ATRI) (Weight: g typ)

PIN ASSIGNMENT (TOP VIEW)

○ 32 PIN AFI/AFTI				○ 32 PIN ATRI			
A18	1	32	V_{DD}	32	1	A18	
A16	2	31	A15	31	2	A16	
A14	3	30	A17	30	3	A14	
A12	4	29	R/W	29	4	A12	
A7	5	28	A13	28	5	A7	
A6	6	27	A8	27	6	A6	
A5	7	26	A9	26	7	A5	
A4	8	25	A11	25	8	A4	
A3	9	24	$\overline{OE}$	24	9	A3	
A2	10	23	A10	23	10	A2	
A1	11	22	$\overline{CE}$	22	11	A1	
A0	12	21	I/O8	21	12	A0	
I/O1	13	20	I/O7	20	13	I/O1	
I/O2	14	19	I/O6	19	14	I/O2	
I/O3	15	18	I/O5	18	15	I/O3	
GND	16	17	I/O4	17	16	GND	

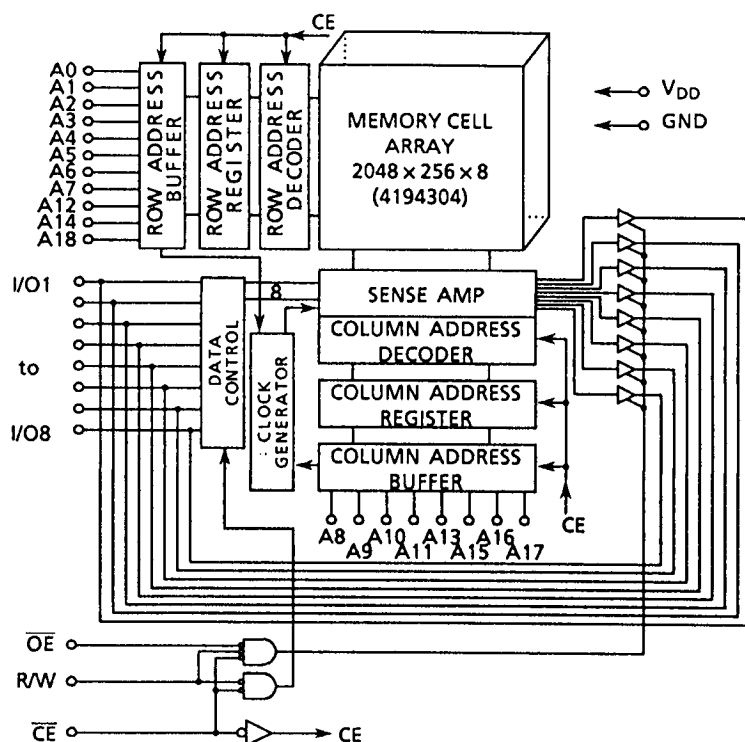
PIN NAMES

A0 to A18	Address Inputs
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/O1 to I/O8	Data Input/Output
V_{DD}	Power
GND	Ground

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BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 to I/O8	POWER
Read	L	L	H	D _{OUT}	I _{DDO}
Write	L	x	L	D _{IN}	I _{DDO}
Output Disabled	L	H	H	High-Z	I _{DDO}
Standby	H	x	x	High-Z	I _{DDs}

Note: X = don't care. H=logic high. L=logic low.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	- 0.3 to 7.0	V
V _{IN}	Input Voltage	- 0.3* to 7.0	V
V _{IO}	Input and Output Voltage	- 0.5 to V _{DD} + 0.5	V
P _D	Power Dissipation	0.6	W
T _{solder}	Soldering Temperature (10 s)	260	°C
T _{strg.}	Storage Temperature	- 55 to 150	°C
T _{opr.}	Operating Temperature	- 40 to 85	°C

* - 3.0 V when measured at a pulse width of 50 ns

DC RECOMMENDED OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C)

SYMBOL	PARAMETER	5 V $\pm$ 10%			2.7 to 5.5V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	2.7	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	$V_{DD} + 0.3$	$V_{DD} - 0.2$	–	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3^*	–	0.6	-0.3^*	–	0.2	V
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	2.0	–	5.5	V

* -3.0 V when measured at a pulse width of 50 nsDC CHARACTERISTICS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 5\text{ V} \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}				–	–	± 1.0	μA
I _{LO}	Output Leakage Current	C _E = V _{IH} or O _E = V _{IH} or R/W = V _{IL} V _{OUT} = 0 V to V _{DD}				–	–	± 1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4 V				– 1.0	–	–	mA
I _{OL}	Output Low Current	V _{OL} = 0.4 V				2.1	–	–	mA
I _{DDO1}	Operating Current	C _E = V _{IL} and R/W = V _{IH} I _{OUT} = 0 mA Other Inputs = V _{IH} /V _{IL}		Tcycle	min	–	–	70	mA
					1 μs	–	15	–	
I _{DDO2}		C _E = 0.2 V and R/W = V _{DD} –0.2 V I _{OUT} = 0 mA Other Inputs = V _{DD} –0.2 V/0.2 V		Tcycle	min	–	–	60	mA
					1 μs	–	10	–	
I _{DDS1}	Standby Current	C _E = V _{IH}				–	–	3	mA
I _{DDS2}		C _E = V _{DD} –0.2 V	V _{DD} = 2.0 to 5.5 V	Ta = 25°C		–	2	5	
				Ta = –40° to 85°C		–	–	100	
			V _{DD} = 3.0 V	Ta = 25°C		–	2	–	
				Ta = –40° to 40°C		–	–	5	
		Ta = –40° to 85°C		–	–	50			

DC CHARACTERISTICS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 3.0\text{ V} \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}			–	–	± 1.0	μA
I _{LO}	Output Leakage Current	CE̅ = V _{IH} or OE̅ = V _{IH} or R/W = V _{IL} V _{OUT} = 0 V to V _{DD}			–	–	± 1.0	μA
I _{OH}	Output High Current	V _{OH} = V _{DD} –0.2 V			– 0.1	–	–	mA
I _{OL}	Output Low Current	V _{OL} = 0.2 V			0.1	–	–	mA
I _{DDO2}	Operating Current	CE̅ = 0.2 V and R/W = V _{DD} –0.2 V I _{OUT} = 0 mA Other Inputs = V _{DD} –0.2 V/0.2 V	T _{cycle}	min	–	–	30	mA
				1 μs	–	5	–	
I _{DDs2}	Standby Current	CE̅ = V _{DD} –0.2 V	V _{DD} = 3.0 ± 0.3 V	T _a = 25°C	–	2	3	μA
				T _a = –40° to 85°C	–	–	56	
			V _{DD} = 3.0 V	T _a = 25°C	–	2	–	
				T _a = –40° to 40°C	–	–	5	
				T _a = –40° to 85°C	–	–	50	

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 5\text{V} \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC554001AFI/AFTI/ATRI						UNIT
		-70 V		-85 V		-10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	70	–	85	–	100	–	ns
t _{ACC}	Address Access Time	–	70	–	85	–	100	
t _{CO}	Chip Enable Accses Time	–	70	–	85	–	100	
t _{OE}	Output Enable Accses Time	–	35	–	45	–	50	
t _{COE}	Chip Enable Low to Output Active	5	–	5	–	5	–	
t _{OEE}	Output Enable Low to Output Active	0	–	0	–	0	–	
t _{OD}	Chip Enable Hige to Output High-Z	–	25	–	30	–	35	
t _{ODO}	Output Enable Hige to Output High-Z	–	25	–	30	–	35	
t _{OH}	Output Data Hold Time	10	–	10	–	10	–	

WRITE CYCLE

SYMBOL	PARAMETER	TC554001AFI/AFTI/ATRI						UNIT
		-70 V		-85 V		-10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	70	–	85	–	100	–	ns
t _{WP}	Write Pulse Width	50	–	55	–	60	–	
t _{CW}	Chip Enable to End of Write	60	–	70	–	80	–	
t _{AS}	Address Setup Time	0	–	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	0	–	
t _{ODW}	R/W Low to Output High-Z	–	30	–	35	–	40	
t _{OEW}	R/W High to Output Active	0	–	0	–	0	–	
t _{DS}	Data Setup Time	30	–	35	–	40	–	
t _{DH}	Data Hold Time	0	–	0	–	0	–	

AC TEST CONDITIONS

Output Load: 100 pF + one TTL gate

Input Pulse Level: 0.4 V, 2.6 V

Timing Measurements: 1.5 V

Reference Level: 1.5 V

 t_r, t_f : 5 ns

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 2.7\text{V}$ to 5.5V)READ CYCLE

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{RC}	Read Cycle Time	150	—	ns
t_{ACC}	Address Access Time	—	150	
t_{CO}	Chip Enable ($\overline{CE}$) Access Time	—	150	
t_{OE}	Output Enable to Output in Valid	—	75	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	5	—	
t_{OEE}	Output Enable to Output in Low-Z	0	—	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	—	50	
t_{ODO}	Output Enable to Output in High-Z	—	50	
t_{OH}	Output Data Hold Time	10	—	

WRITE CYCLE

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{WC}	Write Cycle Time	150	—	ns
t_{WP}	Write Pulse Width	100	—	
t_{CW}	Chip Enable to End of Write	120	—	
t_{AS}	Address Setup Time	0	—	
t_{WR}	Write Recovery Time	0	—	
t_{ODW}	R/W Low to Output High-Z	—	50	
t_{OEW}	R/W High to Output Active	0	—	
t_{DS}	Data Setup Time	60	—	
t_{DH}	Data Hold Time	0	—	

AC TEST CONDITIONS

Output Load: 100 pF (Include Jig)

Input Pulse Level: $V_{DD} - 0.2\text{V}/0.2\text{V}$

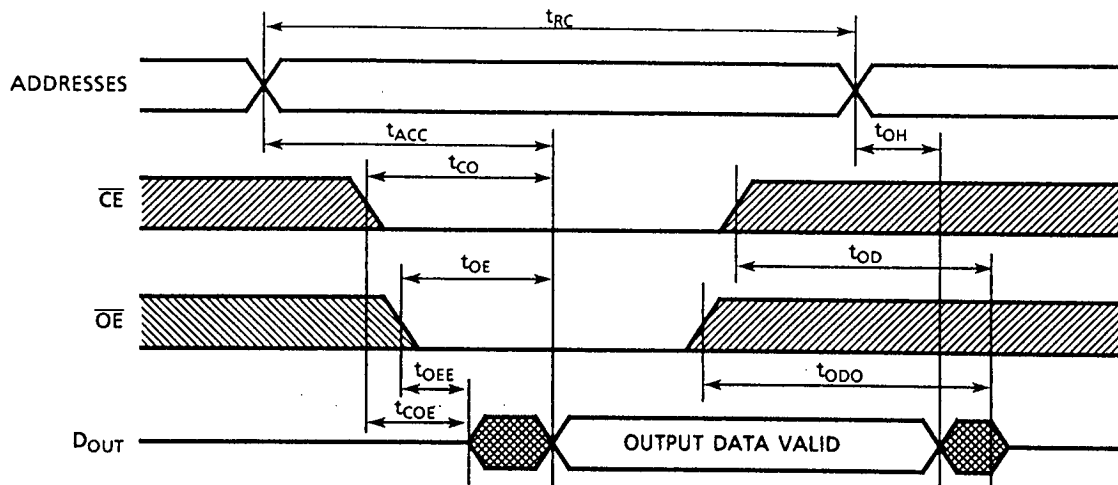
Timing Measurements: 1.5 V

Reference Level: 1.5 V

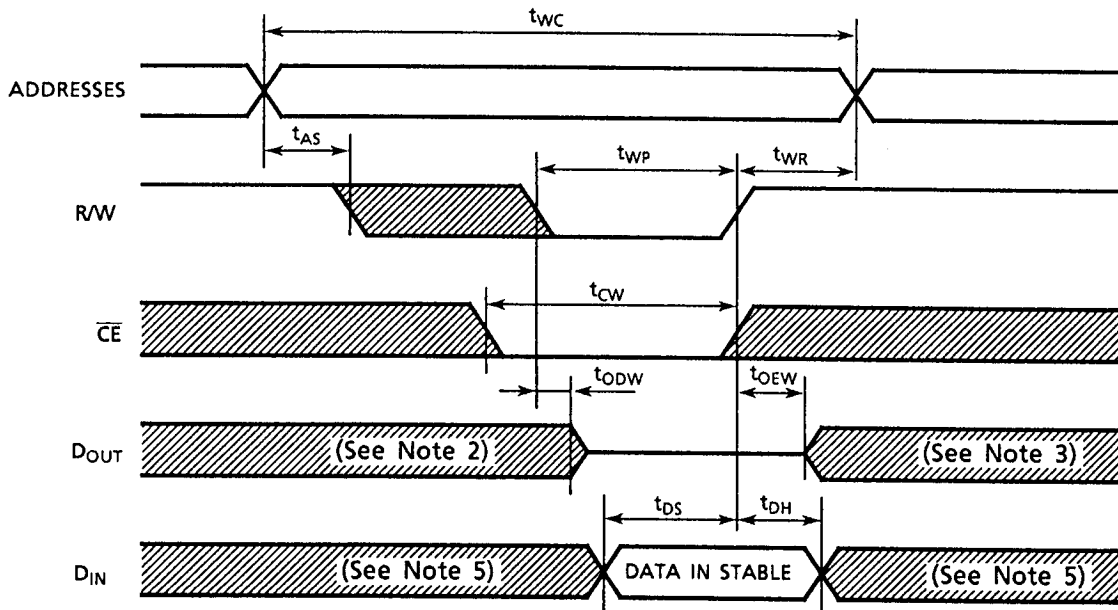
 t_r, t_f : 5 ns

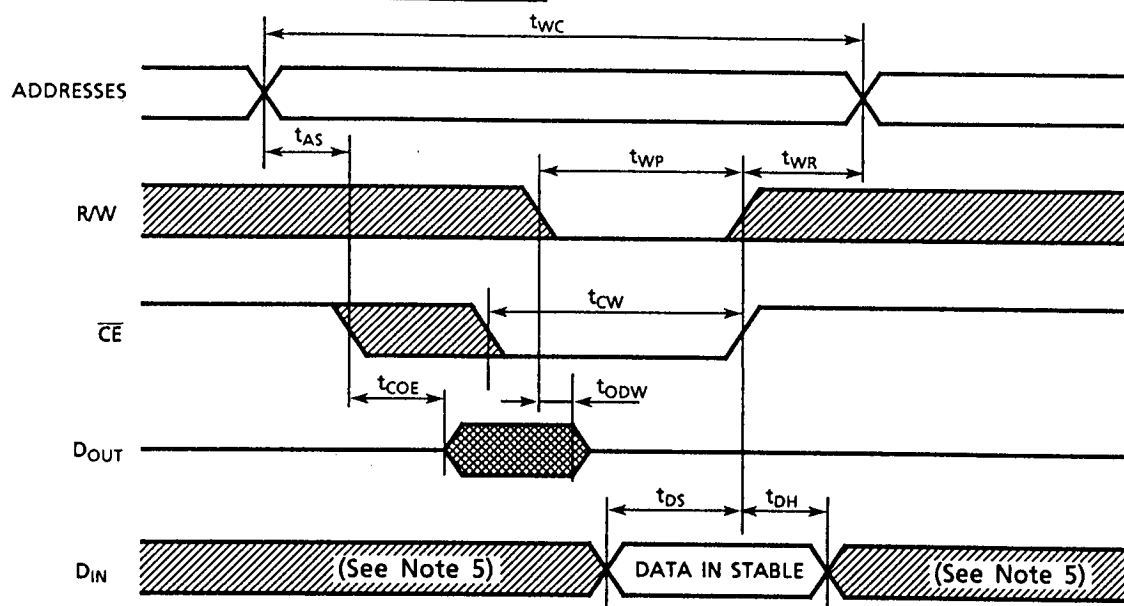
TIMING WAVEFORMS

READ CYCLE (See Note 1)



WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)

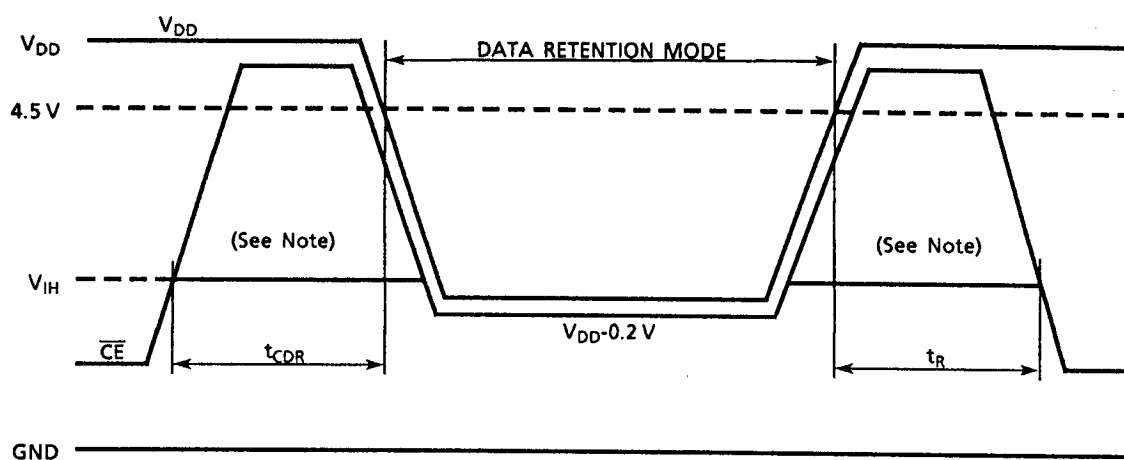


WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 4)

- (1) R/W remains High for Read Cycle.
- (2) If $\overline{CE}$ goes coincident with or after R/W goes LOW, the output will remain at high impedance.
- (3) If $\overline{CE}$ goes HIGH coincident with or before R/W goes HIGH, the output will remain at high impedance.
- (4) IF $\overline{CE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

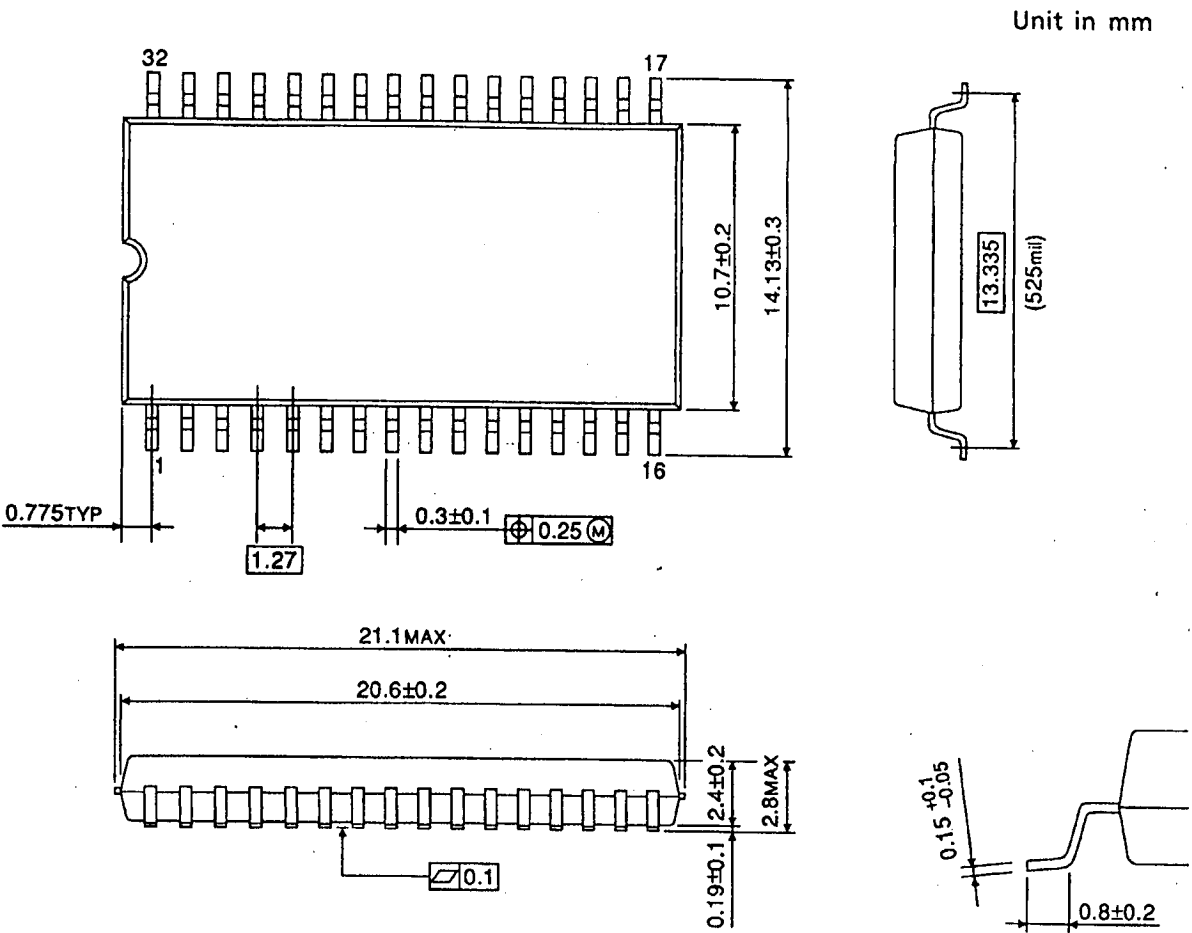
DATA RETENTION CHARACTERISTICS ($T_a = -40^\circ$ to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
$I_{DD\bar{S}2}$	Standby Current	$V_{DH} = 3.0\text{ V}$	—	50*	μA
		$V_{DH} = 5.5\text{ V}$	—	100	
t_{CDR}	Chip Deselect to Data Retention Mode Time	0	—	—	nS
t_R	Recovery Time	5	—	—	mS

*) $5\text{ }\mu\text{A}$ (max) $T_a = -40^\circ$ to 40°C $\overline{\text{CE}}$ Controlled Data Retention Mode

Note: When $\overline{\text{CE}}$ is operating at the V_{IH} level (2.4V), the standby current is given by $I_{DD\bar{S}1}$ during the transition of V_{DD} from 4.5 to 2.6V.

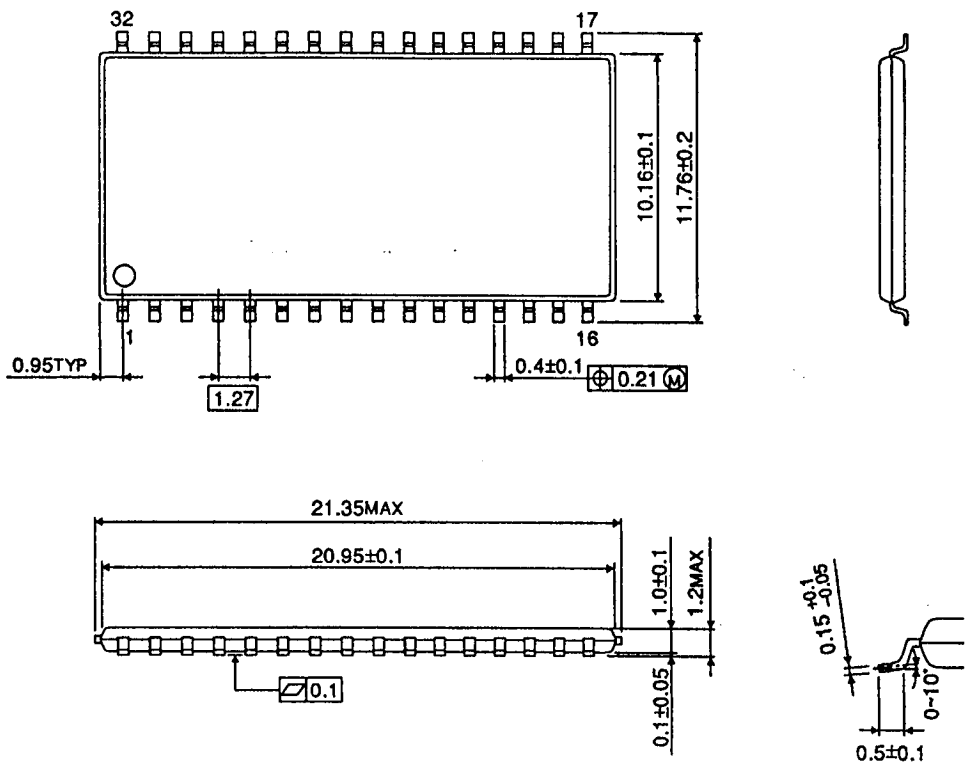
PACKAGE DIMENSIONS (SOP32-P-525-1.27)



Weight: g (typ)

PACKAGE DIMENSIONS (TSOPII 32-P-400-1.27)

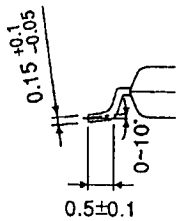
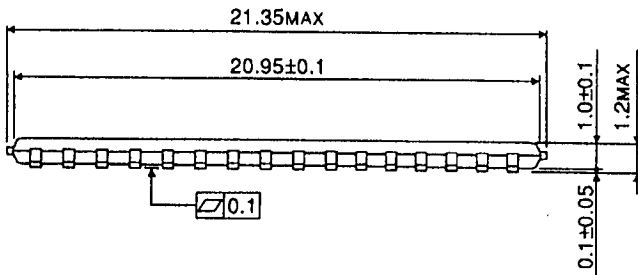
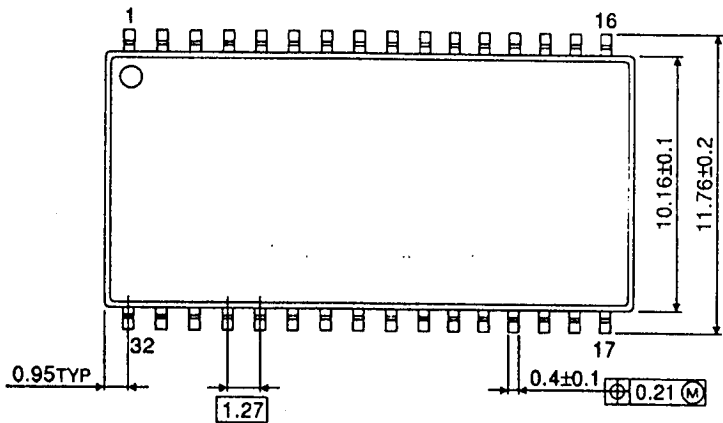
Unit in mm



Weight: g (typ)

PACKAGE DIMENSIONS (TSOPII 32-P-400-1.27A)

Unit in mm



Weight: g (typ)