



IP4285CZ6-TY

ESD protection for high-speed interfaces

Rev. 2 — 12 November 2012

Product data sheet

1. Product profile

1.1 General description

The device is designed to protect electrical interfaces such as USB 2.0 ports in computer or communication devices against ElectroStatic Discharge (ESD).

The device includes high-level ESD protection diodes for high-speed signal lines. It is encapsulated in a very small 6-pin SOT363 Surface-Mounted Device (SMD) plastic package. Due to the small package dimensions the device is suitable for portable devices.

A special diode configuration protects all signal lines. These diodes offer ultra low line capacitance of 0.85 pF maximum and provide protection to downstream components from ESD voltages up to ± 12 kV contact according to IEC 61000-4-2, level 4.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- System ESD protection for USB 2.0
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ± 12 kV according to IEC 61000-4-2, level 4
- Line capacitance of 0.85 pF maximum for each channel

1.3 Applications

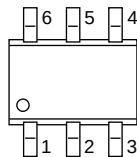
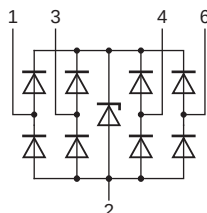
The device is designed for receiver and transmitter port protection in:

- Portable devices
- Mobile handsets
- TVs, monitors
- DVD recorders and players
- Notebooks, mother boards, graphic cards and ports
- Set-top boxes and game consoles



2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	ESD protection for I/O signals		
2	ground		
3	ESD protection for I/O signals		
4	ESD protection for I/O signals		
5	n.c.		
6	ESD protection for I/O signals		

018aaa176

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4285CZ6-TY	SC-88	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 3. Marking codes

Type number	Marking code ^[1]
IP4285CZ6-TY	85*

[1] * = placeholder for manufacturing site code.

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		-0.5	+5.5	V
V_{ESD}	electrostatic discharge voltage	pins 1, 3, 4, 6 to ground; IEC 61000-4-2, level 4			
		contact discharge	-	±12	kV
T_{amb}	ambient temperature		-40	+85	°C
T_{stg}	storage temperature		-55	+125	°C

6. Characteristics

Table 5. Characteristics

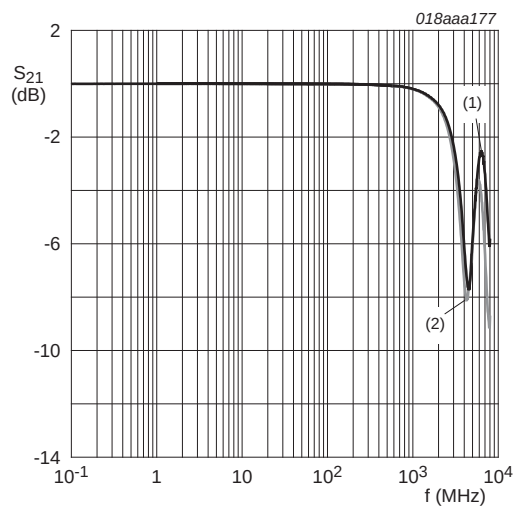
$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BR}	breakdown voltage	$I_{test} = 1\text{ mA}$	6	-	9	V
I_{RM}	reverse leakage current	per channel; $V_I = 5.0\text{ V}$	-	-	1	μA
V_F	forward voltage		-	0.7	-	V
C_{ch}	channel capacitance	$f = 1\text{ MHz}$	[1]			
		$V_{bias} = 0\text{ V}$	-	-	0.85	pF
		$V_{bias} = 2.5\text{ V}$	-	-	0.75	pF
ΔC_{ch}	channel capacitance difference	$f = 1\text{ MHz};$ $V_{bias} = 2.5\text{ V}$	[1]	-	0.1	pF
R_{dyn}	dynamic resistance	TLP	[3]			
		positive transient	-	0.42	-	Ω
		negative transient	-	0.33	-	Ω
		surge	[2]			
		positive transient	-	0.42	-	Ω
		negative transient	-	0.33	-	Ω
$V_{CL(trt)}$	transient clamping voltage	$I_{PP} = 4\text{ A}$	[2]			
		positive transient	-	4.2	-	V
		negative transient	-	-1.9	-	V

[1] This parameter is guaranteed by design.

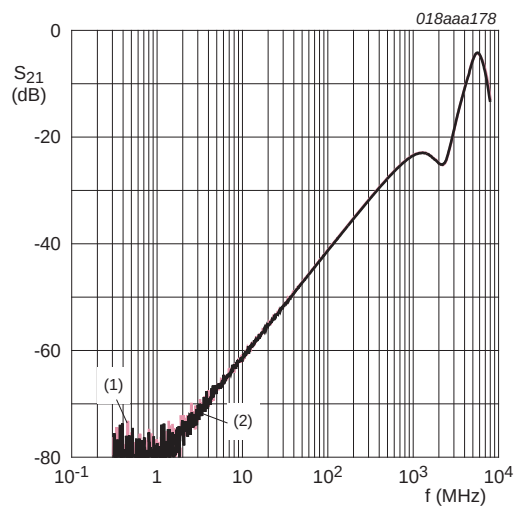
[2] According to IEC 61000-4-5.

[3] 100 ns Transmission Line Pulse (TLP); 50 Ω ; pulser at 80 ns.



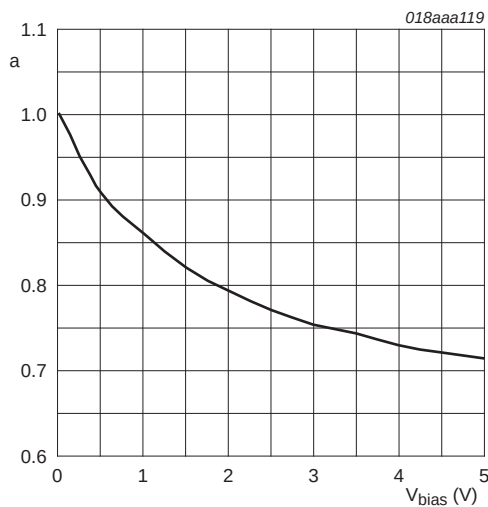
- (1) Pin 1 and 3
- (2) Pin 4 and 6

Fig 1. Insertion loss



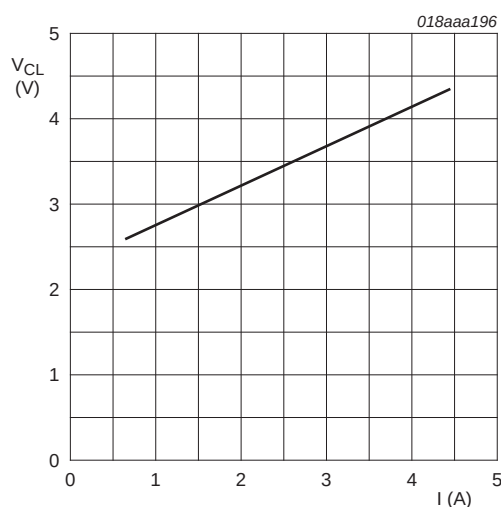
- (1) Pin 1 to 6
- (2) Pin 3 to 4

Fig 2. Crosstalk response curves



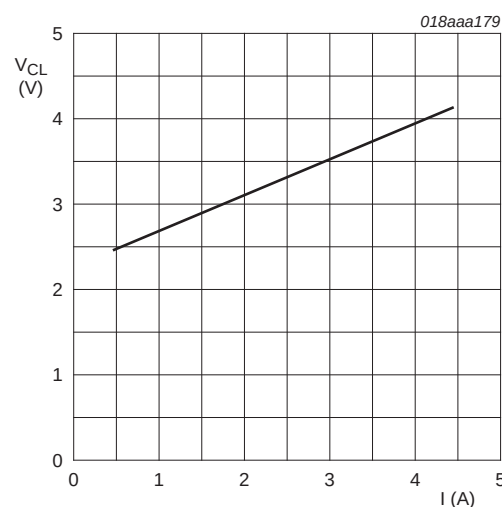
$$a = \frac{C_{ch}}{C_{ch}(0V_{bias})}$$

Fig 3. Relative channel capacitance as a function of bias voltage; typical values



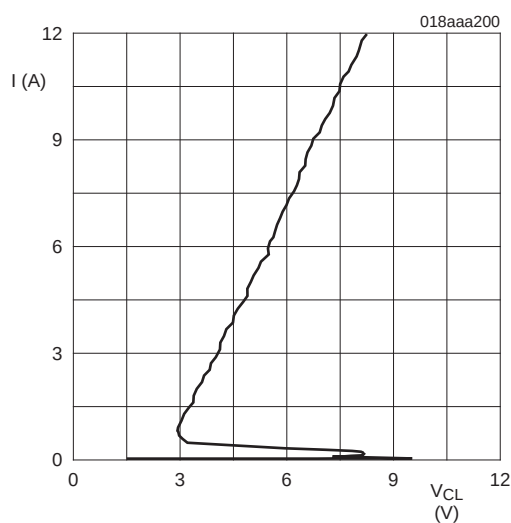
IEC 61000-4-5; $t_p = 8/20 \mu s$; positive pulse

Fig 4. Dynamic resistance with positive clamping



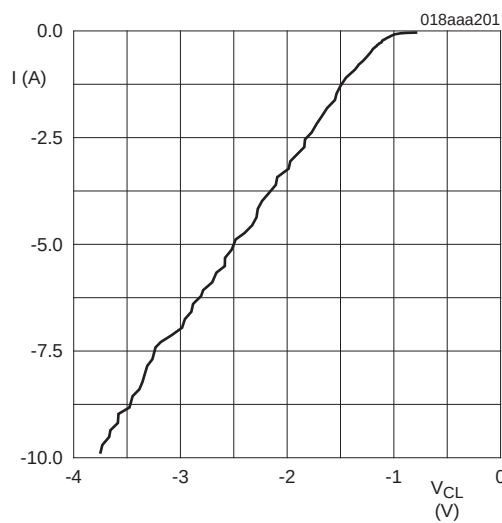
IEC 61000-4-5; $t_p = 8/20 \mu s$; negative pulse

Fig 5. Dynamic resistance with negative clamping



$t_p = 100 ns$; Transmission Line Pulse (TLP)

Fig 6. Dynamic resistance with positive clamping



$t_p = 100 ns$; Transmission Line Pulse (TLP)

Fig 7. Dynamic resistance with negative clamping

The device uses an advanced clamping structure, which shows a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

7. Package outline

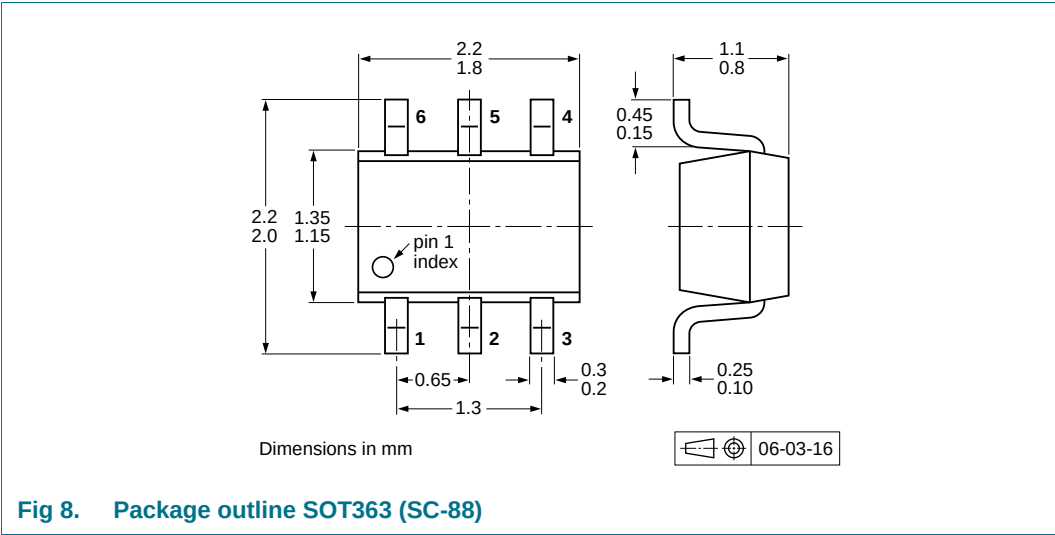
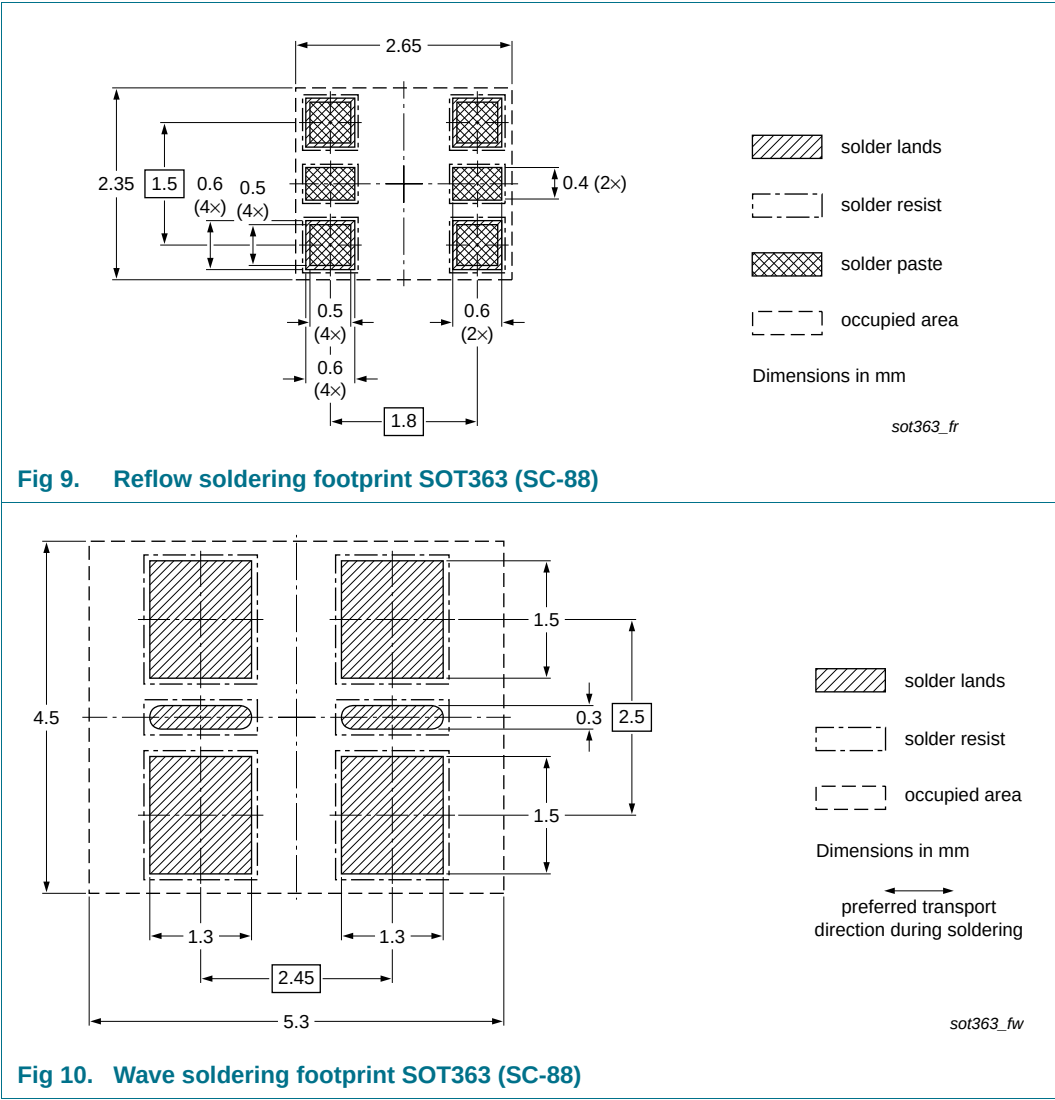


Fig 8. Package outline SOT363 (SC-88)

8. Soldering



9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4285CZ6-TY v.2	20121112	Product data sheet	-	IP4285CZ6-TY v.1
Modifications:	• Table 4 “Limiting values”: updated • Section 6 “Characteristics”: updated • Section 7 “Package outline”: replaced with minimized outline drawing • Section 10 “Legal information”: updated			
IP4285CZ6-TY v.1	20111103	Objective data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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