

# 54ACT11533, 74ACT11533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS017A – D2957, JULY 1987 – REVISED APRIL 1993

- Eight Latches in a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V<sub>CC</sub> and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

## description

These eight latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

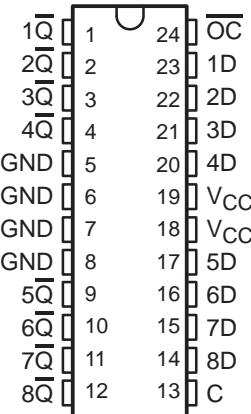
The eight latches of the 'ACT11533 are transparent D-type latches. While the enable (C) is high, the  $\bar{Q}$  outputs will follow the complements of the (D) inputs. When the output control  $\bar{OC}$  is taken low, the  $\bar{Q}$  outputs will be latched. The 'ACT11533 is functionally equivalent to the 'ACT11373 except for having inverted outputs.

A buffered output-control ( $\bar{OC}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components.

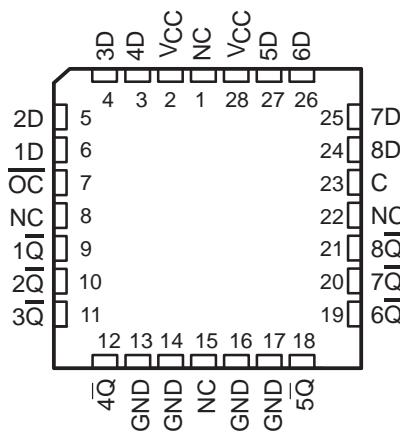
The output control ( $\bar{OC}$ ) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The 54ACT11533 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT11533 is characterized for operation from –40°C to 85°C.

54ACT11533 ... JT PACKAGE  
74ACT11533 ... DW OR NT PACKAGE  
(TOP VIEW)



54ACT11533 ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## FUNCTION TABLE (each latch)

INPUTS			OUTPUT
$\bar{OC}$	C	D	$\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

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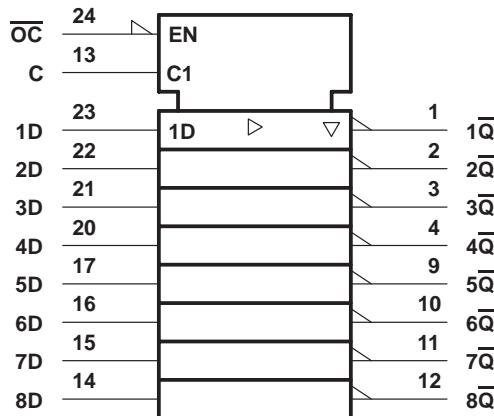
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**WITH 3-STATE OUTPUTS**

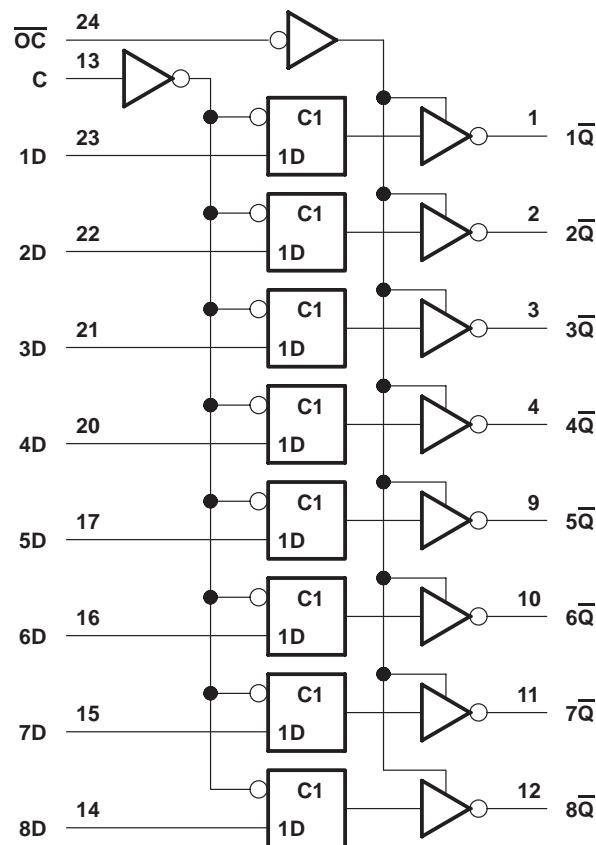
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**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**logic diagram (positive logic)**



Pin numbers shown are for the DW, JT, and NT packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 6 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	± 20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	± 50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	± 50 mA
Continuous current through $V_{CC}$ or GND .....	± 200 mA
Storage temperature range .....	–65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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**recommended operating conditions**

		54ACT11533		74ACT11533		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24		-24	mA
$I_{OL}$	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ C$			54ACT11533	74ACT11533	UNIT
			MIN	TYP	MAX	MIN	MAX	
$V_{OH}$	$I_{OH} = -50 \mu A$	4.5 V	4.4			4.4	4.4	V
		5.5 V	5.4			5.4	5.4	
	$I_{OH} = -24 mA$	4.5 V	3.94			3.7	3.8	
		5.5 V	4.94			4.7	4.8	
	$I_{OH} = -50 mA^\dagger$	5.5 V				3.85		
$V_{OL}$	$I_{OL} = 50 \mu A$	4.5 V		0.1		0.1	0.1	V
		5.5 V		0.1		0.1	0.1	
	$I_{OL} = 24 mA$	4.5 V		0.36		0.5	0.44	
		5.5 V		0.36		0.5	0.44	
	$I_{OL} = 50 mA^\dagger$	5.5 V				1.65		
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5 V		$\pm 0.5$		$\pm 10$	$\pm 5$	$\mu A$
		5.5 V		$\pm 0.1$		$\pm 1$	$\pm 1$	
	$I_I$	$V_I = V_{CC}$ or GND	5.5 V					
	$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		8	160	80	
	$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at GND or $V_{CC}$	5.5 V		0.9	1	1	mA
$C_i$	$V_I = V_{CC}$ or GND	5 V		4				pF
$C_o$	$V_O = V_{CC}$ or GND	5 V		10				pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$			54ACT11533		74ACT11533		UNIT
			MIN	MAX		MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, C high		5			5		5		ns
$t_{su}$	Setup time, data before C↓		3.5			3.5		3.5		ns
$t_h$	Hold time, data after C↓		3.5			3.5		3.5		ns

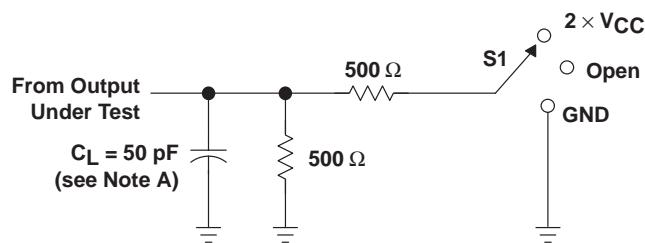
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11533		74ACT11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	$\bar{Q}$	1.5	7	10.1	1.5	11.9	1.5	11.3	ns
$t_{PHL}$			1.5	6.5	8.4	1.5	10.2	1.5	9.5	
$t_{PLH}$	C	Any $\bar{Q}$	1.5	8.5	11.3	1.5	14.1	1.5	13	ns
$t_{PHL}$			1.5	8.5	10.7	1.5	13.2	1.5	12.2	
$t_{PZH}$	$\bar{OC}$	Any $\bar{Q}$	1.5	7.5	10.7	1.5	13.6	1.5	12.5	ns
$t_{PZL}$			1.5	7.5	10.9	1.5	12.9	1.5	12	
$t_{PHZ}$	$\bar{OC}$	Any $\bar{Q}$	1.5	10.5	12.1	1.5	13.1	1.5	12.8	ns
$t_{PLZ}$			1.5	7.5	9.5	1.5	10.7	1.5	10.3	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

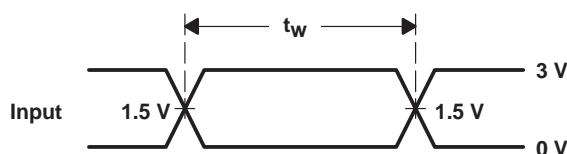
Cpd	Power dissipation capacitance per latch	Outputs enabled	TEST CONDITIONS		TYP	UNIT
			$C_L = 50\text{ pF}$ ,	$f = 1\text{ MHz}$		
		Outputs disabled		69		
					58	pF

PARAMETER MEASUREMENT INFORMATION

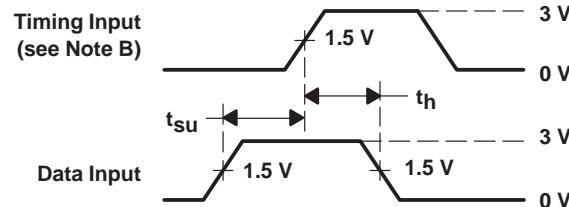


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

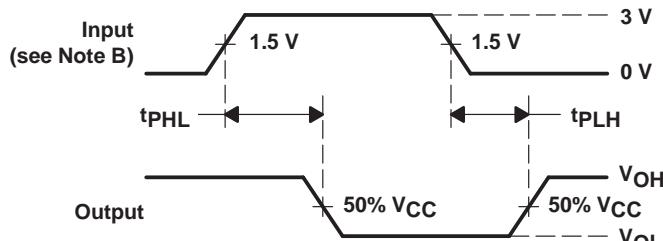
LOAD CIRCUIT



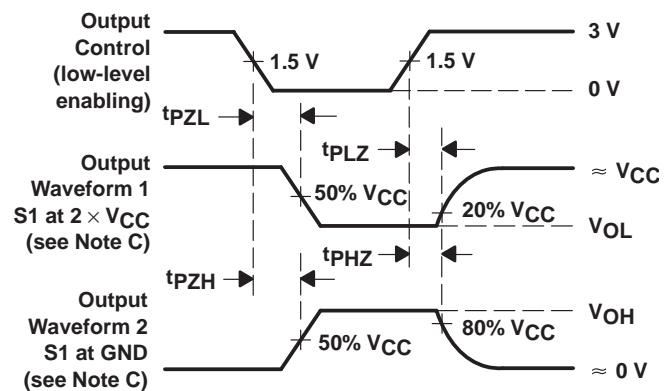
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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