

## ADVANCED REGULATING PULSE WIDTH MODULATORS

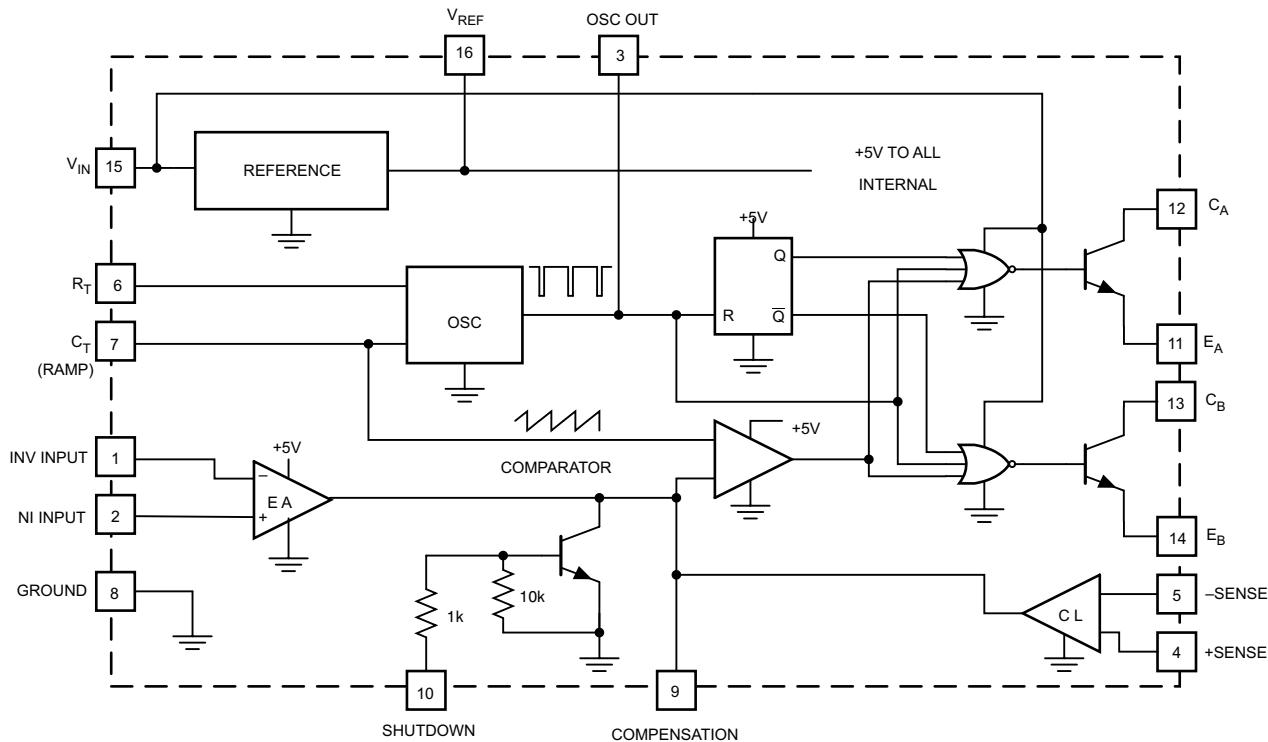
### FEATURES

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for Single-Ended or Push-Pull Applications
- Low Standby Current . . . 8 mA Typical
- Interchangeable With SG1524, SG2524 and SG3524, Respectively

### DESCRIPTION

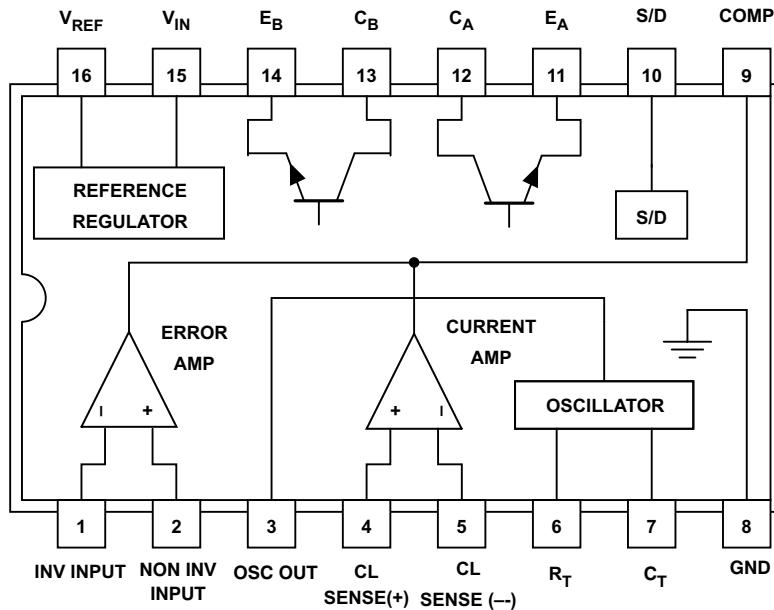
The UC1524, UC2524 and UC3524 incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies, inverters or switching regulators. They can also be used as the control element for high-power-output applications. The UC1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The UC1524 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The UC2524 and UC3524 are designed for operation from  $-25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  and  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ , respectively.

### BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## CONNECTION DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		UNIT
$V_{CC}$	Supply voltage <sup>(1)(2)</sup>	40 V
	Collector output current	100 mA
	Reference output current	50 mA
	Current through $C_T$ terminal	-50 mA
Power dissipation	$T_A = 25^\circ\text{C}$ <sup>(3)</sup>	1000 mW
	$T_C = 25^\circ\text{C}$ <sup>(3)</sup>	2000 mW
Operating junction temperature range		-55°C to 150°C
Storage temperature range		-65°C to +150°C

(1) All voltage values are with respect to the ground terminal, pin 8.

(2) The reference regulator may be bypassed for operation from a fixed 5 V supply by connecting the  $V_{CC}$  and reference output pins both to the supply voltage. In this configuration the maximum supply voltage is 6 V.

(3) Consult packaging section of data book for thermal limitations and considerations of package.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	8	40	40	V
	Reference output current	0	20	20	mA
	Current through $C_T$ terminal	-0.03	-2	-2	mA
$R_T$	Timing resistor	1.8	100	100	k $\Omega$
$C_T$	Timing capacitor	0.001	0.1	0.1	$\mu\text{F}$
Operating ambient temperature range	UC1524	-55	125	125	°C
	UC2524	-25	85	85	
	UC3524	0	70	70	

## ELECTRICAL CHARACTERISTICS

these specifications apply for  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$  for the UC1524,  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  for the UC2524, and  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for the UC3524,  $V_{IN} = 20\text{ V}$ , and  $f = 20\text{ kHz}$ ,  $T_A = T_J$ , over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	UC1524/UC2524			UC3524			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>REFERENCE SECTION</b>								
Output voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line regulation	$V_{IN} = 8\text{ V}$ to $40\text{ V}$		10	20		10	30	mV
Load regulation	$I_L = 0\text{ mA}$ to $20\text{ mA}$		20	50		20	50	mV
Ripple rejection	$f = 120\text{ Hz}$ , $T_J = 25^\circ\text{C}$		66			66		dB
Short circuit current limit	$V_{REF} = 0$ , $T_J = 25^\circ\text{C}$		100			100		mA
Temperature stability	Over operating temperature range		0.3%	1%		0.3%	1%	
Long term stability	$T_J = 125^\circ\text{C}$ , $t = 1000\text{ Hrs}$		20			20		mV
<b>OSCILLATOR SECTION</b>								
Maximum frequency	$C_T = 1\text{ nF}$ , $R_T = 2\text{ k}\Omega$		300			300		kHz
Initial accuracy	$R_T$ and $C_T$ constant		5%			5%		
Voltage stability	$V_{IN} = 8\text{ V}$ to $40\text{ V}$ , $T_J = 25^\circ\text{C}$			1%			1%	
Temperature stability	Over operating temperature range			5%			5%	
Output amplitude	$\text{Pin 3}$ , $T_J = 25^\circ\text{C}$		3.5			3.5		V
Output pulse width	$C_T = 0.01\text{ mfd}$ , $T_J = 25^\circ\text{C}$		0.5			0.5		$\mu\text{s}$
<b>ERROR AMPLIFIER SECTION</b>								
Input offset voltage	$V_{CM} = 2.5\text{ V}$		0.5	5		2	10	mV
Input bias current	$V_{CM} = 2.5\text{ V}$		2	10		2	10	$\mu\text{A}$
Open loop voltage gain		72	80		60	80		dB
Common mode voltage	$T_J = 25^\circ\text{C}$	1.8	3.4		1.8	3.4		V
Common mode rejection ratio	$T_J = 25^\circ\text{C}$		70			70		dB
Small signal bandwidth	$A_V = 0\text{ dB}$ , $T_J = 25^\circ\text{C}$		3			3		MHz
Output voltage	$T_J = 25^\circ\text{C}$	0.5	3.8	0.5	0.5	3.8		V
<b>COMPARATOR SECTION</b>								
Duty-cycle	% Each output on	0%	45%	0%	45%			
Input threshold	Zero duty-cycle		1		1			V
	Maximum duty-cycle		3.5		3.5			
Input bias current		1		1		1		$\mu\text{A}$
<b>CURRENT LIMITING SECTION</b>								
Sense voltage	Pin 9 = $2\text{ V}$ with error amplifier set for maximum out, $T_J = 25^\circ\text{C}$	190	200	210	180	200	220	mV
Sense voltage T.C.			0.2			0.2		$\text{mV}/^\circ\text{C}$
Common mode voltage	$T_J = -55^\circ\text{C}$ to $85^\circ\text{C}$ for the $-1\text{ V}$ to $1\text{ V}$ limit	-1		1	-1		1	V
	$T_J = 25^\circ\text{C}$	-0.3		1				
<b>OUTPUT SECTION (EACH OUTPUT)</b>								
Collector-emitter voltage		40			40			V
Collector leakage current	$V_{CE} = 40\text{ V}$	0.1	50		0.1	50		$\mu\text{A}$
Saturation voltage	$I_C = 50\text{ mA}$	1	2		1	2		V
Emitter output voltage	$V_{IN} = 20\text{ V}$	17	18		17	18		V
Rise Time	$R_C = 2\text{ k}\Omega$ , $T_J = 25^\circ\text{C}$		0.2			0.2		$\mu\text{s}$
Fall Time	$R_C = 2\text{ k}\Omega$ , $T_J = 25^\circ\text{C}$		0.1			0.1		$\mu\text{s}$
Total standby current (Note)	$V_{IN} = 40\text{ V}$	8	10		8	10		mA

## PRINCIPLES OF OPERATION

The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor ( $R_T$ ), and one timing capacitor ( $C_T$ ).  $R_T$  establishes a constant charging current for  $C_T$ . This results in a linear voltage ramp at  $C_T$ , which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5 V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at  $C_T$ . The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor ( $Q_1$  or  $Q_2$ ) by the pulse-steering

flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of  $C_T$ . The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator. Note that for buck regulator topologies, the two outputs can be wire-ORed for an effective 0-90% duty cycle range. With this connection, the output frequency is the same as the oscillator frequency. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier or to provide additional control to the regulator.

## TYPICAL CHARACTERISTICS

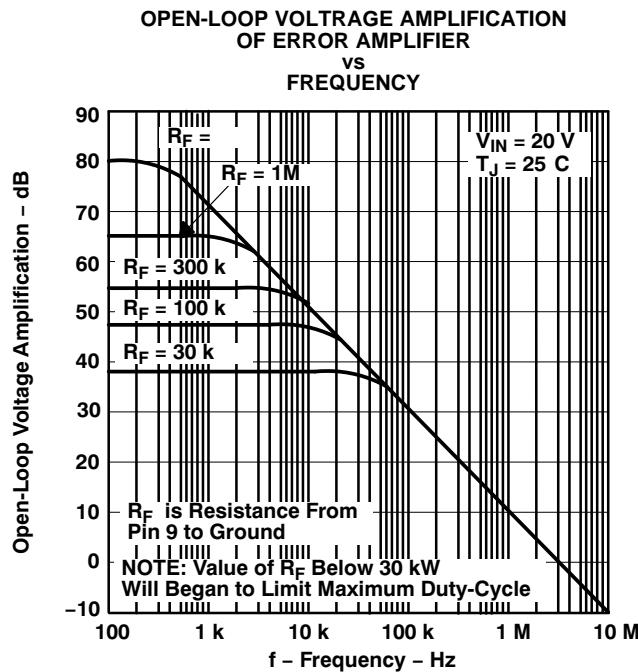


Figure 1.

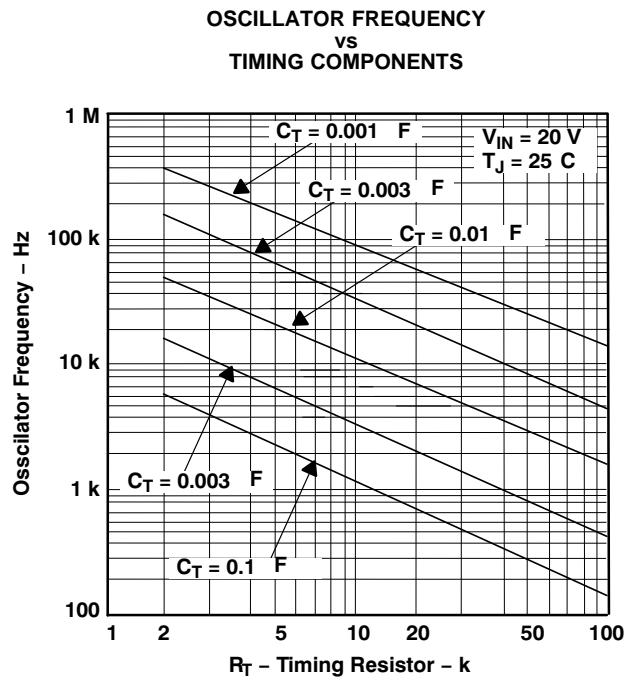


Figure 2.

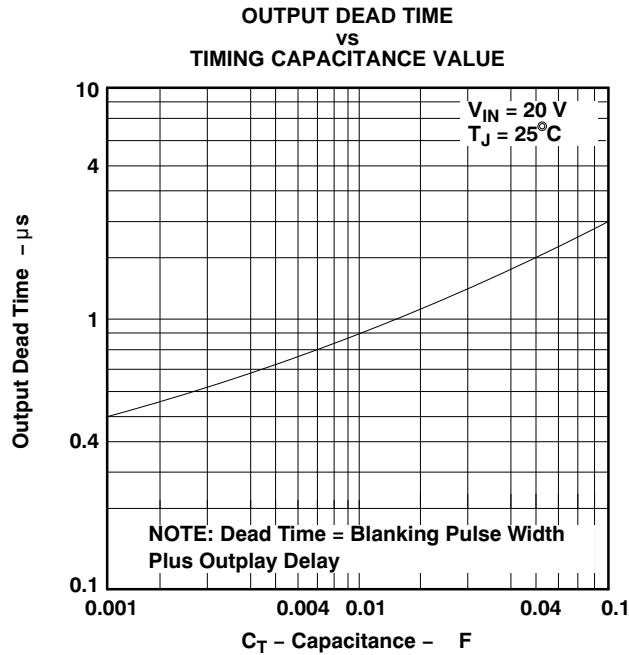


Figure 3.

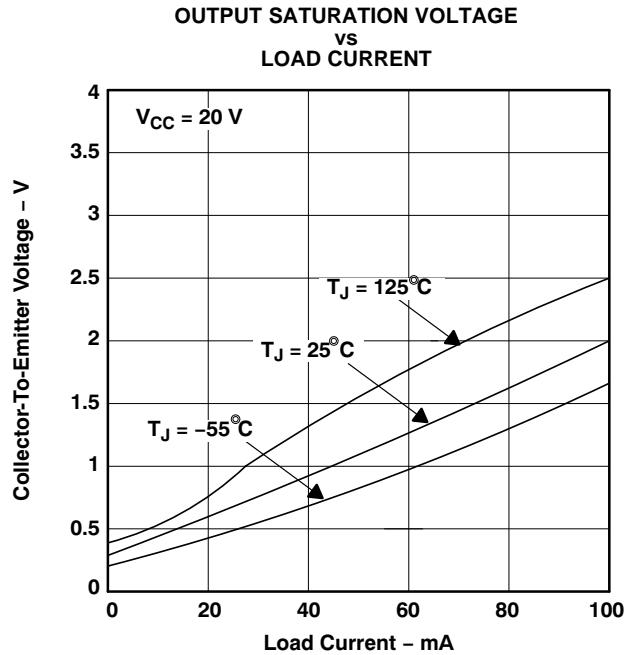


Figure 4.

## APPLICATION INFORMATION

### OSCILLATOR

The oscillator controls the frequency of the UC1524 and is programmed by  $R_T$  and  $C_T$  according to the approximate formula:

$$f = \frac{1.18}{R_T C_T} \quad (1)$$

where

$R_T$  is in k $\Omega$

$C_T$  is in  $\mu\text{F}$

$f$  is in kHz

Practical values of  $C_T$  fall between 1 nF and 100 nF. Practical values of  $R_T$  fall between 1.8 k $\Omega$  and 100 k $\Omega$ . This results in a frequency range typically from 120 Hz to 500 kHz.

### BLANKING

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of  $C_T$ . If small values of  $C_T$  are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100 pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit in Figure 5.

### SYNCHRONOUS OPERATIONS

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 k $\Omega$ . In this configuration  $R_T$ ,  $C_T$  must be selected for a clock period slightly greater than that of the external clock.

If two or more UC1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all  $C_T$  terminals connected to single timing capacitor, and the timing resistor connected to a single  $R_T$  terminal.

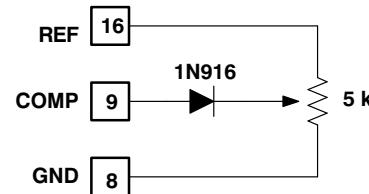


Figure 5. Error Amplifier Clamp

The other  $R_T$  terminals can be left open or shorted to  $V_{REF}$ . Minimum lead lengths should be used between the  $C_T$  terminals.

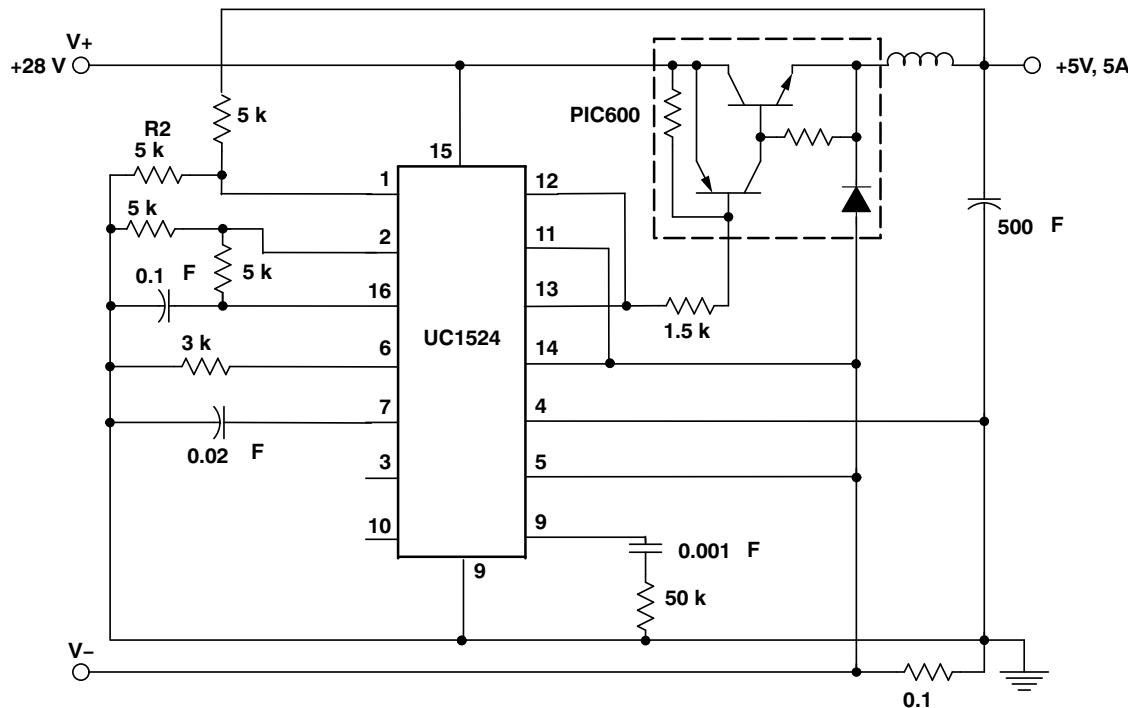


Figure 6. Single-Ended LC Switching Regulator Circuit

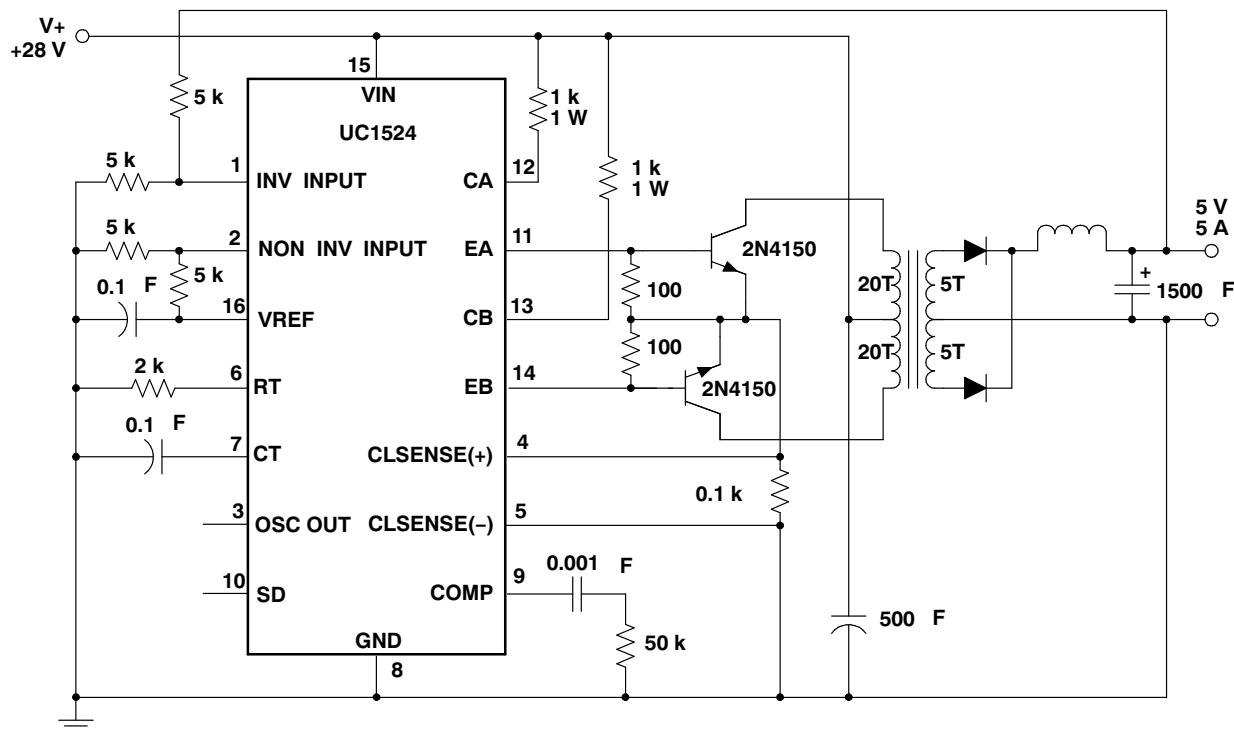


Figure 7. Push-Pull Transformer Coupled Circuit

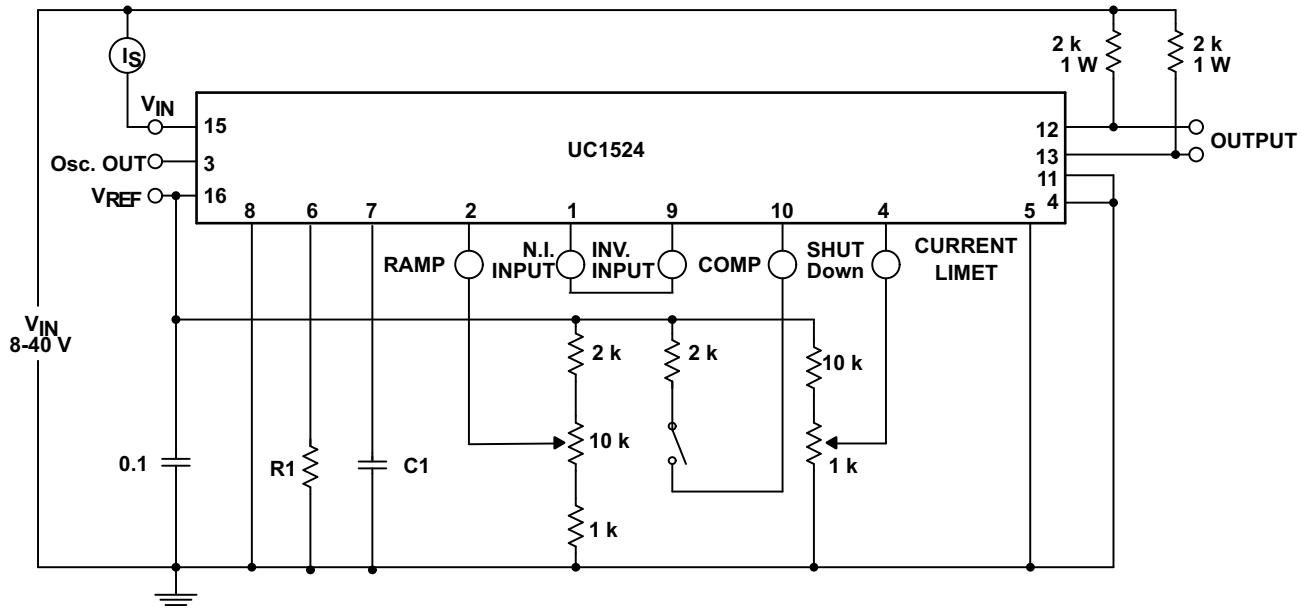


Figure 8. Open Loop Test Circuit

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC2524DW	Obsolete	Production	SOIC (DW)   16	-	-	Call TI	Call TI	-25 to 85	UC2524DW
UC3524D	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524D
UC3524D.A	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524D
UC3524DW	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524DW
UC3524DW.A	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524DW
UC3524DWTR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524DW
UC3524DWTR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524DW

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

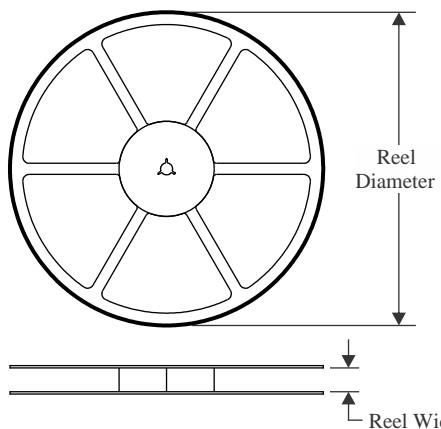
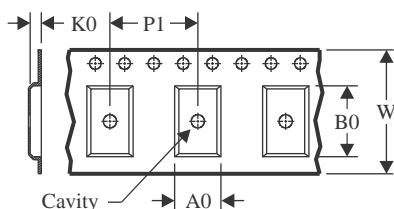
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

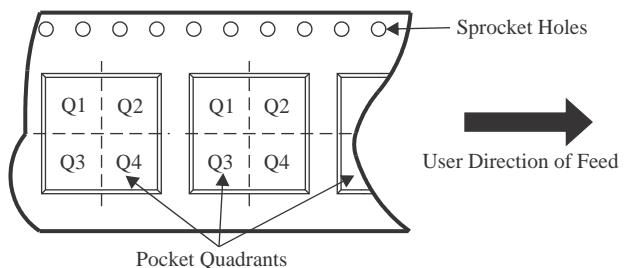
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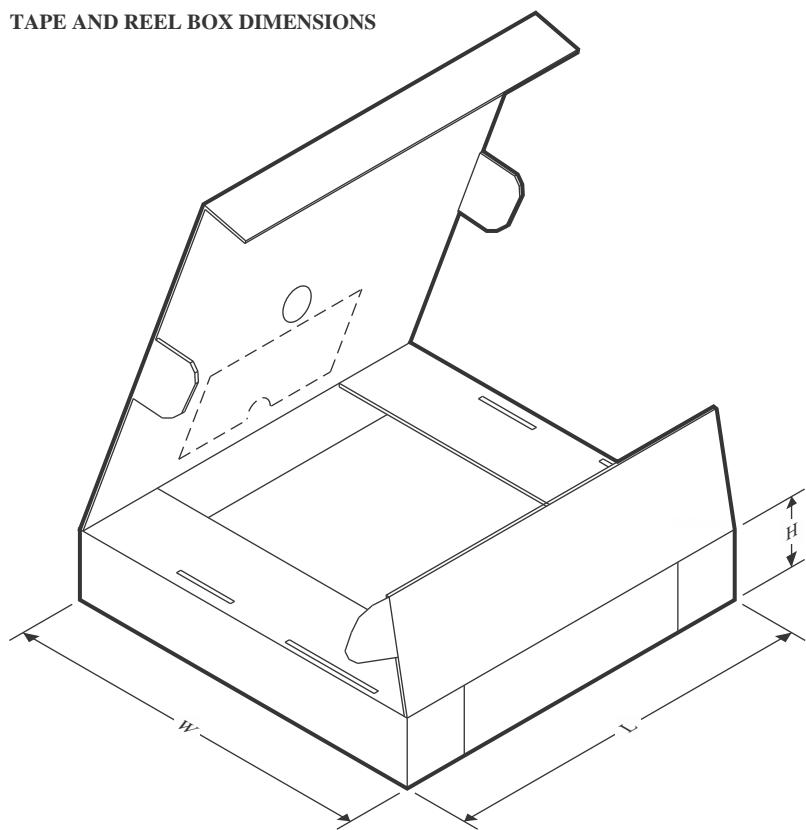
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3524DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3524DWTR	SOIC	DW	16	2000	353.0	353.0	32.0

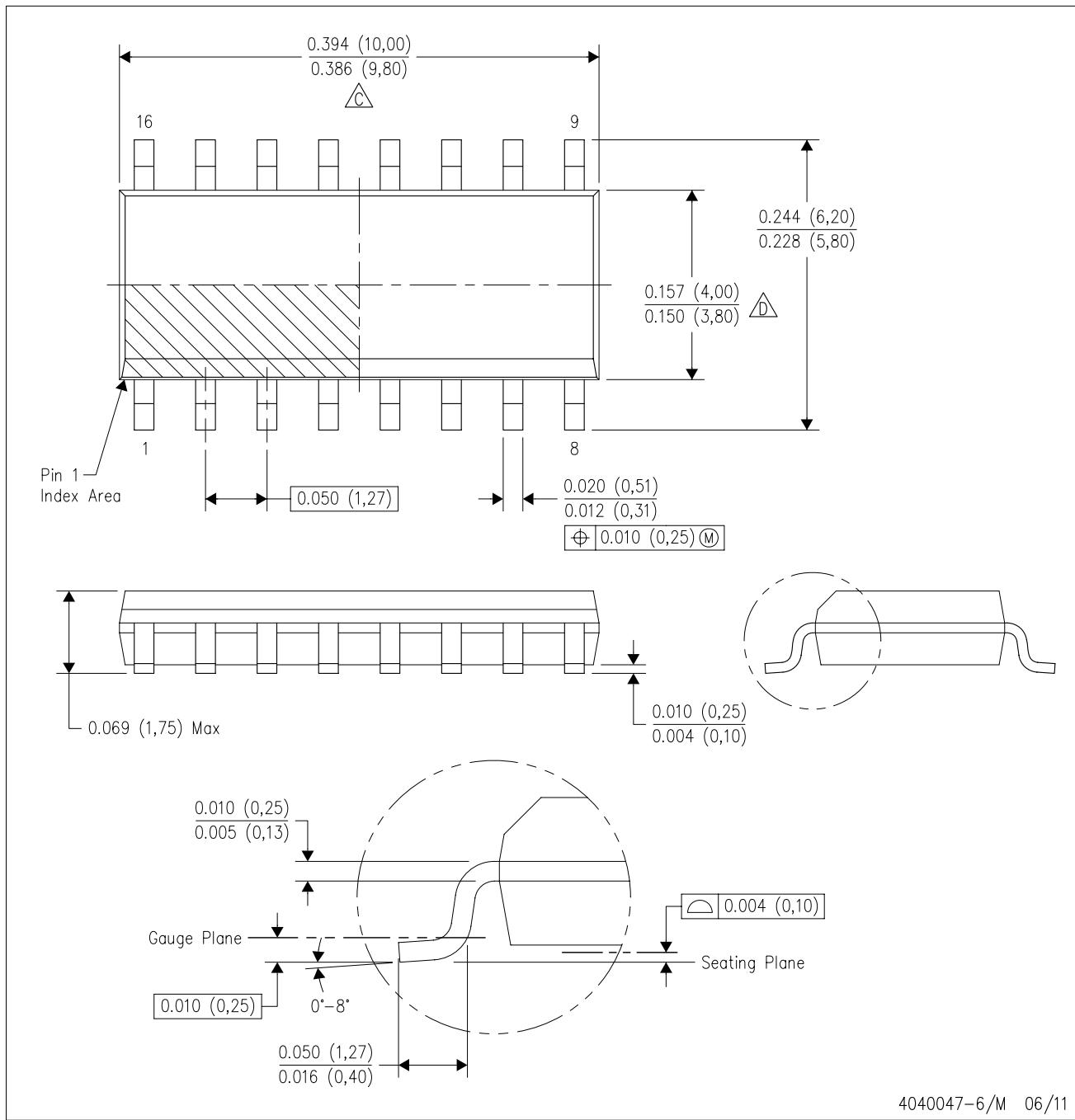
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UC3524D	D	SOIC	16	40	506.6	8	3940	4.32
UC3524D.A	D	SOIC	16	40	506.6	8	3940	4.32
UC3524DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3524DW.A	DW	SOIC	16	40	507	12.83	5080	6.6

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

# GENERIC PACKAGE VIEW

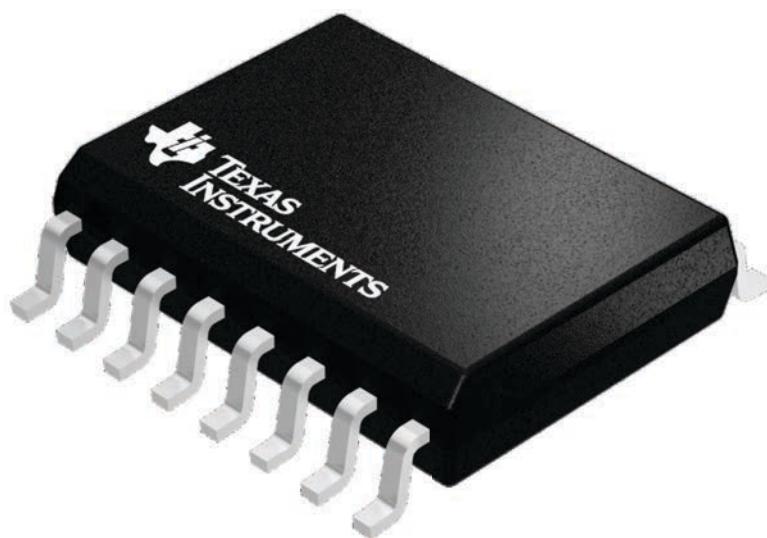
**DW 16**

**SOIC - 2.65 mm max height**

**7.5 x 10.3, 1.27 mm pitch**

**SMALL OUTLINE INTEGRATED CIRCUIT**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

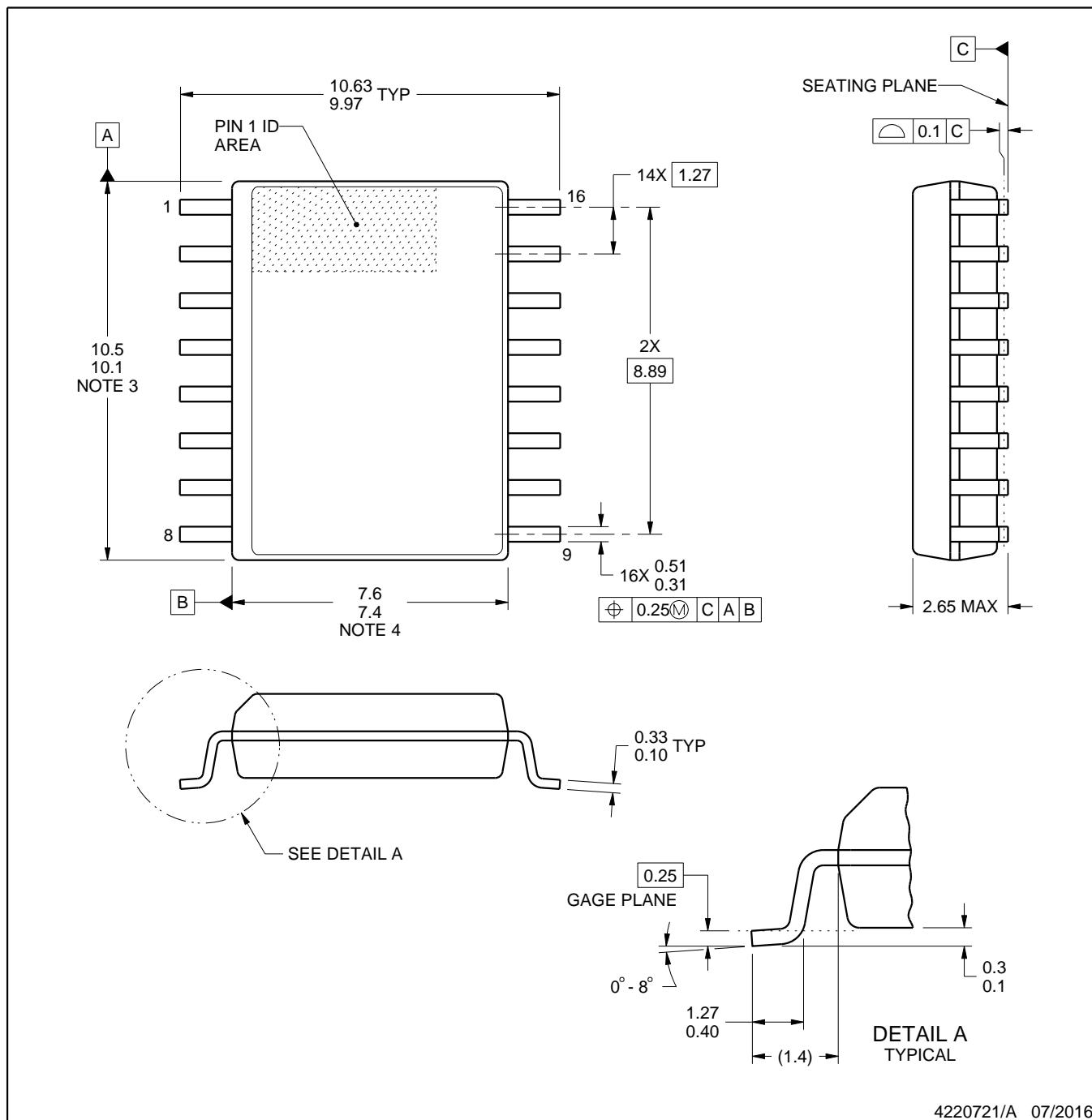


## PACKAGE OUTLINE

**DW0016A**

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

## NOTES:

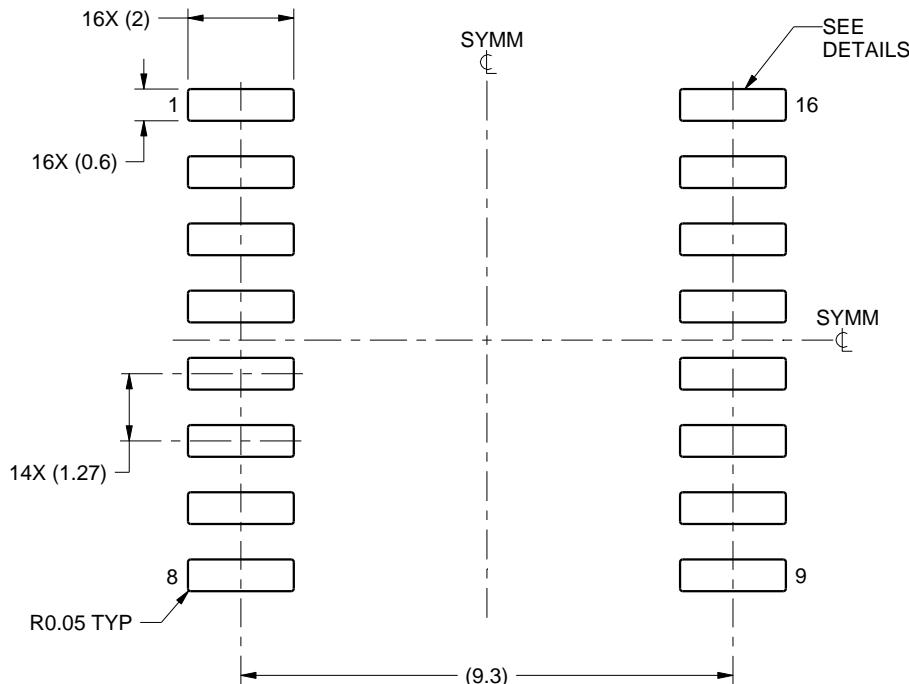
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

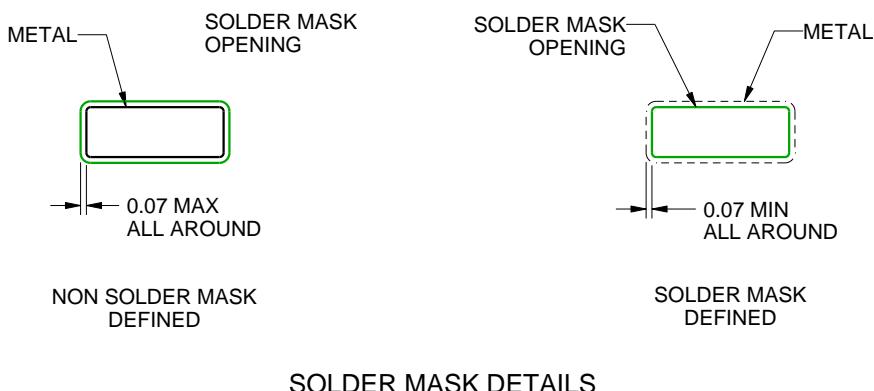
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

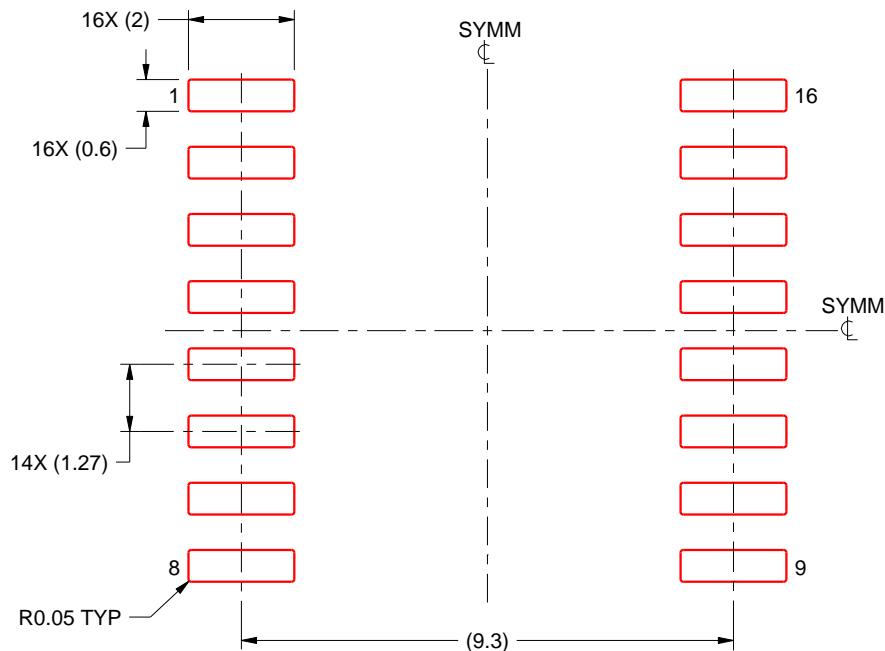
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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