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74LCX112

Low Voltage Dual J-K Negative Edge-Triggered Flip-Flop with 5V Tolerant Inputs

General Description

The LCX112 is a dual J-K flip-flop. Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs with Q, Q outputs. These devices are edge sensitive and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input. LCX devices are designed for low voltage (3.3V or 2.5V) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX112 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

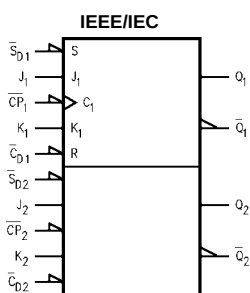
- 5V tolerant inputs
- 2.3V–3.6V V_{CC} specifications provided
- 7.5 ns t_{PD} max ($V_{CC} = 3.3V$), 10 μA I_{CC} max
- Power down high impedance inputs and outputs
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 2000V

Ordering Code:

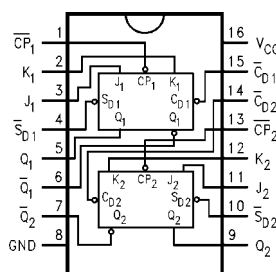
Order Number	Package Number	Package Description
74LCX112M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74LCX112SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX112MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
J ₁ , J ₂ , K ₁ , K ₂	Data Inputs
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)
$\overline{CD}_1$, $\overline{CD}_2$	Direct Clear Inputs (Active LOW)
$\overline{SD}_1$, $\overline{SD}_2$	Direct Set Inputs (Active LOW)
Q ₁ , Q ₂ , $\overline{Q}_1$, $\overline{Q}_2$	Outputs

74LCX112 Low Voltage Dual J-K Negative Edge-Triggered Flip-Flop with 5V Tolerant Inputs

Truth Table

(Each half)

Inputs					Outputs	
$\overline{S_D}$	$\overline{C_D}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\sim$	h	h	$\overline{Q_0}$	Q_0
H	H	$\sim$	l	h	L	H
H	H	$\sim$	h	l	H	L
H	H	$\sim$	l	l	Q_0	$\overline{Q_0}$
H	H	H	X	X	Q_0	$\overline{Q_0}$

H(h) = HIGH Voltage Level

L(l) = LOW Voltage Level

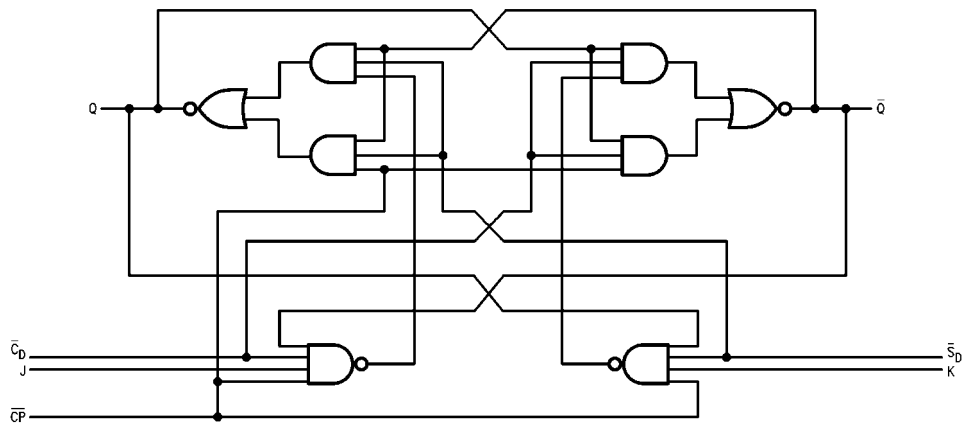
X = Immaterial

$\sim$ = HIGH-to-LOW Clock Transition

$Q_0(\overline{Q_0})$ = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

Logic Diagram



Absolute Maximum Ratings ^(Note 1)				
Symbol	Parameter	Value	Conditions	Units
V _{CC}	Supply Voltage	−0.5 to +7.0		V
V _I	DC Input Voltage	−0.5 to +7.0		V
V _O	DC Output Voltage	−0.5 to V _{CC} + 0.5	Output in HIGH or LOW State (Note 2)	V
I _{IK}	DC Input Diode Current	−50	V _I < GND	mA
I _{OK}	DC Output Diode Current	−50 +50	V _O < GND V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supple Current per Supply Pin	±100		mA
I _{GND}	DC Ground Current per Ground Pin	±100		mA
T _{STG}	Storage Temperature	−65 to 150		°C

Recommended Operating Conditions ^(Note 3)

Symbol	Parameter	Min	Max	Units
V _{CC}	Supply Voltage	Operating Data Retention	2.0 3.6	V
V _I	Input Voltage	0	5.5	V
V _O	Output Voltage	HIGH or LOW State	0 V _{CC}	V
I _{OH} /I _{OL}	Output Current	V _{CC} = 3.0V – 3.6V V _{CC} = 2.7V – 3.0V V _{CC} = 2.3V – 2.7V	±24 ±12 ±8	mA
T _A	Free-Air Operating Temperature	−40	85	°C
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V	0	10	ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum rating must be observed.

Note 3: Unused Inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 40°C to +85°C		Units
				Min	Max	
V _{IH}	HIGH Level Input Voltage		2.3 – 2.7 2.7 – 3.6	1.7 2.0		V
V _{IL}	LOW Level Input Voltage		2.3 – 2.7 2.7 – 3.6		0.7 0.8	V
V _{OH}	HIGH Level Output Voltage	I _{OH} = −100μA I _{OH} = −8 mA I _{OH} = −12 mA I _{OH} = −18 mA I _{OH} = −24 mA	2.3 – 3.6 2.3 2.7 3.0 3.0	V _{CC} − 0.2 1.8 2.2 2.4 2.2	0.7	V
V _{OL}	LOW Level Output Voltage	I _{OL} = 100μA I _{OL} = 8mA I _{OL} = 12 mA I _{OL} = 16 mA I _{OL} = 24 mA	2.3 – 3.6 2.3 2.7 3.0 3.0		0.6 0.2 0.4 0.4 0.55	V
I _I	Input Leakage Current	0 ≤ I _I ≤ 5.5V	2.3 – 3.6		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND 3.6V ≤ V _I ≤ 5.5V	2.3 – 3.6 2.3 – 3.6		10 ±10	μA
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} − 0.6V	2.3 – 3.6		500	μA

AC Electrical Characteristics

Symbol	Parameters	T _A = 40°C to 85°C, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		
		C _L =50 pF		C _L = 50 pF		C _L =30 pF		
		Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	150		150		150		MHz
t _{PHL}	Propagation Delay	1.5	7.5	1.5	8.0	1.5	9.0	ns
t _{PLH}	$\overline{CP}_n$ to Q _n or $\overline{Q}_n$	1.5	7.5	1.5	8.0	1.5	9.0	
t _{PHL}	Propagation Delay	1.5	7.0	1.5	8.0	1.5	8.4	ns
t _{PLH}	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q _n or $\overline{Q}_n$	1.5	7.0	1.7	8.0	1.5	8.4	
t _S	Setup Time	2.5		2.5		4.0		ns
t _H	Hold Time	1.5		1.5		2.0		ns
t _W	Pulse Width $\overline{CP}$	3.3		3.3		4.0		ns
t _W	Pulse Width ($\overline{C}_D$, $\overline{S}_D$)	3.3		3.3		4.0		ns
t _{REC}	Recovery Time	2.0		2.5		4.5		ns
t _{OSHL}	Output to Output Skew		1.0					ns
t _{OSLH}	(Note 4)		1.0					

Note 4: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^\circ\text{C}$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50\text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$ $C_L = 30\text{ pF}, V_{IH} = 2.5V, V_{IL} = 0V$	3.3 2.5	0.8 0.6	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50\text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$ $C_L = 30\text{ pF}, V_{IH} = 2.5V, V_{IL} = 0V$	3.3 2.5	-0.8 -0.6	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0V \text{ or } V_{CC}$	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}, f = 10\text{ MHz}$	25	pF

AC Loading and Waveforms Generic for LCX Family

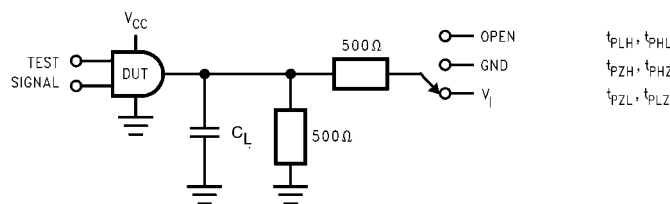
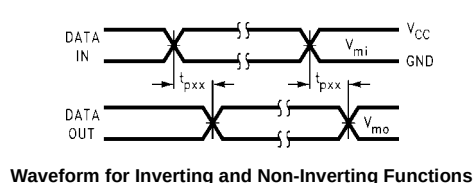
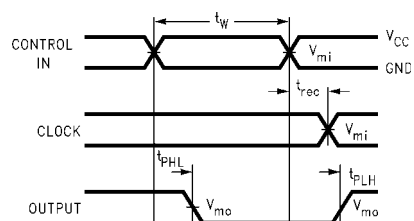


FIGURE 1. AC Test Circuit
(C_L includes probe and jig capacitance)

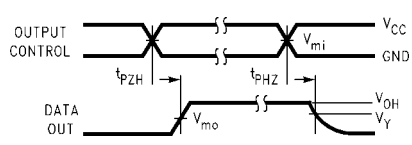
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH}, t_{PHZ}	GND



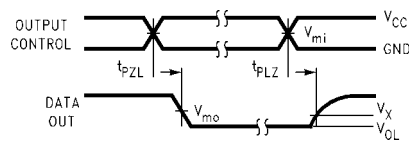
Waveform for Inverting and Non-Inverting Functions



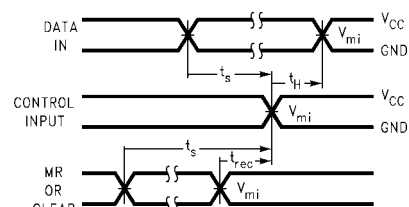
Propagation Delay, Pulse Width and t_{rec} Waveforms



3-STATE Output High Enable and Disable Times for Logic



3-STATE Output Low Enable and Disable Times for Logic



Setup Time, Hold Time and Recovery Time for Logic

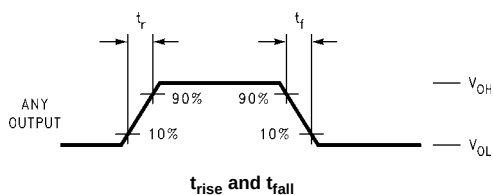
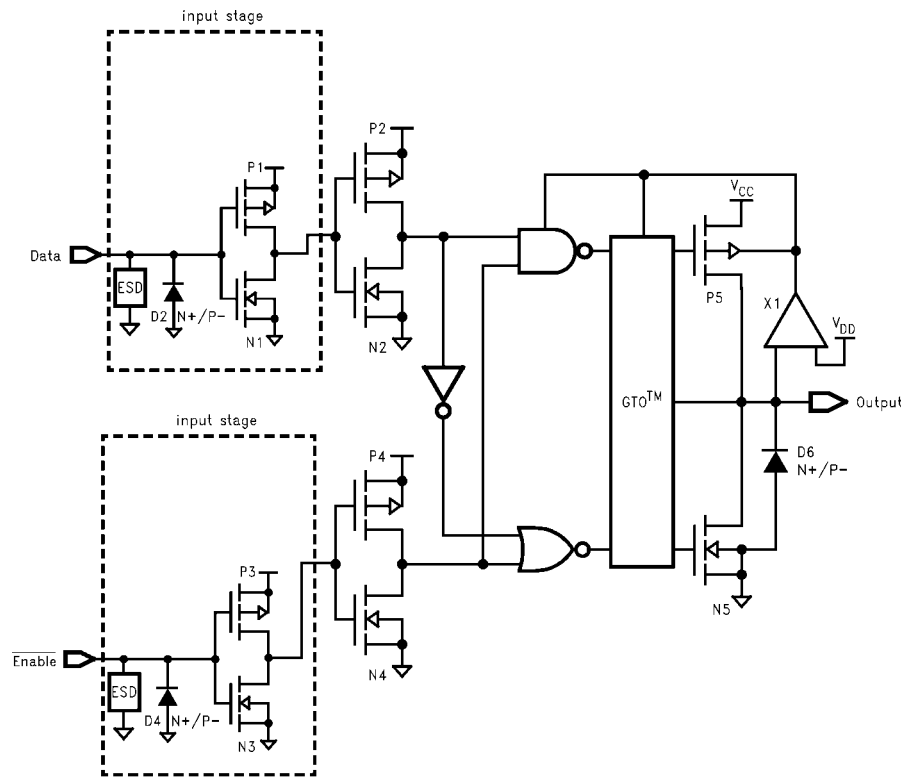


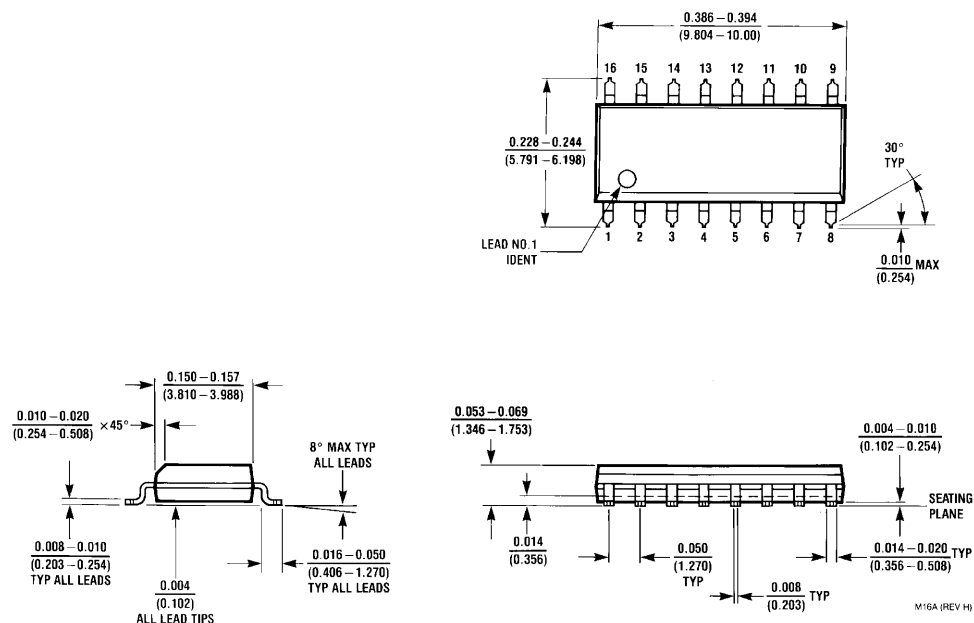
FIGURE 2. Waveforms
(Input Pulse Characteristics; $f=1MHz$, $t_r=t_f=3ns$)

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family

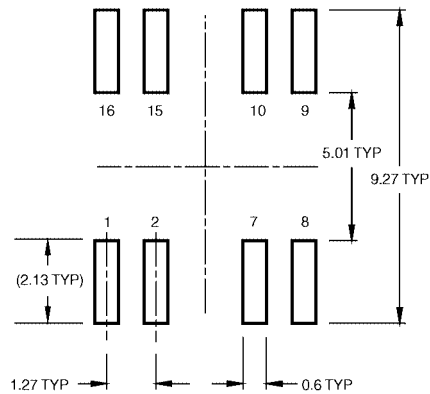
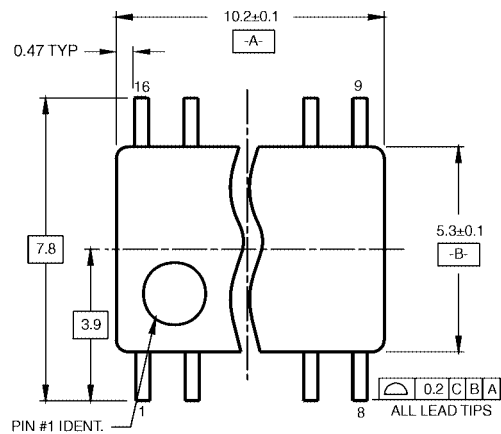


Physical Dimensions inches (millimeters) unless otherwise noted

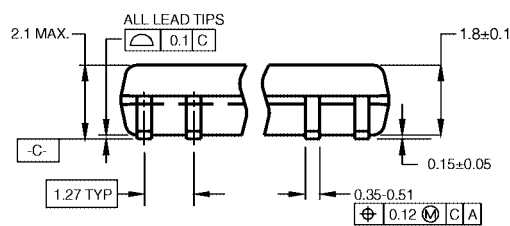


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A**

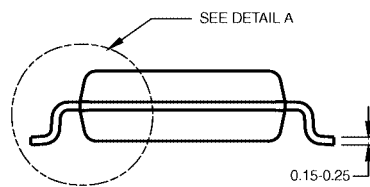
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



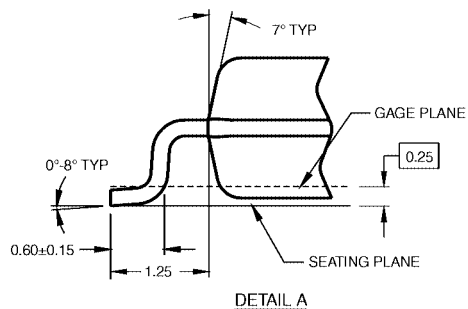
DIMENSIONS ARE IN MILLIMETERS



NOTES:

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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

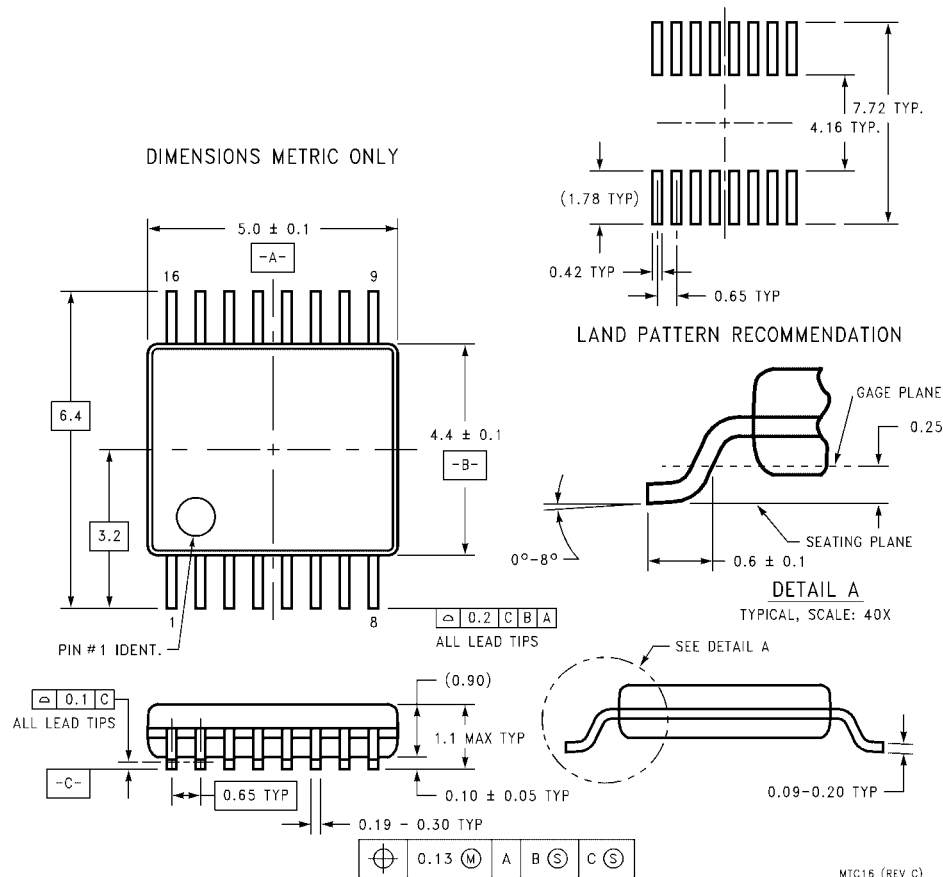
M16DRevB1



DETAIL A

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

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