

INVERTER GRADE THYRISTORS

Stud Version

Features

- All diffused design
- Center amplifying gate
- Guaranteed high dv/dt
- Guaranteed high di/dt
- High surge current capability
- Low thermal impedance
- High speed performance

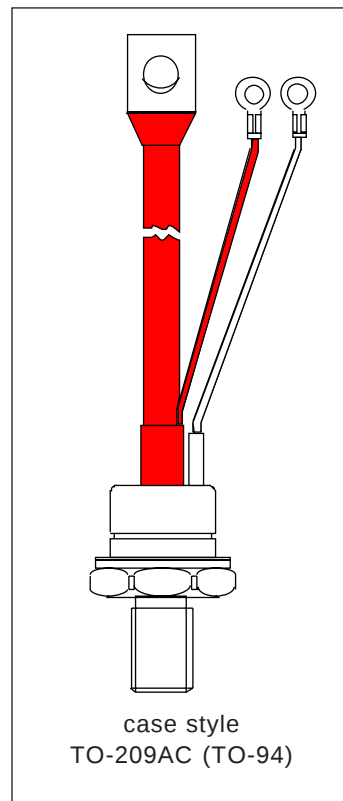
105A

Typical Applications

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

Major Ratings and Characteristics

Parameters	ST103S	Units
$I_{T(AV)}$	105	A
@ T_C	85	°C
$I_{T(RMS)}$	165	A
I_{TSM} @ 50Hz	3000	A
@ 60Hz	3150	A
I^2t @ 50Hz	45	KA ² s
@ 60Hz	41	KA ² s
V_{DRM}/V_{RRM}	400 to 800	V
t_q range	10 to 25	μs
T_J	- 40 to 125	°C



ST103S Series

Bulletin I25183 rev. B 03/94

International
IR Rectifier

ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{DRM}/V_{RRM} , maximum repetitive peak voltage V	V_{RSM} , maximum non-repetitive peak voltage V	I_{DRM}/I_{RRM} max. @ $T_J = T_J$ max. mA
ST103S	04	400	500	30
	08	800	900	

Current Carrying Capability

Frequency							Units
50Hz	280	180	440	330	4730	3630	A
400Hz	310	200	470	300	2500	1850	
1000Hz	320	200	480	310	1530	1090	
2500Hz	340	210	490	320	840	580	
Recovery voltage Vr	50	50	50	50	50	50	V
Voltage before turn-on Vd	V _{DRM}		V _{DRM}		V _{DRM}		
Rise of on-state current di/dt	50	50	-	-	-	-	A/µs
Case temperature	60	85	60	85	60	85	°C
Equivalent values for RC circuit	22Ω / 0.15µF		22Ω / 0.15µF		22Ω / 0.15µF		

On-state Conduction

Parameter	ST103S	Units	Conditions
$I_{T(AV)}$ Max. average on-state current @ Case temperature	105 85	A °C	180° conduction, half sine wave
$I_{T(RMS)}$ Max. RMS on-state current	165	A	DC @ 76°C case temperature
I_{TSM} Max. peak, one half cycle, non-repetitive surge current	3000		t = 10ms No voltage reappplied
	3150		t = 8.3ms
	2530		t = 10ms 100% V_{RRM} reappplied
	2650		t = 8.3ms
I^2t Maximum I^2t for fusing	45	KA²s	t = 10ms No voltage reappplied
	41		t = 8.3ms
	32		t = 10ms 100% V_{RRM} reappplied
	29		t = 8.3ms
$I^2\sqrt{t}$ Maximum $I^2\sqrt{t}$ for fusing	450	KA²√s	t = 0.1 to 10ms, no voltage reappplied

On-state Conduction

Parameter	ST103S	Units	Conditions
V_{TM} Max. peak on-state voltage	1.73	V	$I_{TM} = 300A$, $T_J = T_J \text{ max}$, $t_p = 10\text{ms}$ sine wave pulse
$V_{T(TO)1}$ Low level value of threshold voltage	1.32		$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J \text{ max}$.
$V_{T(TO)2}$ High level value of threshold voltage	1.35		$(I > \pi \times I_{T(AV)})$, $T_J = T_J \text{ max}$.
r_{t1} Low level value of forward slope resistance	1.40	m Ω	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J \text{ max}$.
r_{t2} High level value of forward slope resistance	1.30		$(I > \pi \times I_{T(AV)})$, $T_J = T_J \text{ max}$.
I_H Maximum holding current	600	mA	$T_J = 25^\circ\text{C}$, $I_T > 30A$
I_L Typical latching current	1000		$T_J = 25^\circ\text{C}$, $V_A = 12V$, $R_a = 6\Omega$, $I_G = 1A$

Switching

Parameter	ST103S	Units	Conditions
di/dt Max. non-repetitive rate of rise of turned-on current	1000	A/ μs	$T_J = T_J \text{ max}$, $V_{DRM} = \text{rated } V_{DRM}$ $I_{TM} = 2 \times di/dt$
t_d Typical delay time	0.80	μs	$T_J = 25^\circ\text{C}$, $V_{DM} = \text{rated } V_{DRM}$, $I_{TM} = 50A \text{ DC}$, $t_p = 1\mu\text{s}$ Resistive load, Gate pulse: 10V, 5 Ω source
t_q Max. turn-off time	Min 10 Max 25		$T_J = T_J \text{ max}$, $I_{TM} = 100A$, commutating $di/dt = 10A/\mu\text{s}$ $V_R = 50V$, $t_p = 200\mu\text{s}$, dv/dt : see table in device code

Blocking

Parameter	ST103S	Units	Conditions
dv/dt Maximum critical rate of rise of off-state voltage	500	V/ μs	$T_J = T_J \text{ max}$., linear to 80% V_{DRM} , higher value available on request
I_{RRM} I_{DRM} Max. peak reverse and off-state leakage current	30	mA	$T_J = T_J \text{ max}$, rated V_{DRM}/V_{RRM} applied

Triggering

Parameter	ST103S	Units	Conditions
P_{GM} Maximum peak gate power	40	W	$T_J = T_J \text{ max}$, $f = 50\text{Hz}$, $d\% = 50$
$P_{G(AV)}$ Maximum average gate power	5		
I_{GM} Max. peak positive gate current	5	A	$T_J = T_J \text{ max}$, $t_p \leq 5\text{ms}$
$+V_{GM}$ Maximum peak positive gate voltage	20	V	$T_J = T_J \text{ max}$, $t_p \leq 5\text{ms}$
$-V_{GM}$ Maximum peak negative gate voltage	5		
I_{GT} Max. DC gate current required to trigger	200	mA	$T_J = 25^\circ\text{C}$, $V_A = 12V$, $R_a = 6\Omega$
V_{GT} Max. DC gate voltage required to trigger	3	V	
I_{GD} Max DC gate current not to trigger	20	mA	$T_J = T_J \text{ max}$, rated V_{DRM} applied
V_{GD} Max. DC gate voltage not to trigger	0.25	V	

ST103S Series

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International
IOR Rectifier

Thermal and Mechanical Specifications

Parameter	ST103S	Units	Conditions
T _j Max. junction operating temperature range	-40 to 125	°C	
T _{stg} Max. storage temperature range	-40 to 150		
R _{thJC} Max. thermal resistance, junction to case	0.195	K/W	DC operation
R _{thCS} Max. thermal resistance, case to heatsink	0.08		Mounting surface, smooth, flat and greased
T Mounting torque, ± 10%	15.5 (137)	Nm (lbf-in)	Non lubricated threads
	14 (120)	Nm (lbf-in)	Lubricated threads
wt Approximate weight	130	g	
Case style	TO-209AC (TO-94)		See Outline Table

ΔR_{thJC} Conduction

(The following table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC)

Conduction angle	Sinusoidal conduction	Rectangular conduction	Units	Conditions
180°	0.034	0.025	K/W	T _j = T _j max.
120°	0.040	0.042		
90°	0.052	0.056		
60°	0.076	0.079		
30°	0.126	0.127		

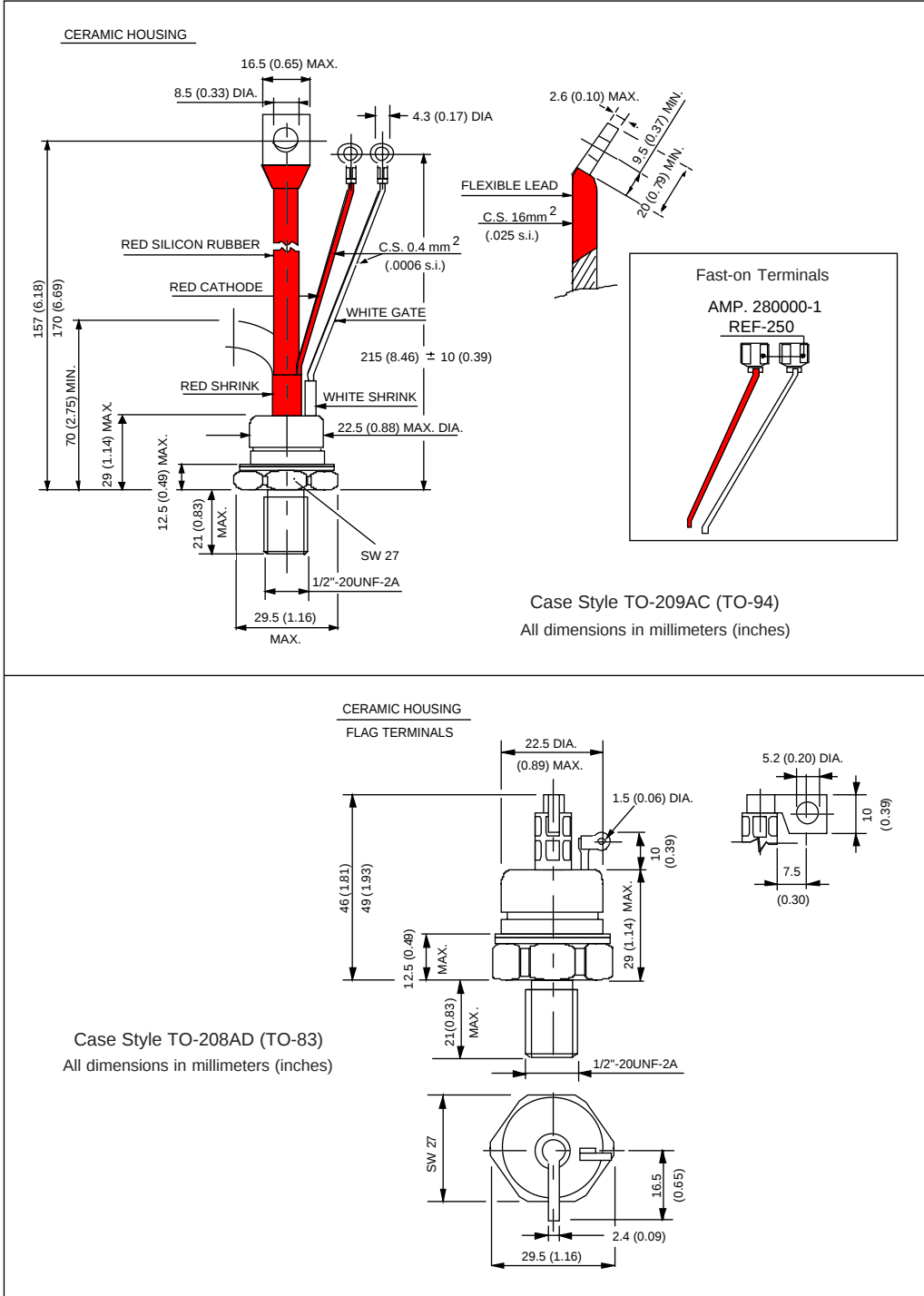
Ordering Information Table

Device Code ST103S08PFN0 12345678910									
1	- Thyristor								
2	- Essential part number								
3	- 3 = Fast turn off								
4	- S = Compression bonding Stud								
5	- Voltage code: Code x 100 = V _{RRM} (See Voltage Ratings table)								
6	- P = Stud Base 1/2" 20UNF								
7	- Reapplied dv/dt code (for t _q test condition)								
8	- t _q code								
9	- 0 = Eyelet terminals (Gate and Aux. Cathode Leads)								
	1 = Fast-on terminals (Gate and Aux. Cathode Leads)								
	2 = Flag terminals (For Cathode and Gate Terminals)								
10	- Critical dv/dt:								
	None = 500V/μsec (Standard value)								
	L = 1000V/μsec (Special selection)								

dv/dt - t _q combinations available					
dv/dt (V/μs)	20	50	100	200	400
t _q (μs)	10	CN	DN	EN	FN *
	12	CM	DM	EM	FM
	15	CL	DL	EL	FL *
	18	CP	DP	EP	FP
	20	CK	DK	EK	FK
	25	--	--	--	HJ

*Standard part number.
All other types available only on request.

Outline Table



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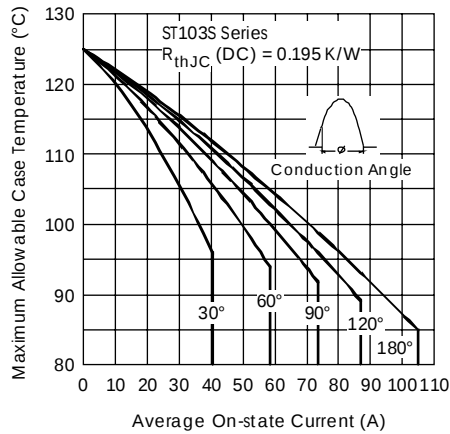


Fig. 1 - Current Ratings Characteristics

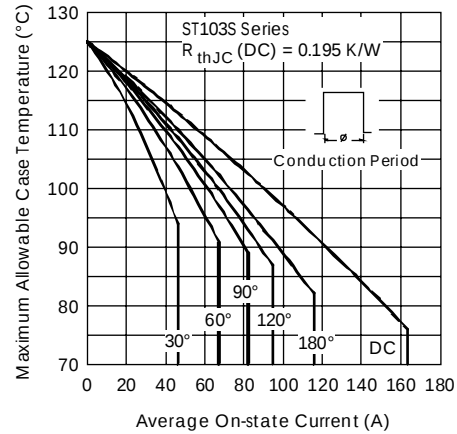


Fig. 2 - Current Ratings Characteristics

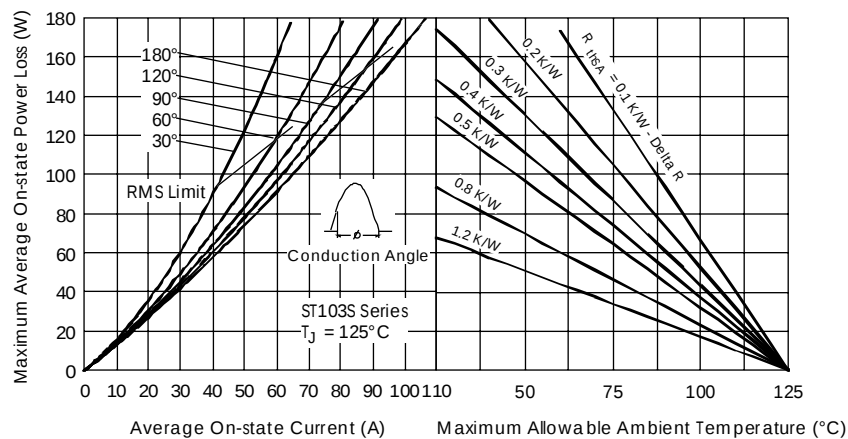


Fig. 3 - On-state Power Loss Characteristics

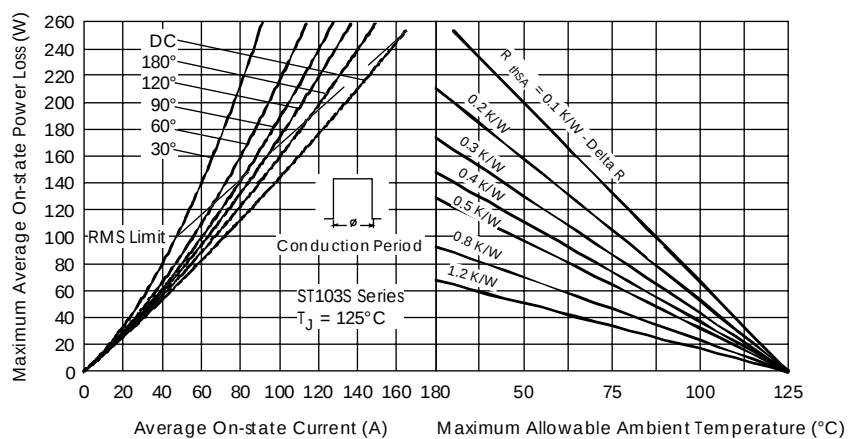


Fig. 4 - On-state Power Loss Characteristics

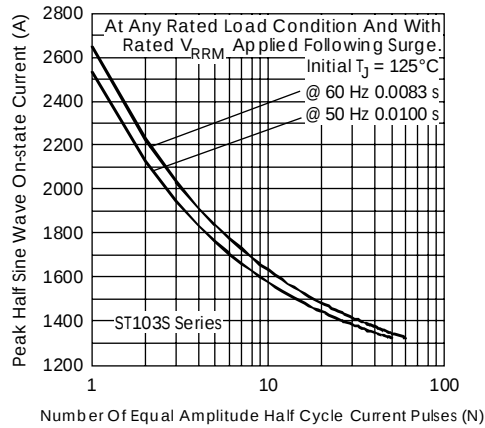


Fig. 5 - Maximum Non-repetitive Surge Current

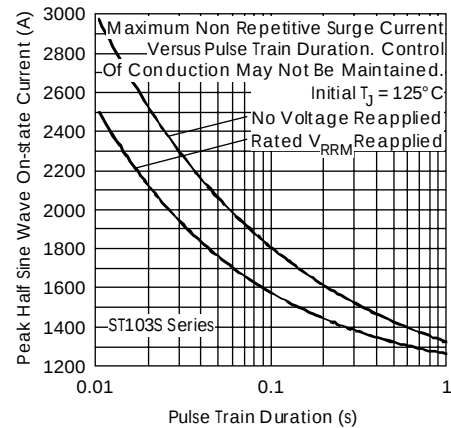


Fig. 6 - Maximum Non-repetitive Surge Current

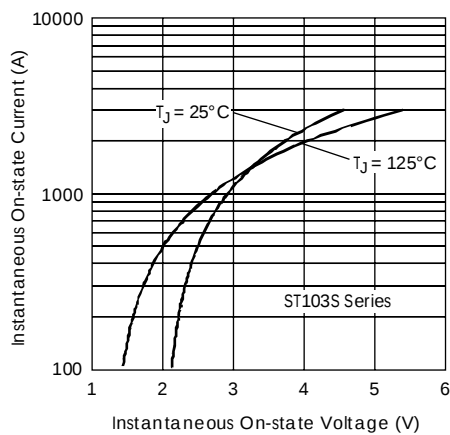


Fig. 7 - On-state Voltage Drop Characteristics

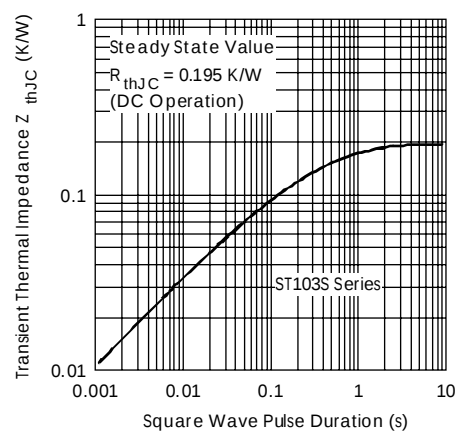


Fig. 8 - Thermal Impedance Z_{thJC} Characteristic

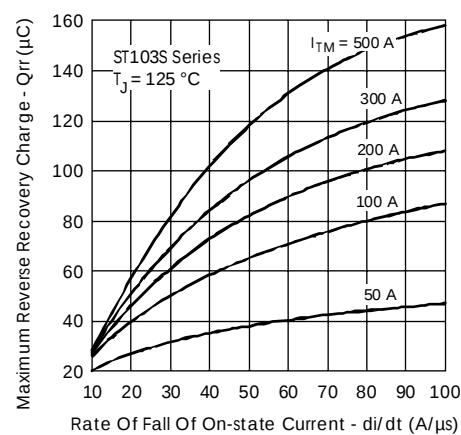


Fig. 9 - Reverse Recovered Charge Characteristics

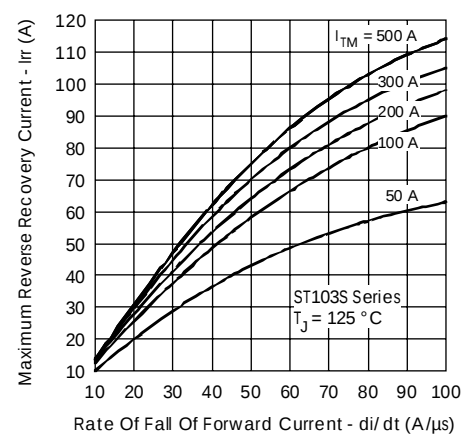


Fig. 10 - Reverse Recovery Current Characteristics

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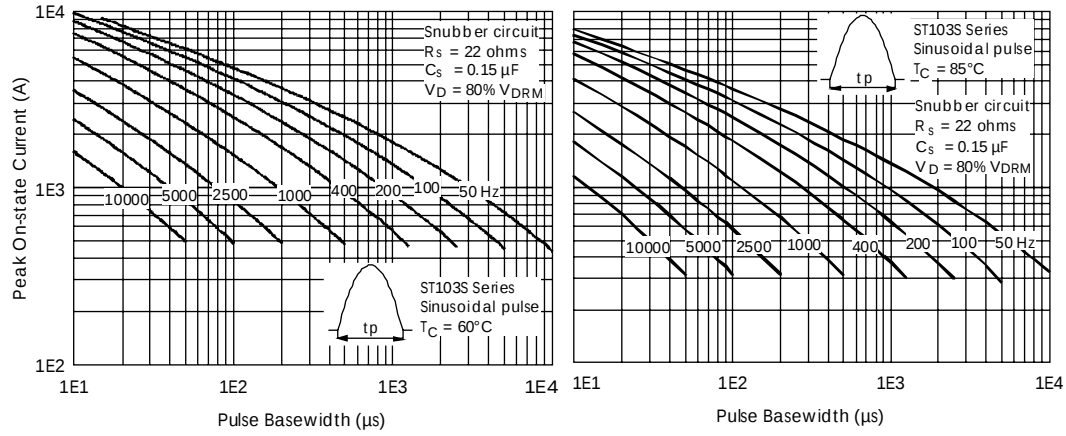


Fig. 11 - Frequency Characteristics

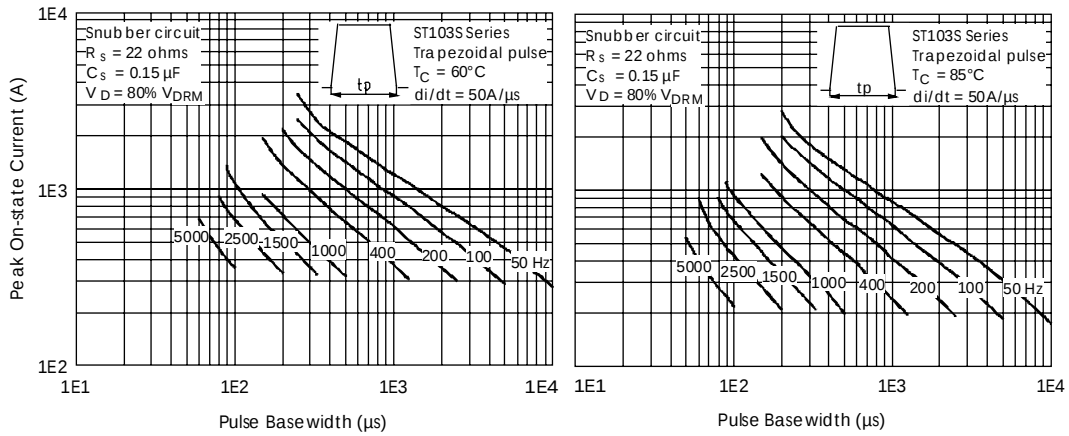


Fig. 12 - Frequency Characteristics

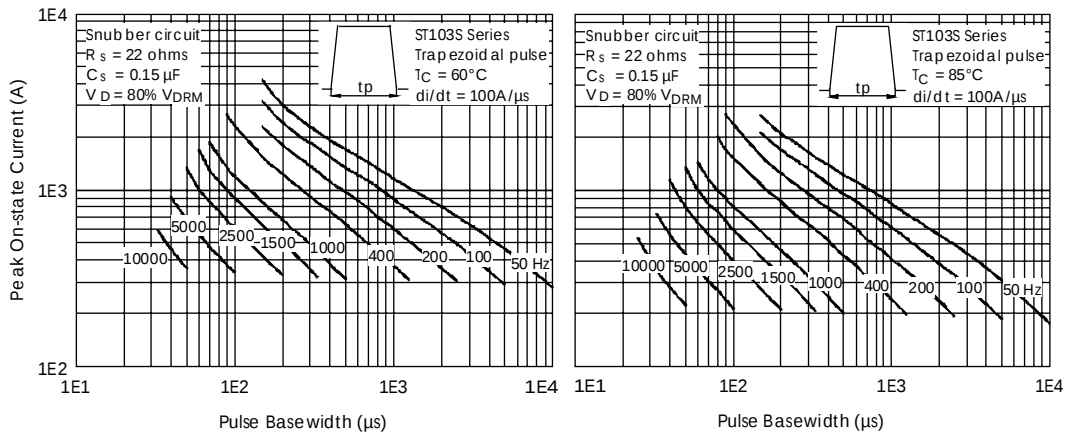


Fig. 13 - Frequency Characteristics

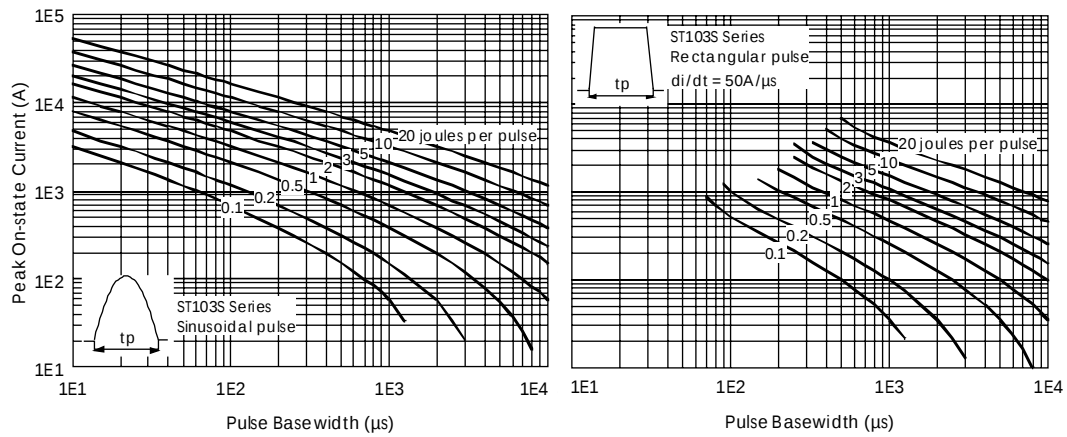


Fig. 14 - Maximum On-state Energy Power Loss Characteristics

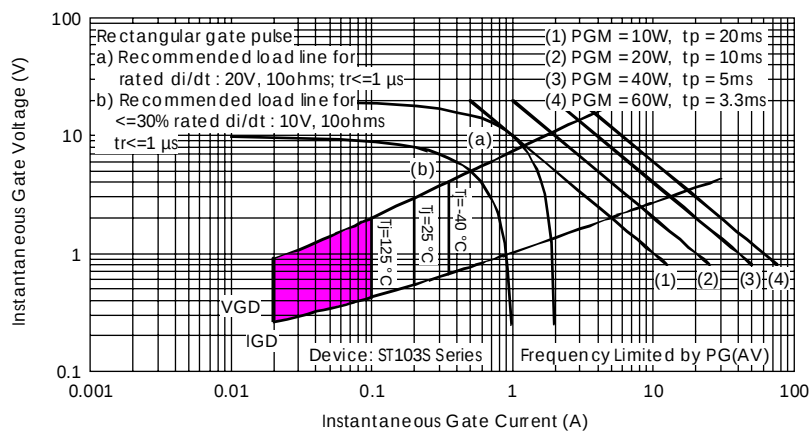


Fig. 15 - Gate Characteristics