



DAC7644

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16-Bit, Quad Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **LOW POWER:** 10mW
- **UNIPOLAR OR BIPOLAR OPERATION**
- **SETTLING TIME:** 10 μ s to 0.003%
- **15-BIT LINEARITY AND MONOTONICITY:** -40°C to $+85^{\circ}\text{C}$
- **PROGRAMMABLE RESET TO MID-SCALE OR ZERO-SCALE**
- **DATA READBACK**
- **DOUBLE-BUFFERED DATA INPUTS**

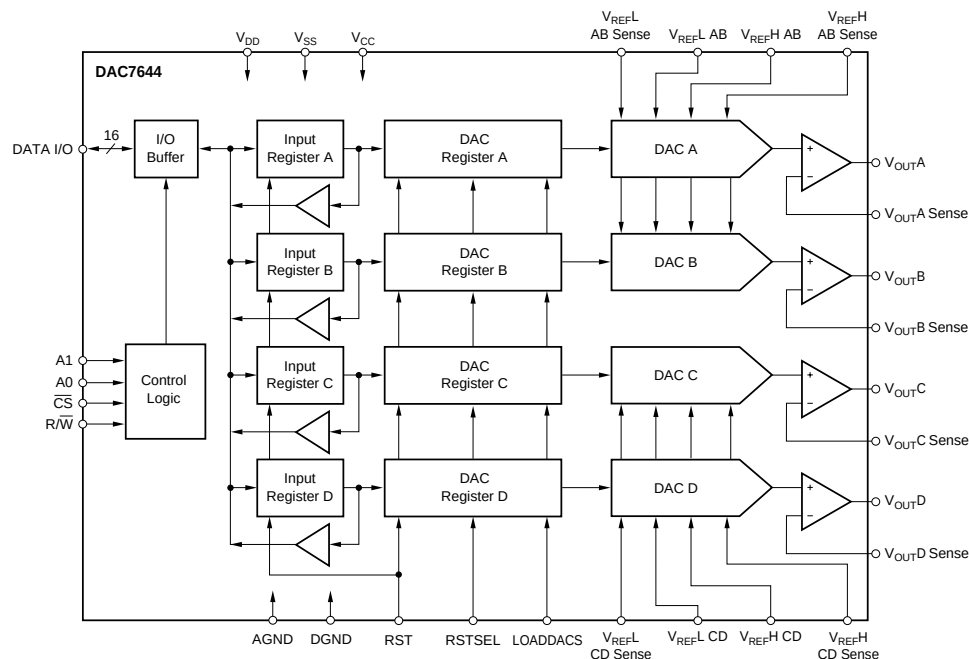
APPLICATIONS

- **PROCESS CONTROL**
- **CLOSED-LOOP SERVO-CONTROL**
- **MOTOR CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **DAC-PER-PIN PROGRAMMERS**

DESCRIPTION

The DAC7644 is a 16-bit, quad voltage output digital-to-analog converter with guaranteed 15-bit monotonic performance over the specified temperature range. It accepts 16-bit parallel input data, has double-buffered DAC input logic (allowing simultaneous update of all DACs), and provides a readback mode of the internal input registers. Programmable asynchronous reset clears all registers to a mid-scale code of 8000_H or to a zero-scale of 0000_H. The DAC7644 can operate from a single +5V supply or from +5V and -5V supplies.

Low power and small size per DAC make the DAC7644 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7644 is available in a 48-lead SSOP package and offers guaranteed specifications over the -40°C to $+85^{\circ}\text{C}$ temperature range.



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SPECIFICATIONS (Dual Supply)

At $T_A = T_{MIN}$ to T_{MAX} , $V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, $V_{REFH} = +2.5V$, and $V_{REFL} = -2.5V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7644E			DAC7644EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error			±3	±4		±2	±3	LSB
Linearity Match			±4			±2		LSB
Differential Linearity Error			±2	±3		±1	±2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			Bits
Bipolar Zero Error			±1	±2		*	*	mV
Bipolar Zero Error Drift			5	10		*	*	ppm/°C
Full-Scale Error			±1	±2		*	*	mV
Full-Scale Error Drift			5	10		*	*	ppm/°C
Bipolar Zero Matching	Channel-to-Channel Matching		±1	±2		±1	±2	mV
Full Scale Matching	Channel-to-Channel Matching		±1	±2		±1	±2	mV
Power Supply Rejection Ratio (PSRR)	At Full Scale		10	100		*	*	ppm/V
ANALOG OUTPUT								
Voltage Output	$V_{REF} = -2.5V$, $R_L = 10k\Omega$, $V_{SS} = -5V$	$V_{REFL} - 1.25$		$V_{REFH} + 1.25$	*		*	V
Output Current					*		*	mA
Maximum Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			-10, +30			*		mA
Short-Circuit Duration	GND or V_{CC} or V_{SS}		Indefinite			*		
REFERENCE INPUT								
Ref High Input Voltage Range		$V_{REFL} + 1.25$		+2.5	*		*	V
Ref Low Input Voltage Range		-2.5		$V_{REFH} - 1.25$	*		*	V
Ref High Input Current			500			*		μA
Ref Low Input Current			-500			*		μA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.003%, 5V Output Step		8	10		*	*	μs
Channel-to-Channel Crosstalk	See Figure 5.		0.5			*		LSB
Digital Feedthrough			2			*		nV-s
Output Noise Voltage	f = 10kHz		60			*		nV/√Hz
DAC Glitch	7FFF _H to 8000 _H or 8000 _H to 7FFF _H		40			*		nV-s
DIGITAL INPUT								
V_{IH}		$0.7 \cdot V_{DD}$			*			V
V_{IL}				$0.3 \cdot V_{DD}$			*	V
I_{IH}				±10			*	μA
I_{IL}				±10			*	μA
DIGITAL OUTPUT								
V_{OH}	$I_{OH} = -0.8mA$	3.6	4.5		*	*		V
V_{OL}	$I_{OL} = 1.2mA$		0.3	0.4		*	*	V
POWER SUPPLY								
V_{DD}		+4.75	+5.0	+5.25	*	*	*	V
V_{CC}		+4.75	+5.0	+5.25	*	*	*	V
V_{SS}		-5.25	-5.0	-4.75	*	*	*	V
I_{CC}			1.5	2		*	*	mA
I_{DD}			50			*	*	μA
I_{SS}		-2.3	-1.5		*	*	*	mA
Power			15	20		*	*	mW
TEMPERATURE RANGE								
Specified Performance		-40		+85	*		*	°C

* Specifications same as DAC7644E.

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SPECIFICATIONS (Single Supply)

At $T_A = T_{MIN}$ to T_{MAX} , $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +2.5V$, and $V_{REFL} = 0V$, unless otherwise noted.

		DAC7644E			DAC7644EB			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ACCURACY Linearity Error ⁽¹⁾ Linearity Match Differential Linearity Error Monotonicity, T _{MIN} to T _{MAX} Zero Scale Error Zero Scale Error Drift Full-Scale Error Full-Scale Error Drift Zero Scale Matching Full-Scale Matching Power Supply Rejection Ratio (PSRR)	 Channel-to-Channel Matching Channel-to-Channel Matching At Full Scale	 14 						

NOTE: (1) If $V_{SS} = 0V$ specification applies at Code 0040_H and above due to possible negative zero-scale error.

* Specifications same as DAC7644E.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

V_{CC} and V_{DD} to V_{SS}	–0.3V to 11V
V_{CC} and V_{DD} to GND	–0.3V to 5.5V
V_{REFL} to V_{SS}	–0.3V to ($V_{CC} - V_{SS}$)
V_{CC} to V_{REFH}	–0.3V to ($V_{CC} - V_{SS}$)
V_{REFH} to V_{REFL}	–0.3V to ($V_{CC} - V_{SS}$)
Digital Input Voltage to GND	–0.3V to $V_{DD} + 0.3V$
Digital Output Voltage to GND	–0.3V to $V_{DD} + 0.3V$
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

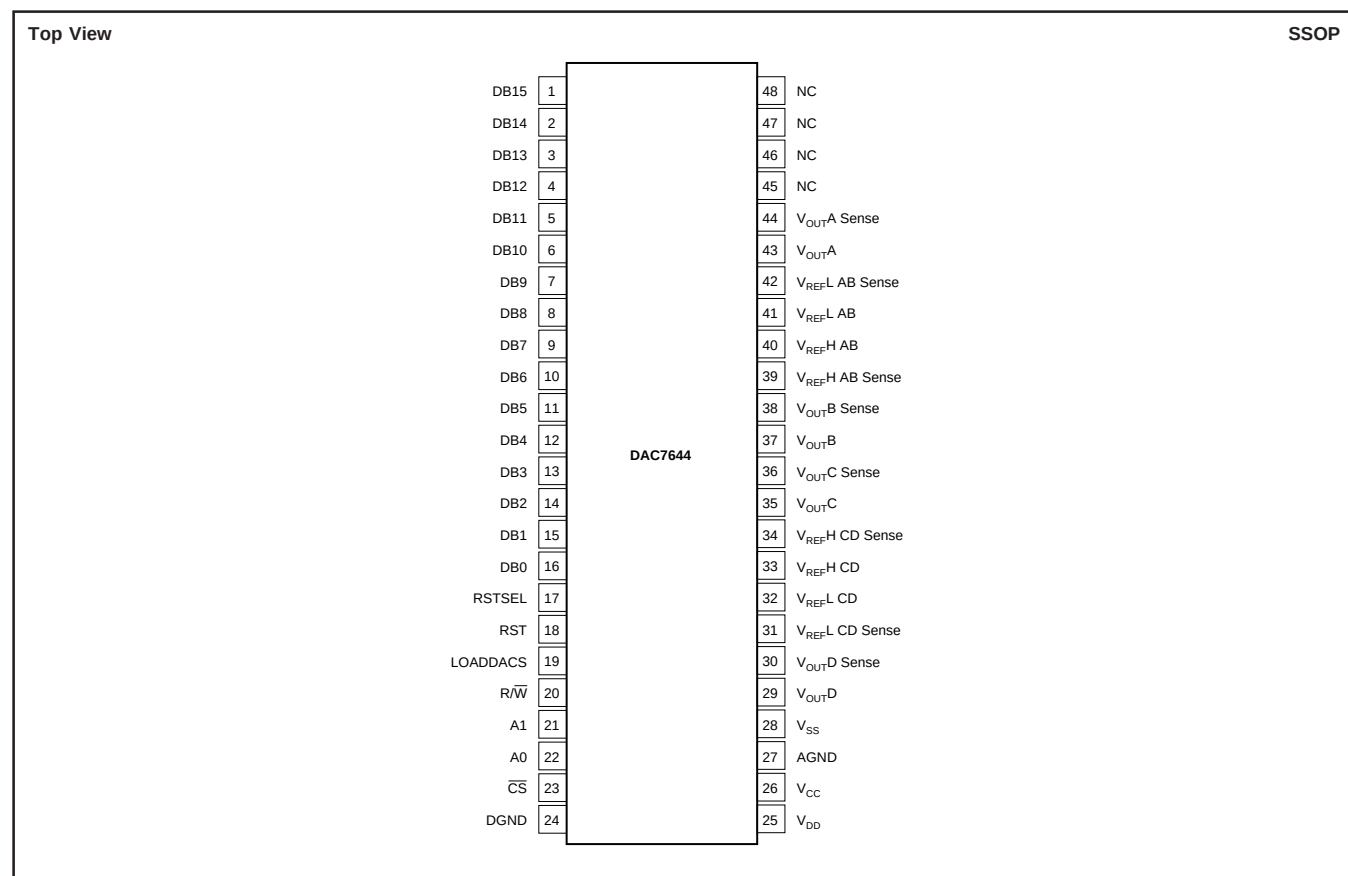
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	LINEARITY ERROR (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER ⁽²⁾	TRANSPORT MEDIA
DAC7644E	±4	±3	48-Lead SSOP	333	–40°C to +85°C	DAC7644E	Rails
"	"	"	"	"	"	DAC7644E/1K	Tape and Reel
DAC7644EB	±3	±2	48-Lead SSOP	333	–40°C to +85°C	DAC7644EB	Rails
"	"	"	"	"	"	DAC7644EB/1K	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of “DAC7644/1K” will get a single 1000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

PIN CONFIGURATION



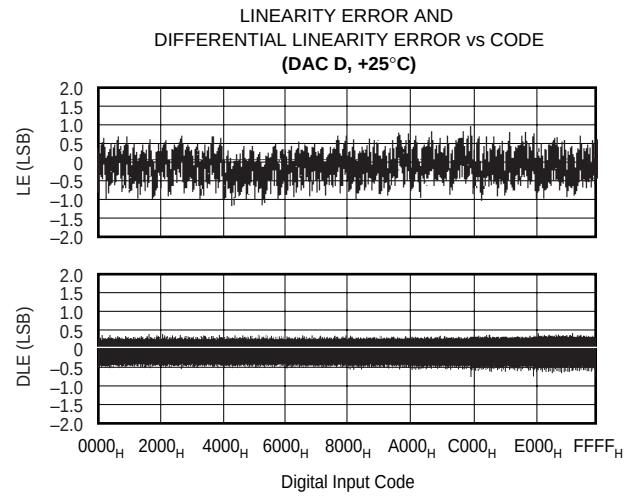
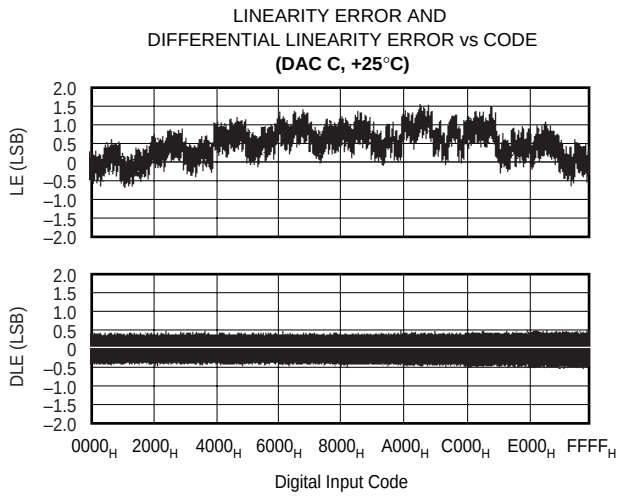
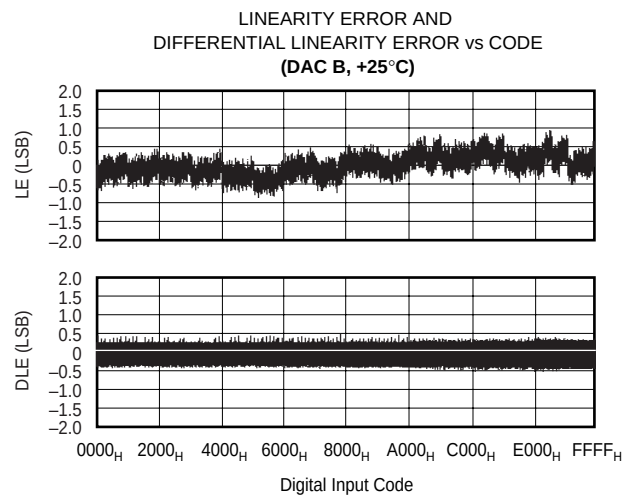
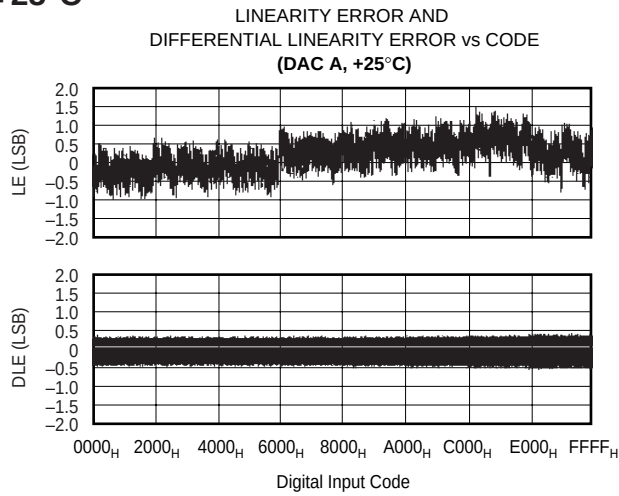
PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	DB15	Data Bit 15, MSB	23	CS	Chip Select. Active LOW.
2	DB14	Data Bit 14	24	DGND	Digital Ground
3	DB13	Data Bit 13	25	VDD	Positive Power Supply (digital)
4	DB12	Data Bit 12	26	VCC	Positive Power Supply (analog)
5	DB11	Data Bit 11	27	AGND	Analog Ground
6	DB10	Data Bit 10	28	VSS	Negative Power Supply
7	DB9	Data Bit 9	29	VOUTD	DAC D Voltage Output
8	DB8	Data Bit 8	30	VOUTD Sense	DAC D's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
9	DB7	Data Bit 7	31	VREFL CD Sense	DAC C and D Reference Low Sense Input
10	DB6	Data Bit 6	32	VREFL CD	DAC C and D Reference Low Input
11	DB5	Data Bit 5	33	VREFH CD	DAC C and D Reference High Input
12	DB4	Data Bit 4	34	VREFH CD Sense	DAC C and D Reference High Sense Input
13	DB3	Data Bit 3	35	VOUTC	DAC C Voltage Output
14	DB2	Data Bit 2	36	VOUTC Sense	DAC C's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
15	DB1	Data Bit 1	37	VOUTB	DAC B Voltage Output
16	DB0	Data Bit 0, LSB	38	VOUTB Sense	DAC B's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
17	RSTSEL	Reset Select. Determines the action of RST. If HIGH, a RST command will set the DAC registers to mid-scale. If LOW, a RST command will set the DAC registers to zero.	39	VREFH AB Sense	DAC A and B Reference High Sense Input
18	RST	Reset, Rising Edge Triggered. Depending on the state of RSTSEL, the DAC registers are set to either mid-scale or zero.	40	VREFH AB	DAC A and B Reference High Input
19	LOADDACS	DAC Output Registers Load Control. Rising edge triggered.	41	VREFL AB	DAC A and B Reference Low Input
20	R/W	Enabled by the CS, Controls Data Read and Write from the Input Registers.	42	VREFL AB Sense	DAC A and B Reference Low Sense Input
21	A1	Enabled by the CS, in Combination With A0 Selects the Individual DAC Input Registers.	43	VOUTA	DAC A Voltage Input
22	A0	Enabled by the CS, in Combination With A1 Selects the Individual DAC Input Registers.	44	VOUTA Sense	DAC A's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
			45	NC	No Connection
			46	NC	No Connection
			47	NC	No Connection
			48	NC	No Connection

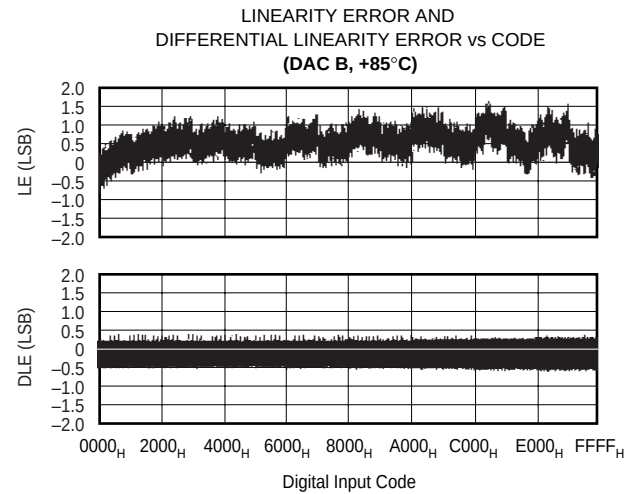
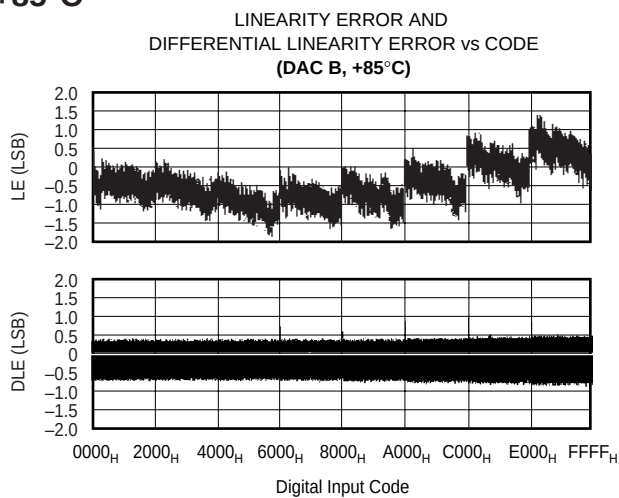
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$

At $T_A = +25^\circ C$, $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +2.5V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.

+25°C



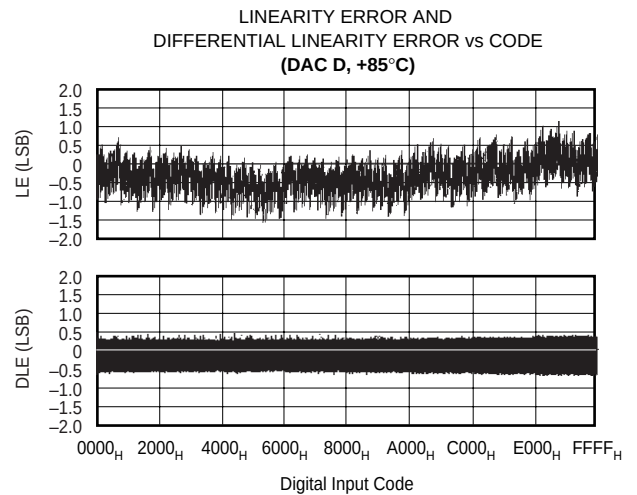
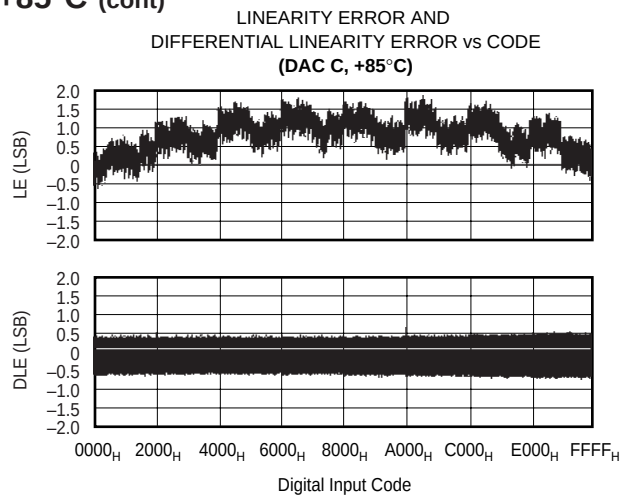
+85°C



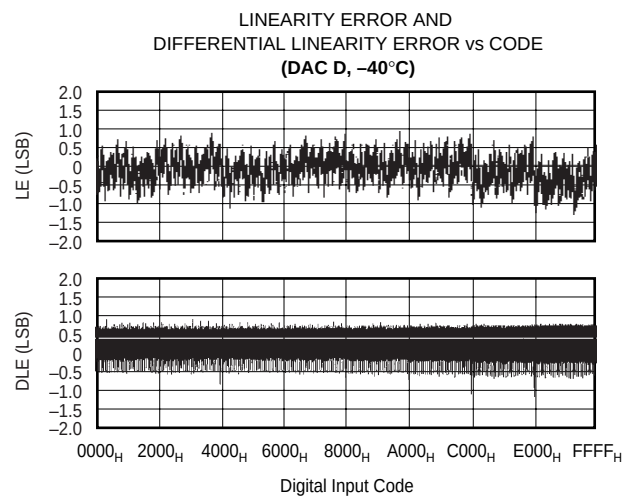
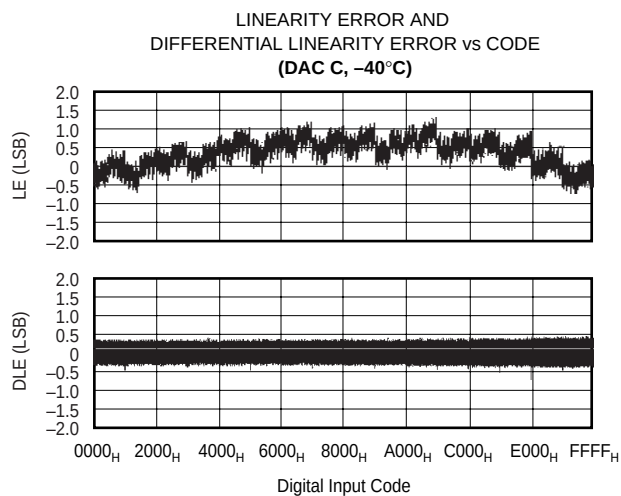
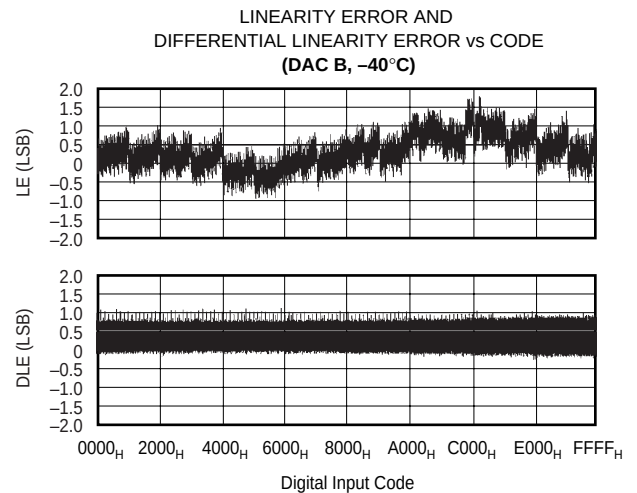
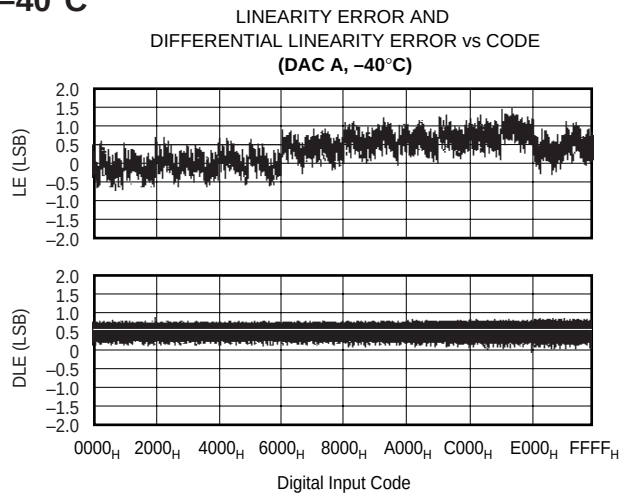
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (CONT)

At $T_A = +25^\circ C$, $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +2.5V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.

+85°C (cont)

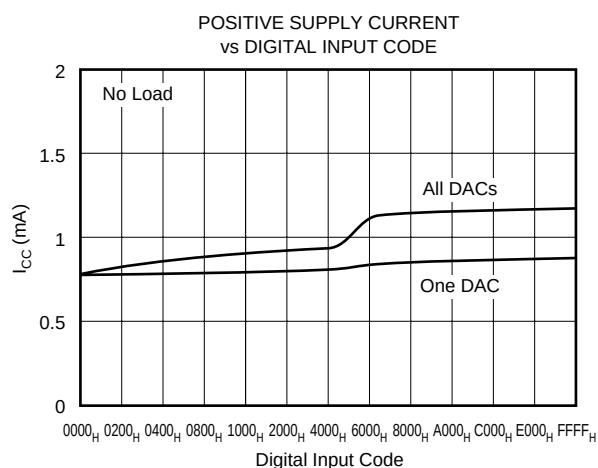
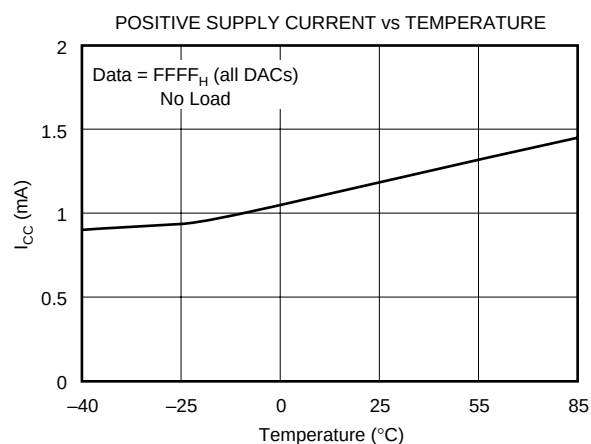
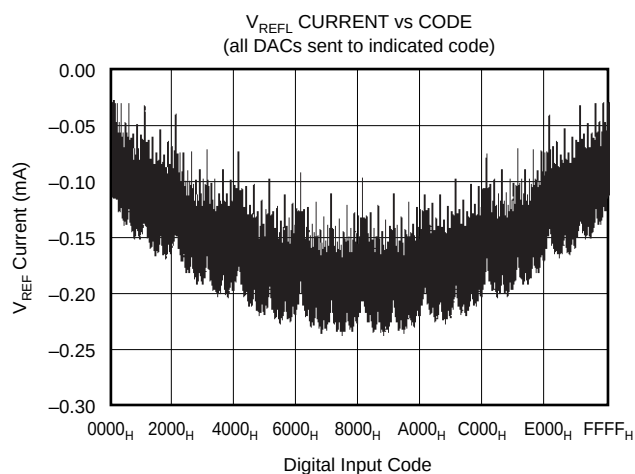
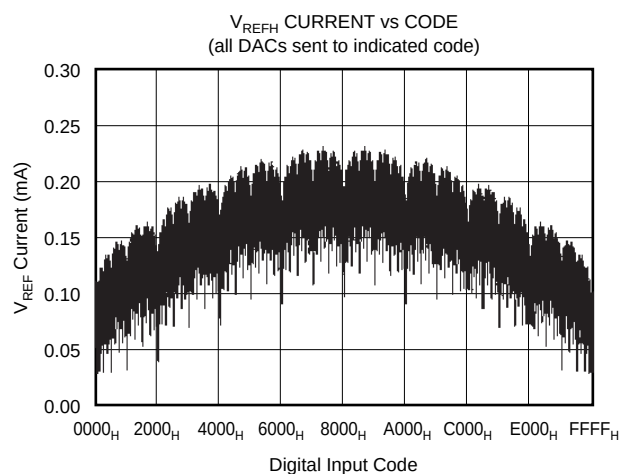
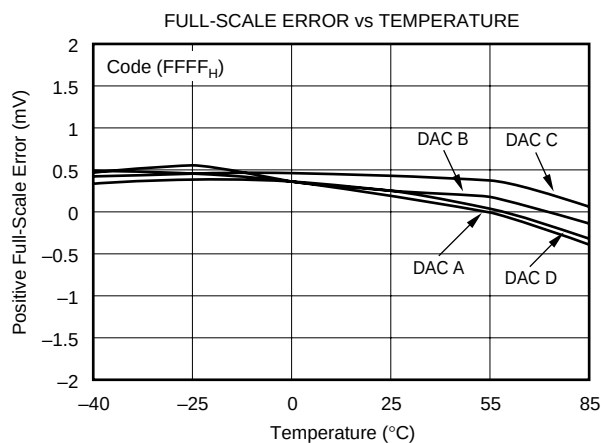
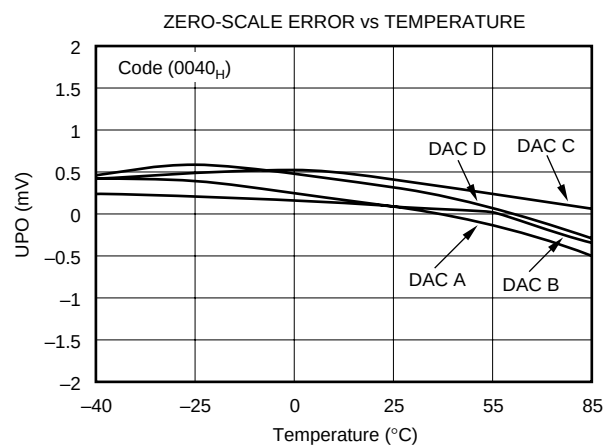


-40°C



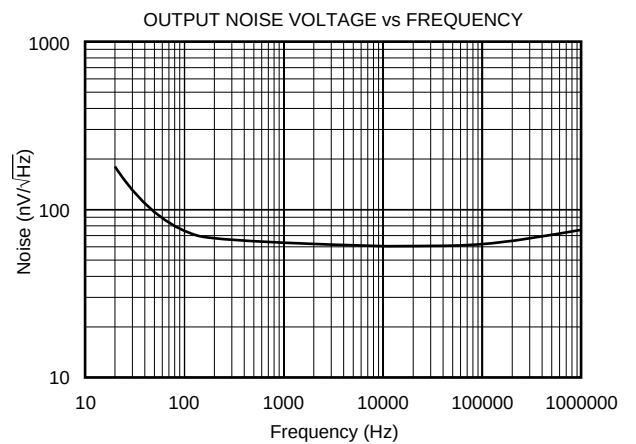
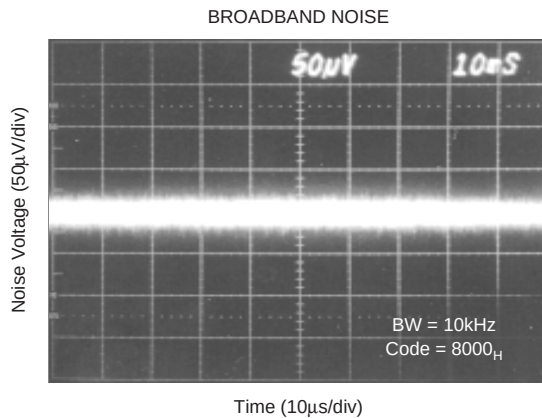
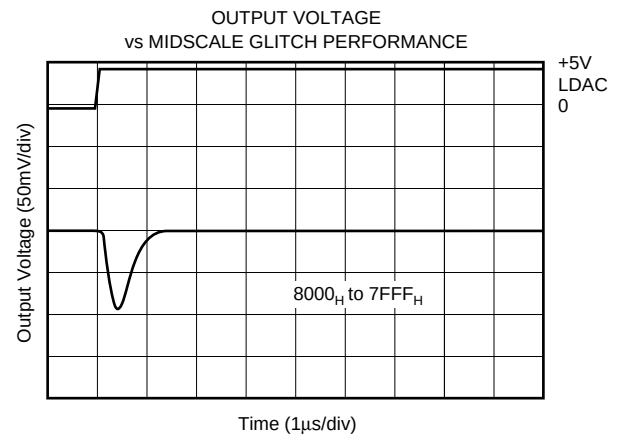
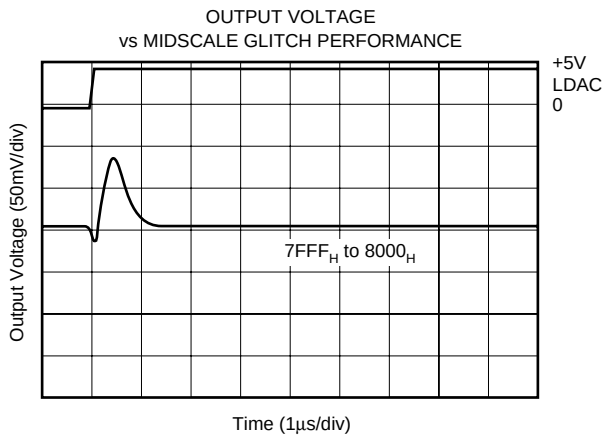
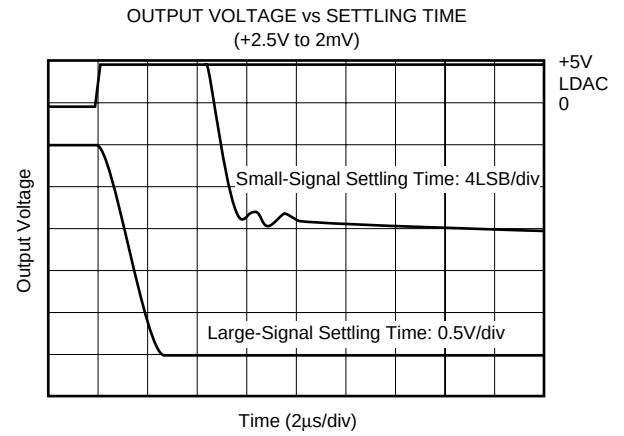
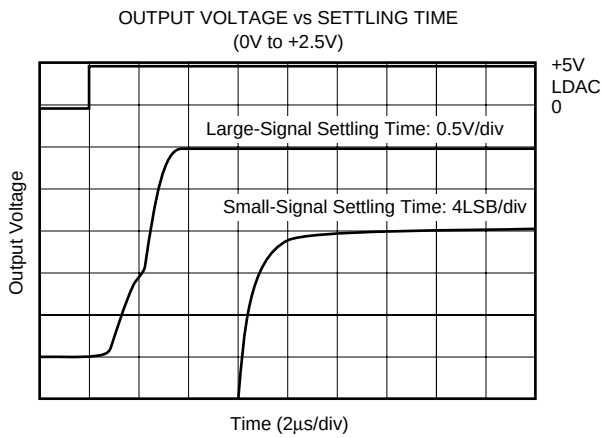
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (CONT)

At $T_A = +25^\circ C$, $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +2.5V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.



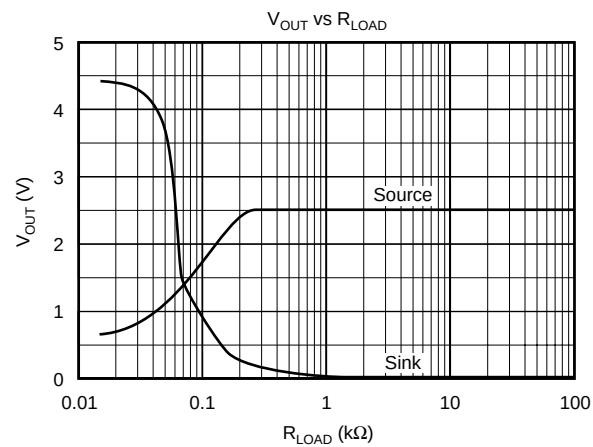
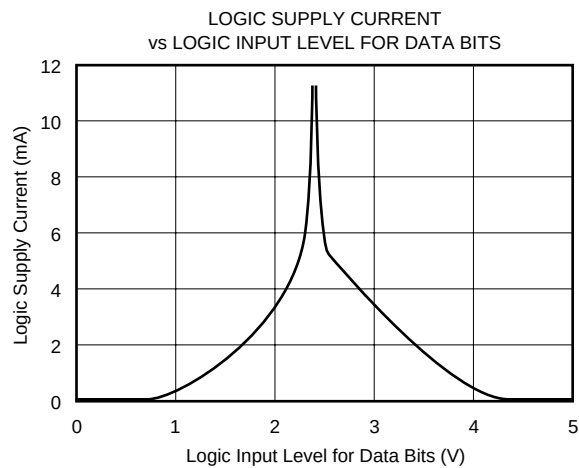
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (CONT)

At $T_A = +25^\circ C$, $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +2.5V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.



TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (CONT)

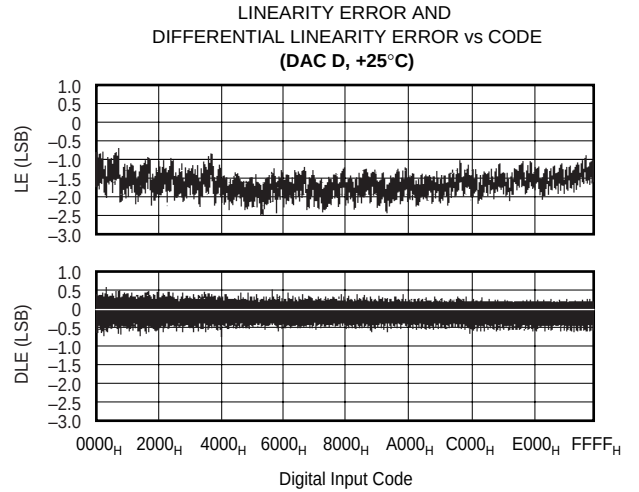
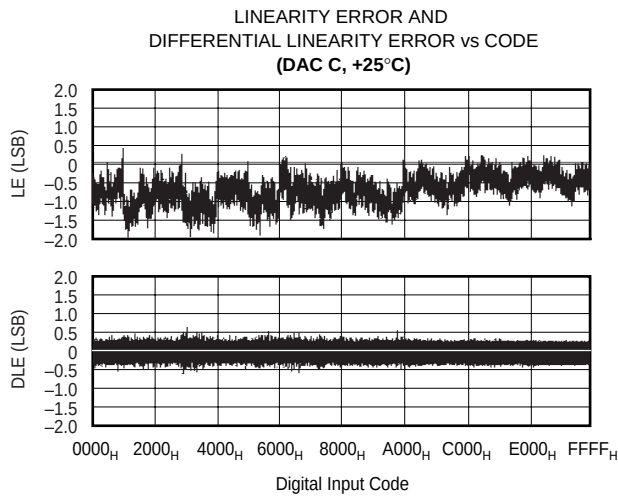
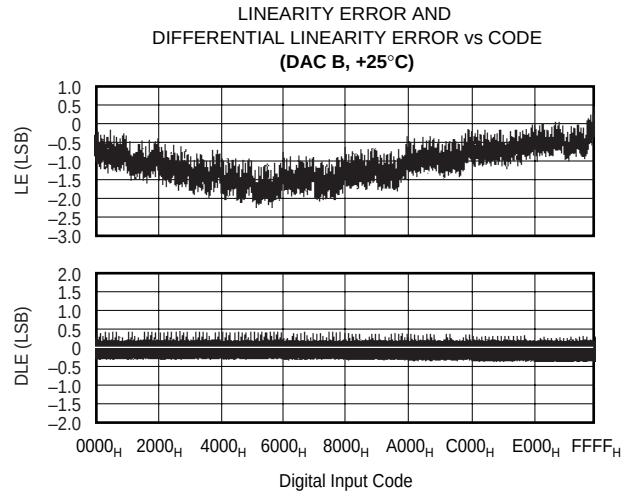
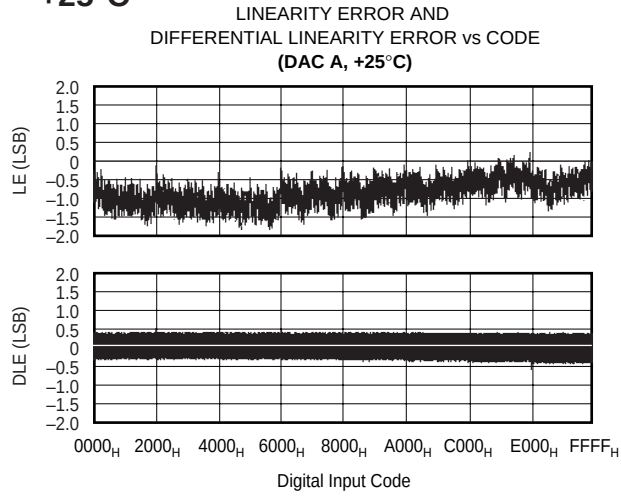
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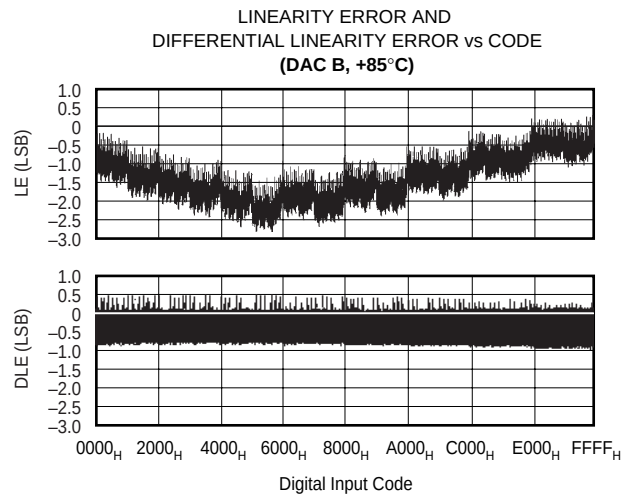
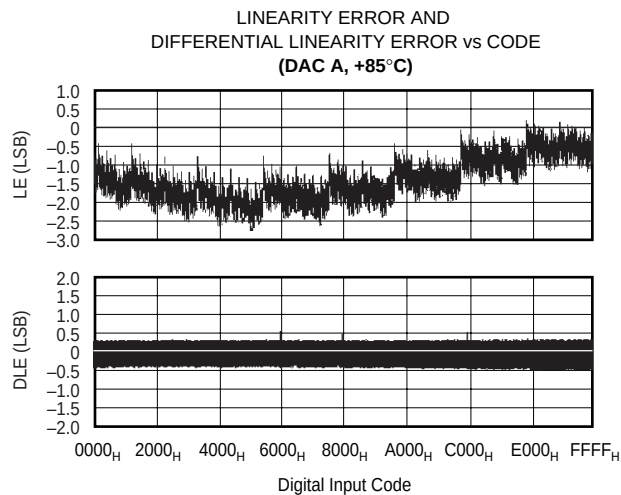
TYPICAL PERFORMANCE CURVES: $V_{SS} = -5V$

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+25°C



+85°C

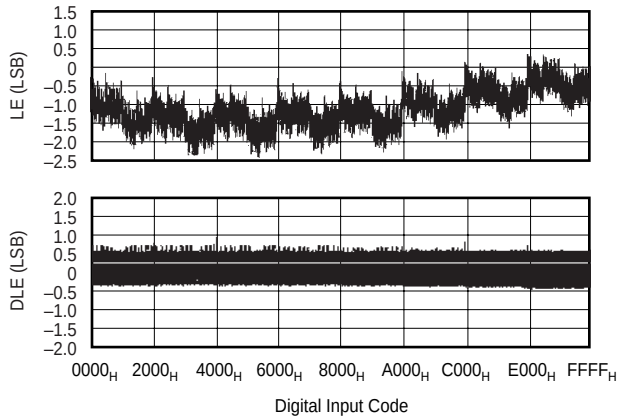


TYPICAL PERFORMANCE CURVES: $V_{SS} = -5V$ (CONT)

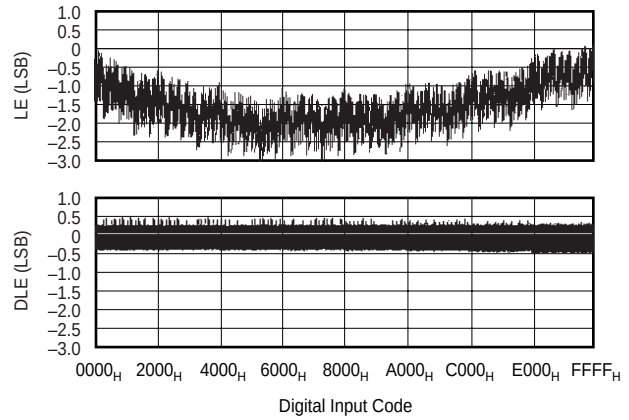
At $T_A = +25^\circ C$, $V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, $V_{REFH} = +2.5V$, $V_{REFL} = -2.5V$, representative unit, unless otherwise specified.

+85°C (cont)

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +85°C)

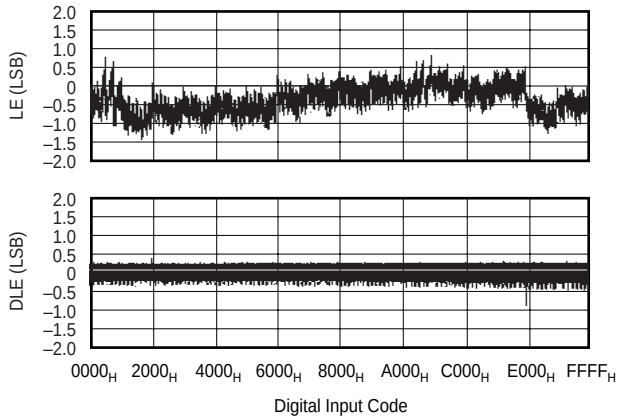


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +85°C)

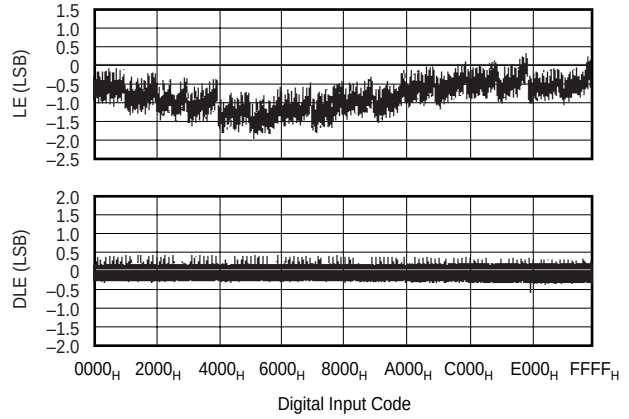


-40°C

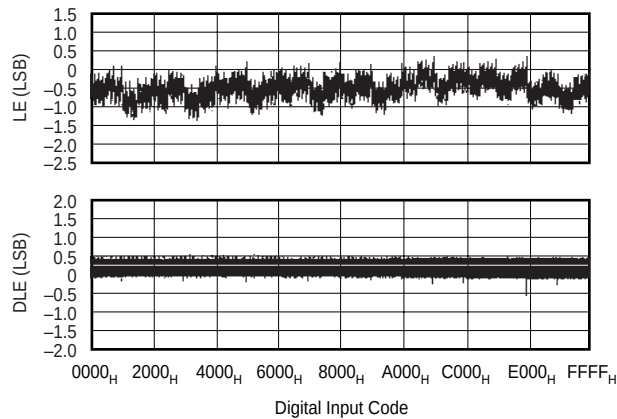
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DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, -40°C)



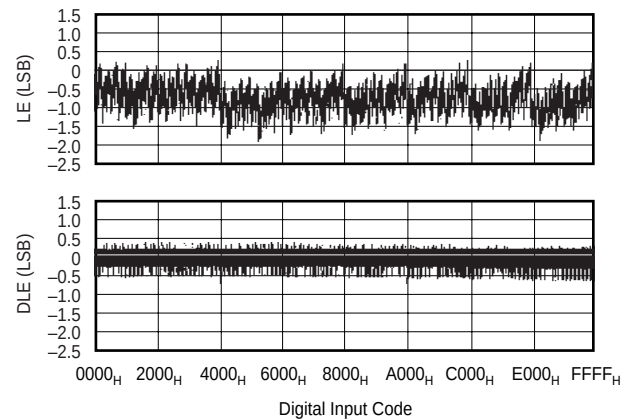
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DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, -40°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, -40°C)

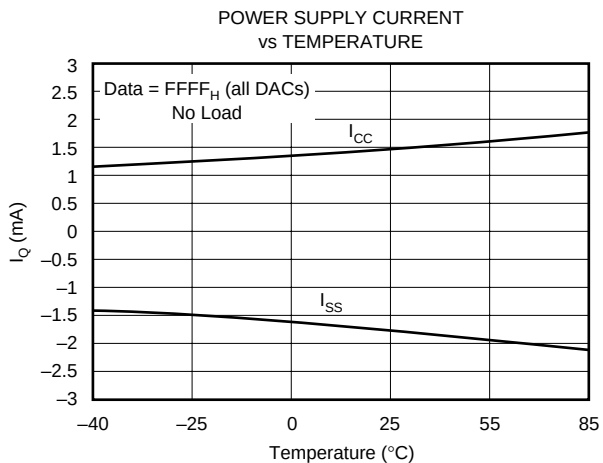
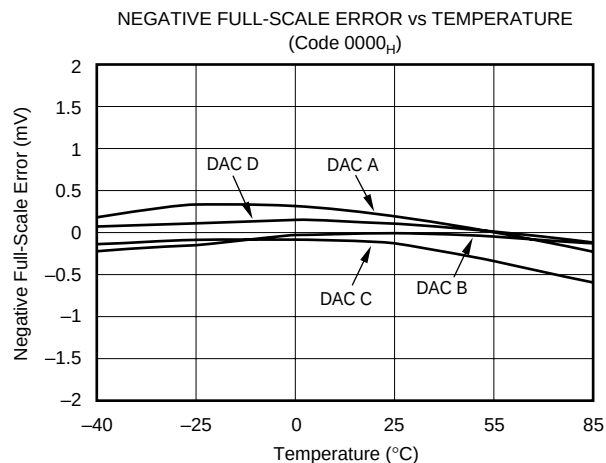
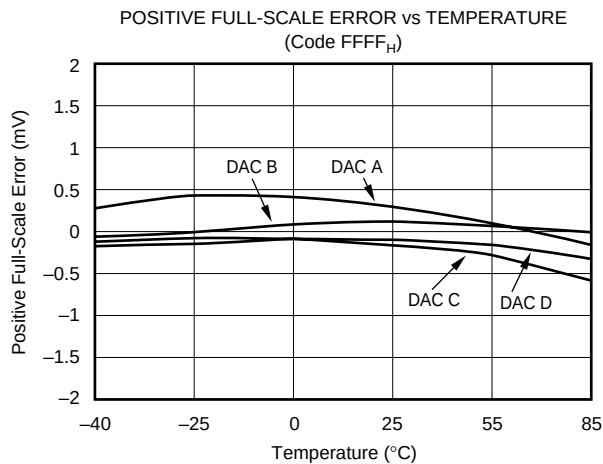
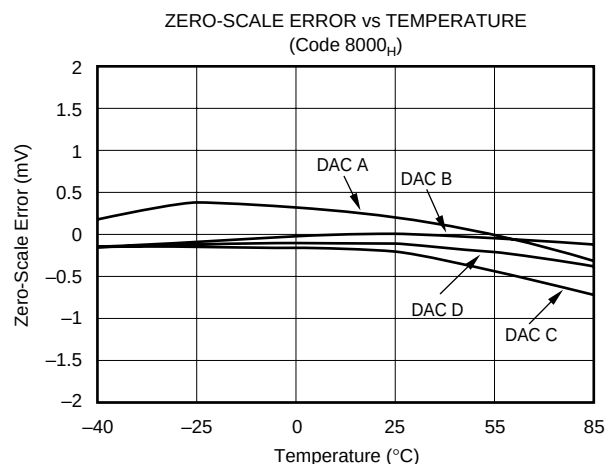
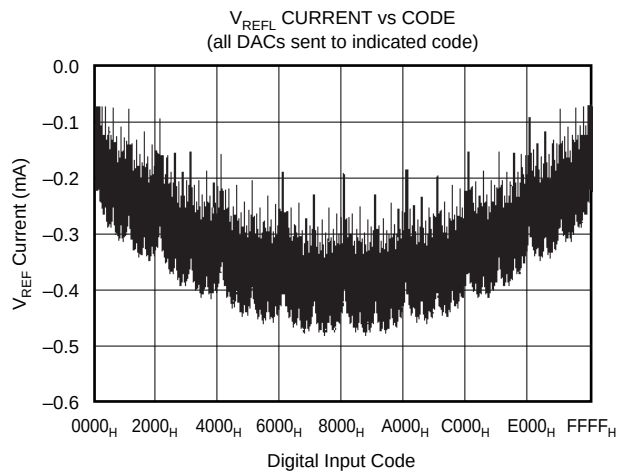
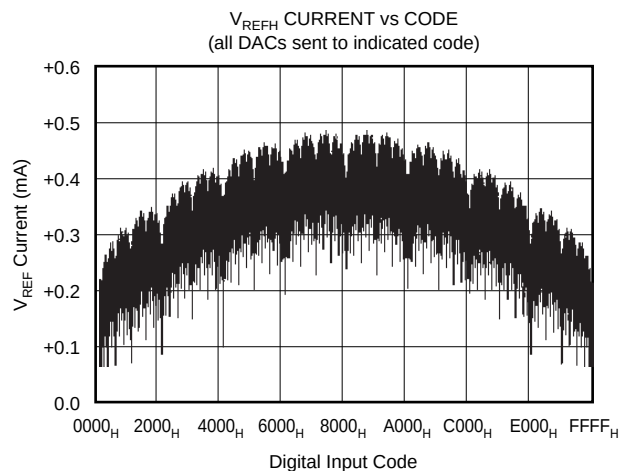


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, -40°C)



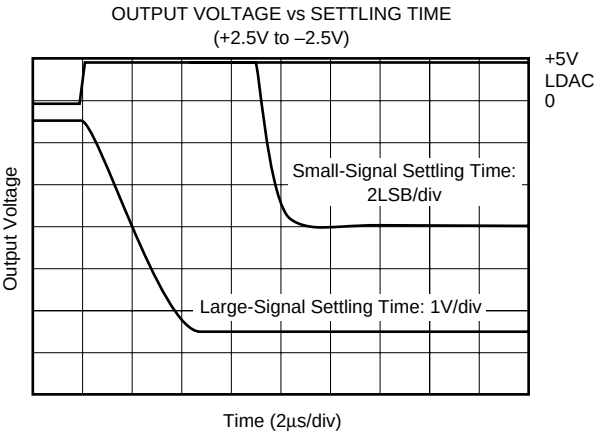
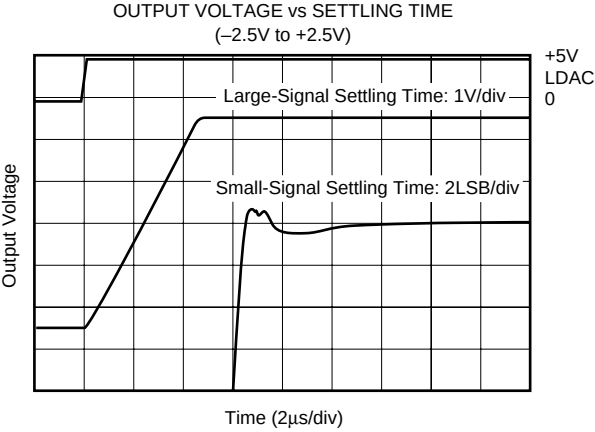
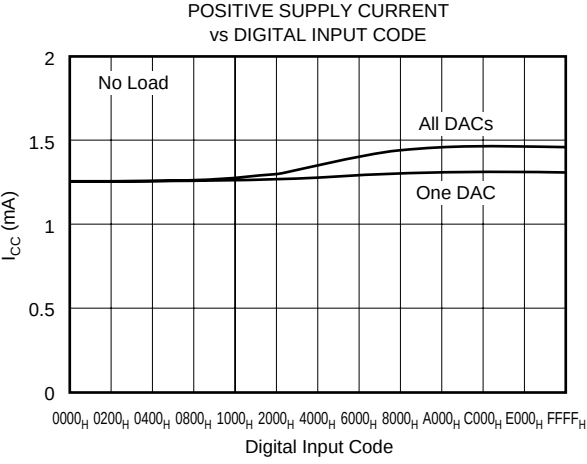
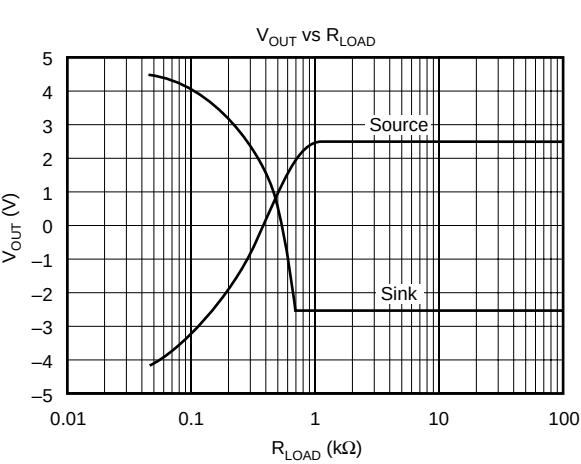
TYPICAL PERFORMANCE CURVES: $V_{SS} = -5V$ (CONT)

At $T_A = +25^\circ C$, $V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, $V_{REFH} = +2.5V$, $V_{REFL} = -2.5V$, representative unit, unless otherwise specified.



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THEORY OF OPERATION

The DAC7644 is a quad voltage output, 16-bit digital-to-analog converter (DAC). The architecture is an R-2R ladder configuration with the three MSB's segmented followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network, segmented MSBs and output op amp (see Figure 1). The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set

by the external voltage references (V_{REFL} and V_{REFH} , respectively). The digital input is a 16-bit parallel word and the DAC input registers offer a readback capability. The converters can be powered from either a single +5V supply or a dual $\pm 5V$ supply. The device offers a reset function which immediately sets all DAC output voltages and DAC registers to mid-scale code 8000_H or to zero-scale, code 0000_H. See Figures 2 and 3 for the basic operation of the DAC7644.

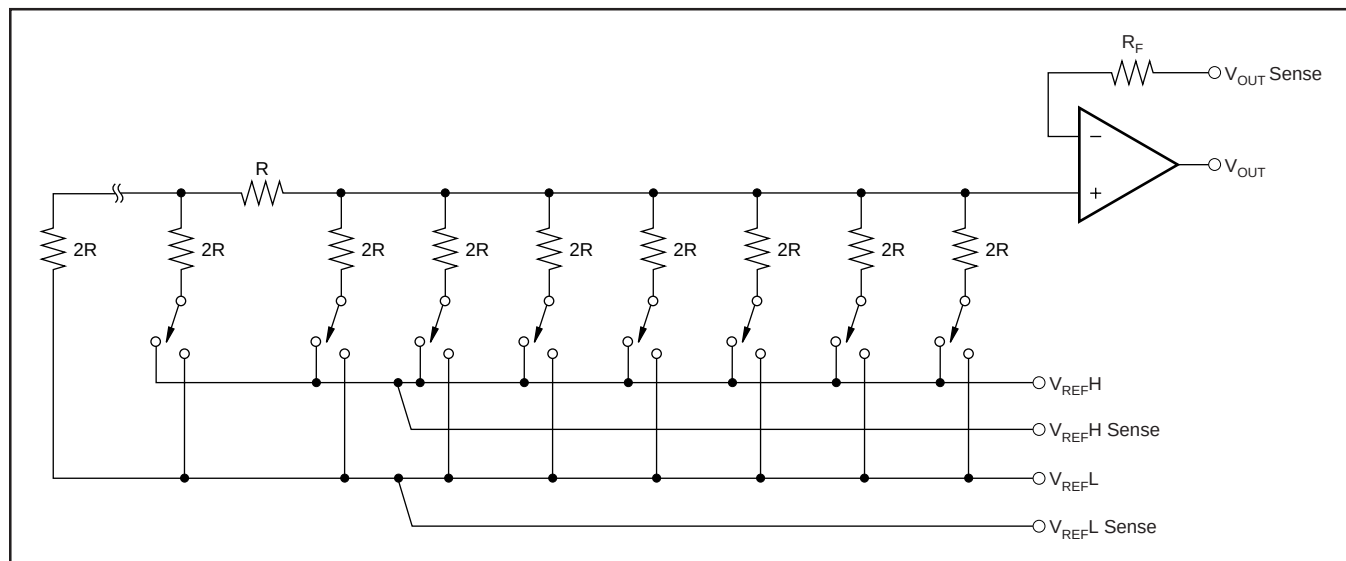


FIGURE 1. DAC7644 Architecture.

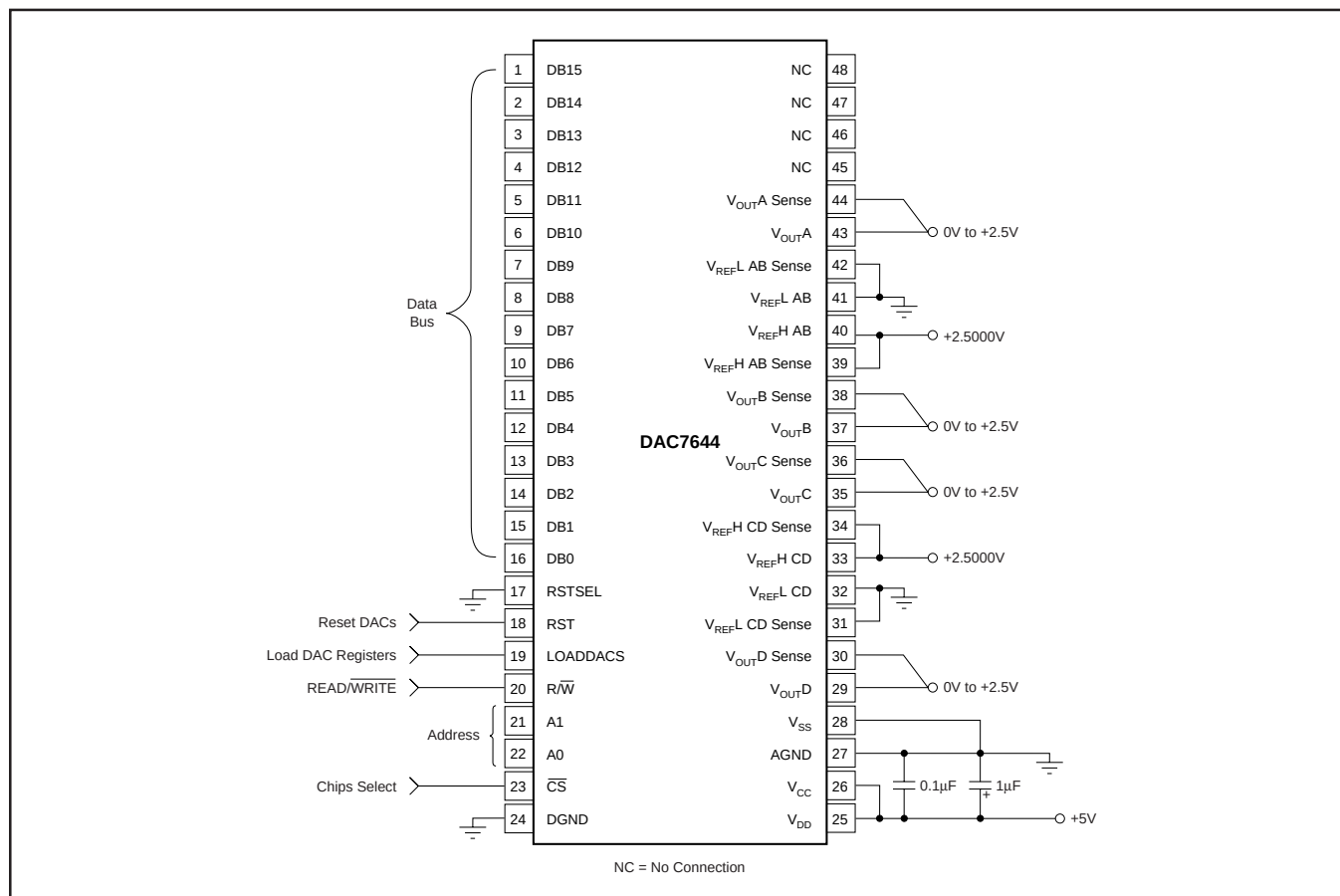
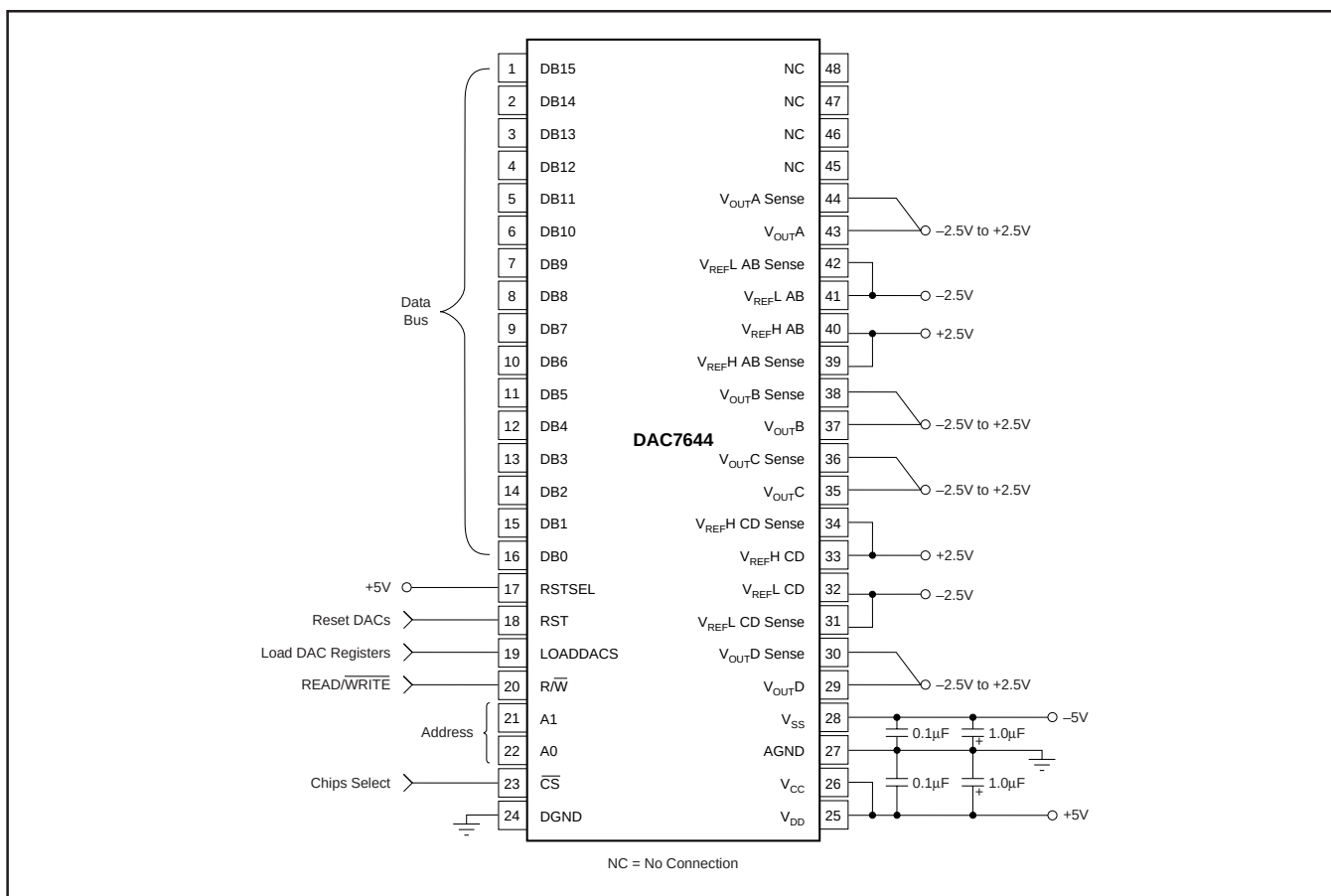


FIGURE 2. Basic Single-Supply Operation of the DAC7644.

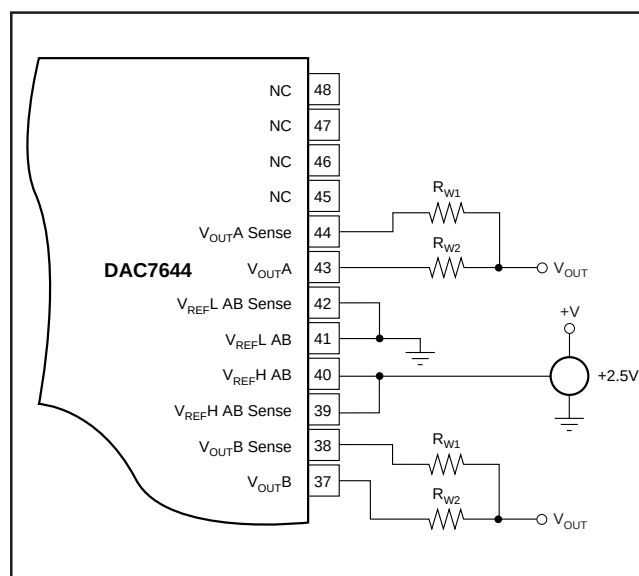


ANALOG OUTPUTS

When $V_{SS} = -5V$ (dual supply operation), the output amplifier can swing to within 2.25V of the supply rails, guaranteed over the $-40^{\circ}C$ to $+85^{\circ}C$ temperature range. With $V_{SS} = 0V$ (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to ground. Care must also be taken when measuring the zero-scale error when $V_{SS} = 0V$. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000_H, 0001_H, 0002_H, etc.) if the output amplifier has a negative offset. At the negative limit of $-2mV$, the first specified output starts at code 0040_H.

Due to the high accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 2.5V full-scale range has a 1LSB value of 38 μ V. With a load current of 1mA, series wiring and connector resistance (see Figure 4) of only 40m Ω (R_{w2}) will cause a voltage drop of 40 μ V. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 m Ω per square. For a 1mA load, a 10 milli-inch wide printed circuit conductor 600 milli-inches long will result in a voltage drop of 30 μ V.

The DAC7644 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (see Figure 4), thus ensuring an accurate output voltage.



REFERENCE INPUTS

The reference inputs, V_{REFL} and V_{REFH} , can be any voltage between $V_{SS} + 2.5V$ and $V_{CC} - 2.5V$ provided that V_{REFH} is at least 1.25V greater than V_{REFL} . The minimum output of each DAC is equal to V_{REFL} plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to V_{REFH} plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of $-4.75V$ to $-5.25V$. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the V_{REFH} input and out of V_{REFL} depends on the DAC output voltages and can vary from a few microamps to approximately 0.5mA. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. The DAC7644 features a reference drive and sense connection such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figures 5 through 12 show different reference configurations and the effect on the linearity and differential linearity.

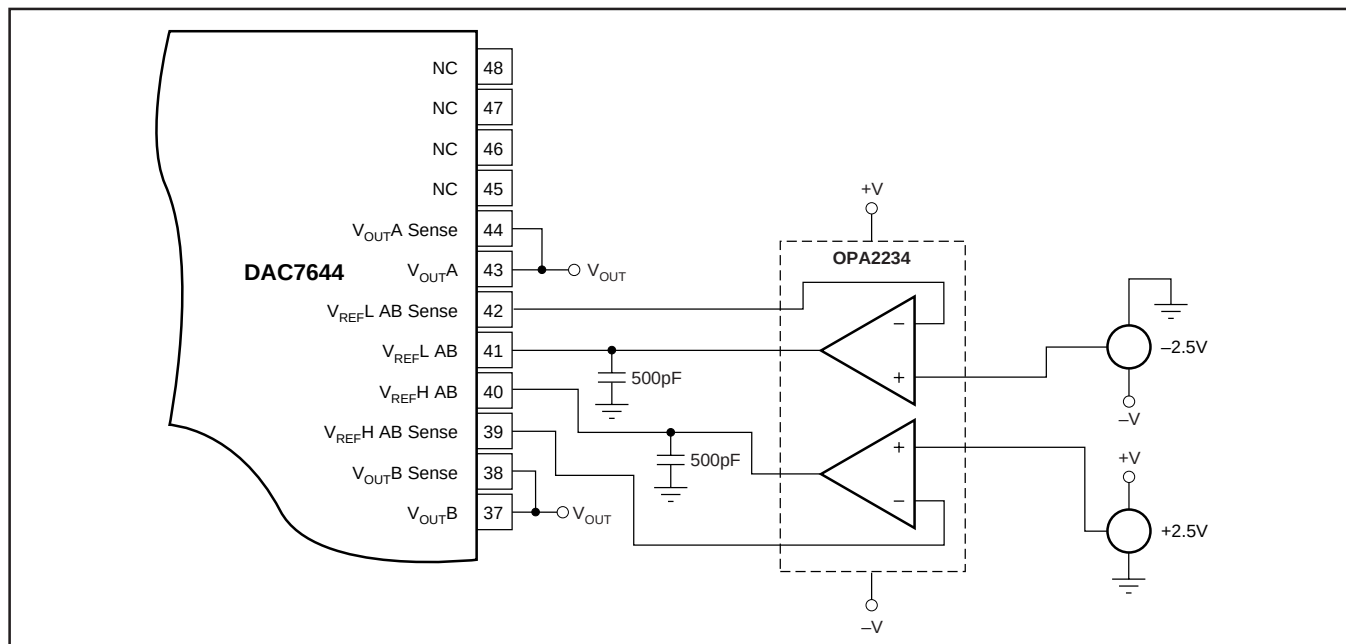


FIGURE 5. Dual Supply Configuration-Buffered References, used for Dual Supply Performance Curves (1/2 DAC7644).

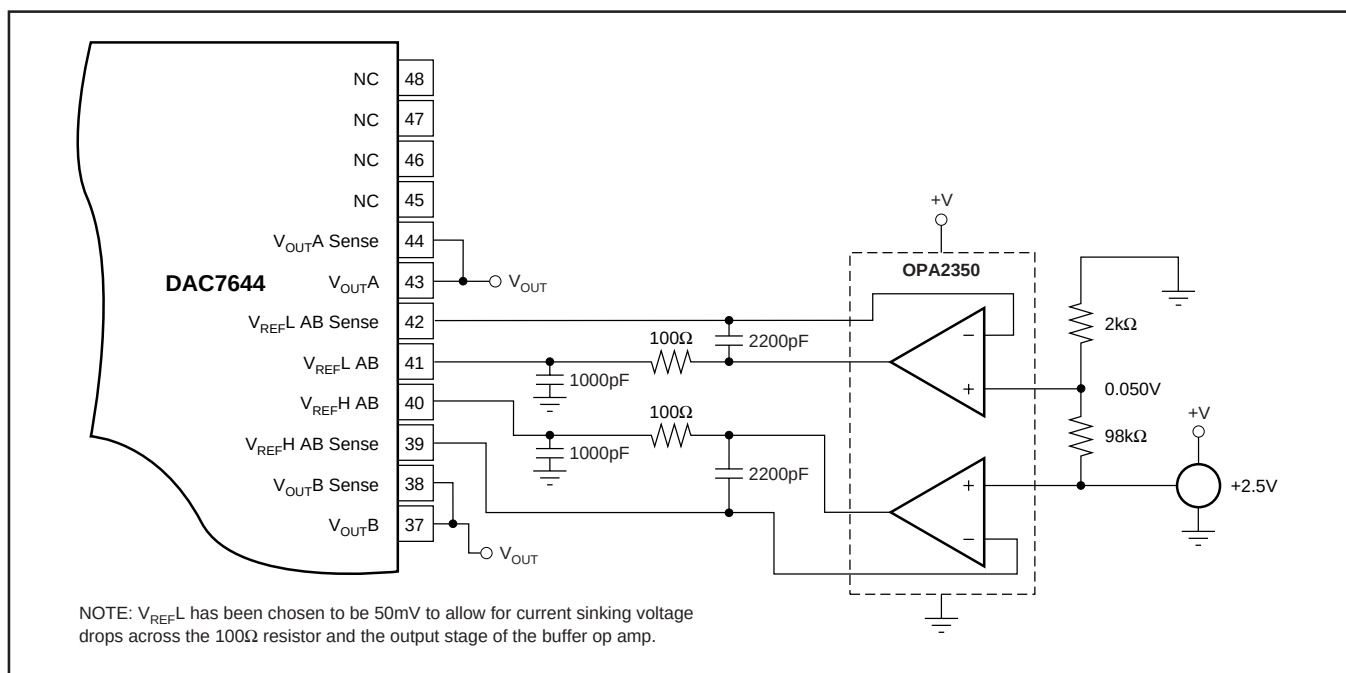


FIGURE 6. Single-Supply Buffered Reference with a Reference Low of 50mV (1/2 DAC7644).

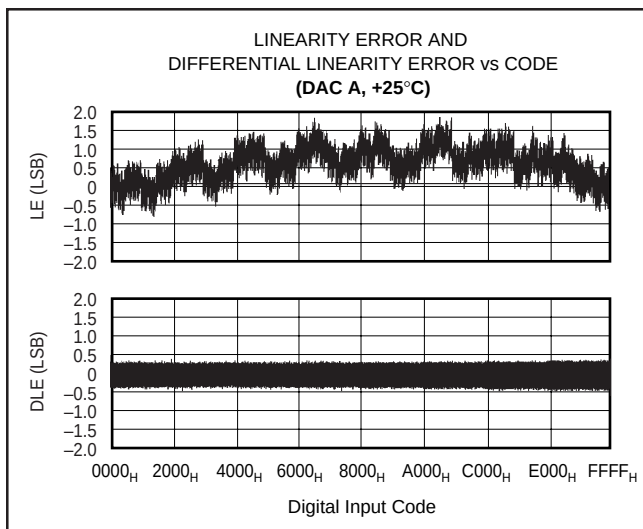


FIGURE 7. Integral Linearity and Differential Linearity Error Curves for Figure 6.

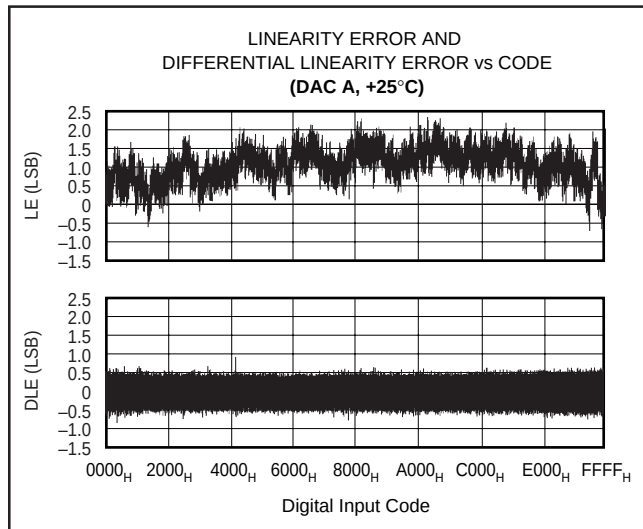


FIGURE 8. Integral Linearity and Differential Linearity Error Curves for Figure 9.

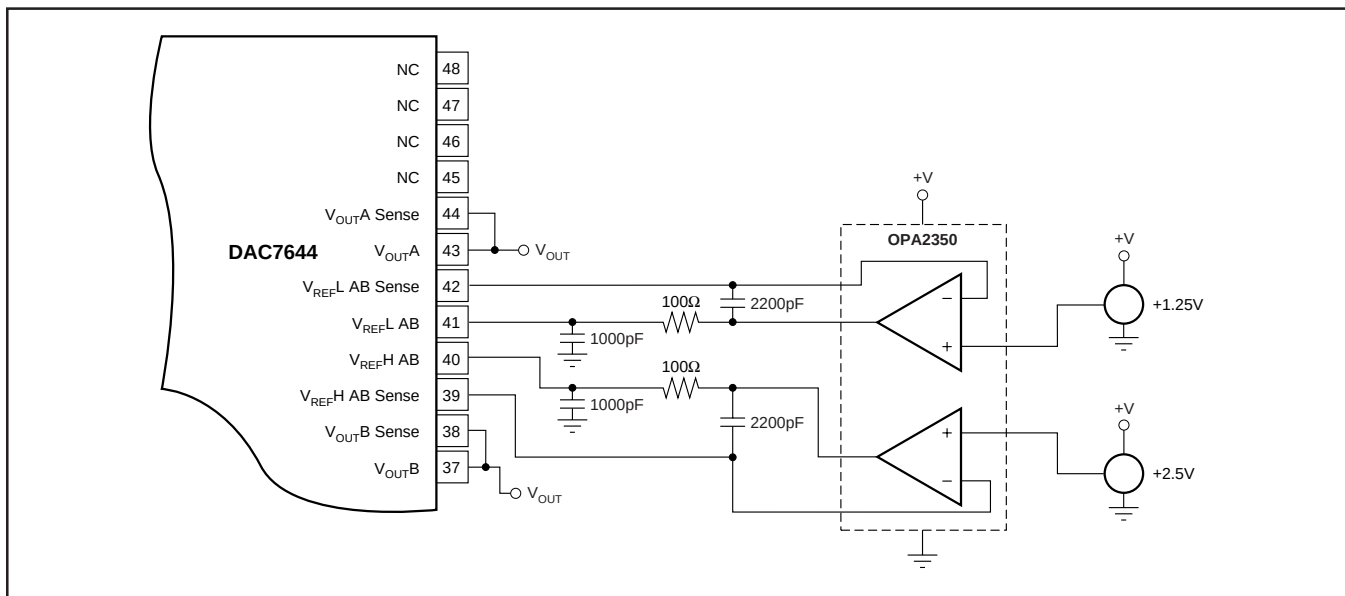


FIGURE 9. Single-Supply Buffered Reference with $V_{REFL} = +1.25V$ and $V_{REFH} = +2.5V$ (1/2 DAC7644).

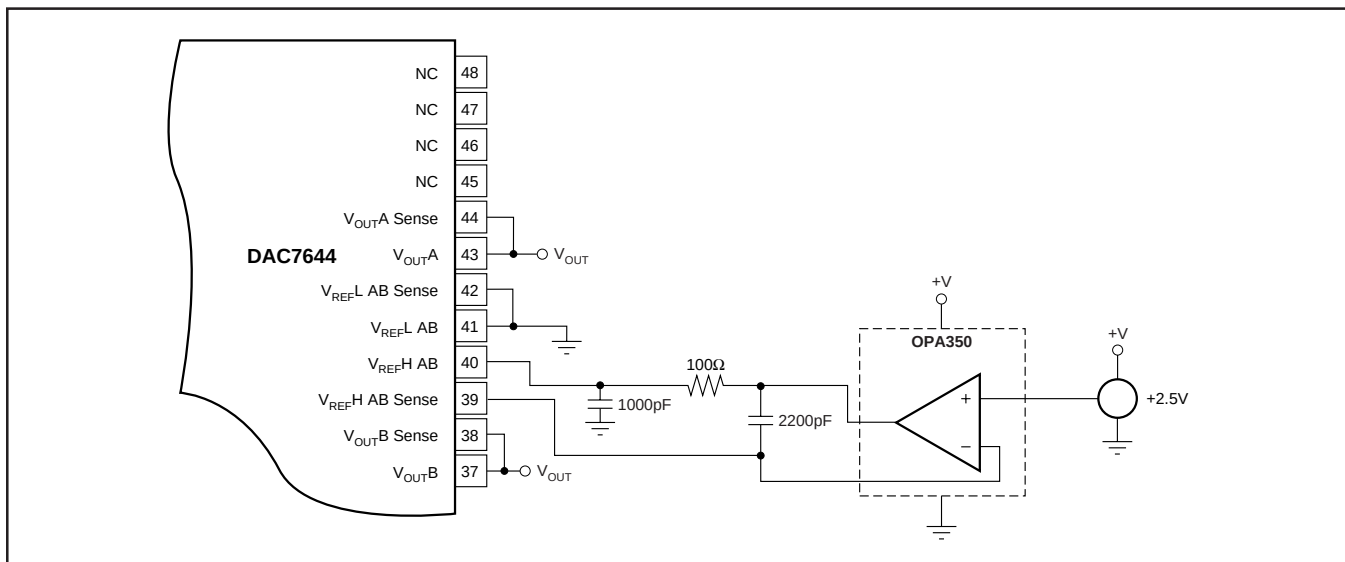


FIGURE 10. Single-Supply Buffered V_{REFH} (1/2 DAC7644).

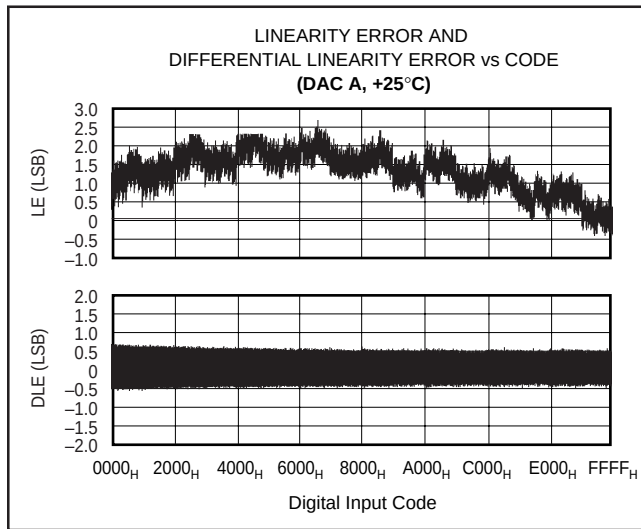


FIGURE 11. Linearity and Differential Linearity Error Curves for Figure 10.

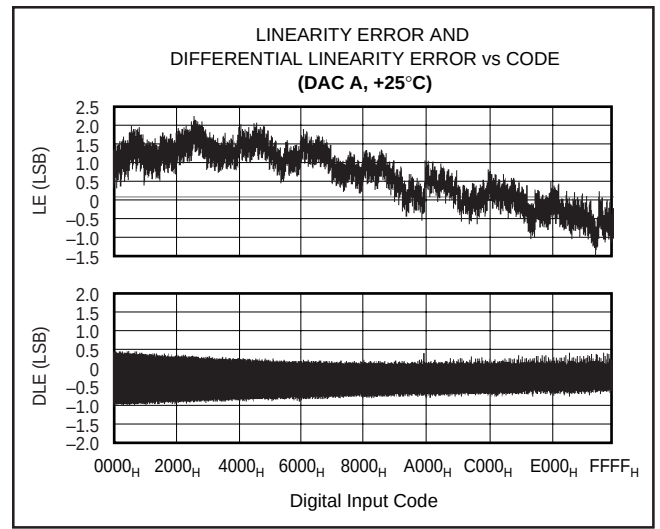


FIGURE 13. Linearity and Differential Linearity Error Curves for Figure 12.

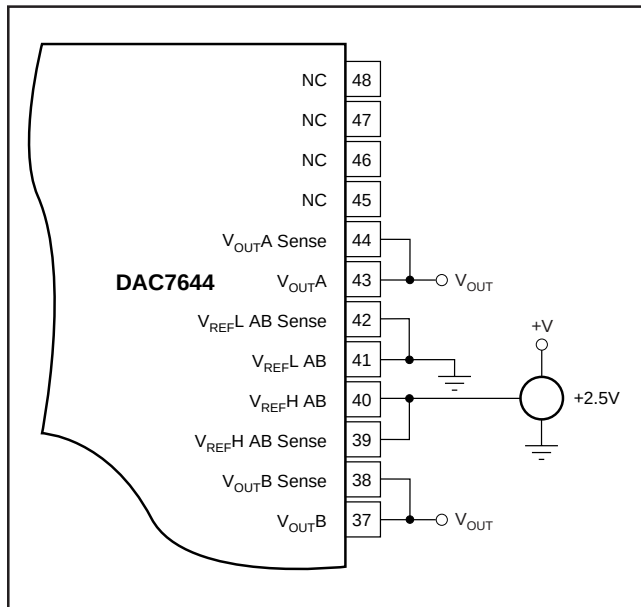


FIGURE 12. Low Cost Single-Supply Configuration.

DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7644. Note that each internal register is edge triggered and not level triggered. When the LOADDACS signal is transitioned to HIGH, the digital word currently in the register is latched. The first set of registers (the input registers) are triggered via the A0, A1, R/W, and CS inputs. Only one of these registers is transparent at any given time.

The double-buffered architecture is designed mainly so each DAC input register can be written to at any time and then all DAC voltages updated simultaneously by the rising edge of LOADDACS. It also allows a DAC input register to be written to at any point and the DAC voltages to be synchronously changed via a trigger signal connected to LOADDACS.

A1	A0	R/W	CS	RST	RSTSEL	LOADDACS	INPUT REGISTER	DAC REGISTER	MODE	DAC
L	L	L	L	H	X	X	Write	Hold	Write Input	A
L	H	L	L	H	X	X	Write	Hold	Write Input	B
H	L	L	L	H	X	X	Write	Hold	Write Input	C
H	H	L	L	H	X	X	Write	Hold	Write Input	D
L	L	H	L	H	X	X	Read	Hold	Read Input	A
L	H	H	L	H	X	X	Read	Hold	Read Input	B
H	L	H	L	H	X	X	Read	Hold	Read Input	C
H	H	H	L	H	X	X	Read	Hold	Read Input	D
X	X	X	H	H	X	↑	Hold	Write	Update	All
X	X	X	H	H	X	H	Hold	Hold	Hold	All
X	X	X	X	↑	L	X		Reset to Zero	Reset to Zero	All
X	X	X	X	↑	H	X		Reset to Midscale	Reset to Midscale	All

TABLE I. DAC7644 Logic Truth Table.

DIGITAL TIMING

Figure 14 and Table II provide detailed timing for the digital interface of the DAC7644.

$$V_{OUT} = V_{REF}L + \frac{(V_{REF}H - V_{REF}L) \cdot N}{65,536} \quad (1)$$

DIGITAL INPUT CODING

The DAC7644 input data is in Straight Binary format. The output voltage is given by Equation 1.

where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

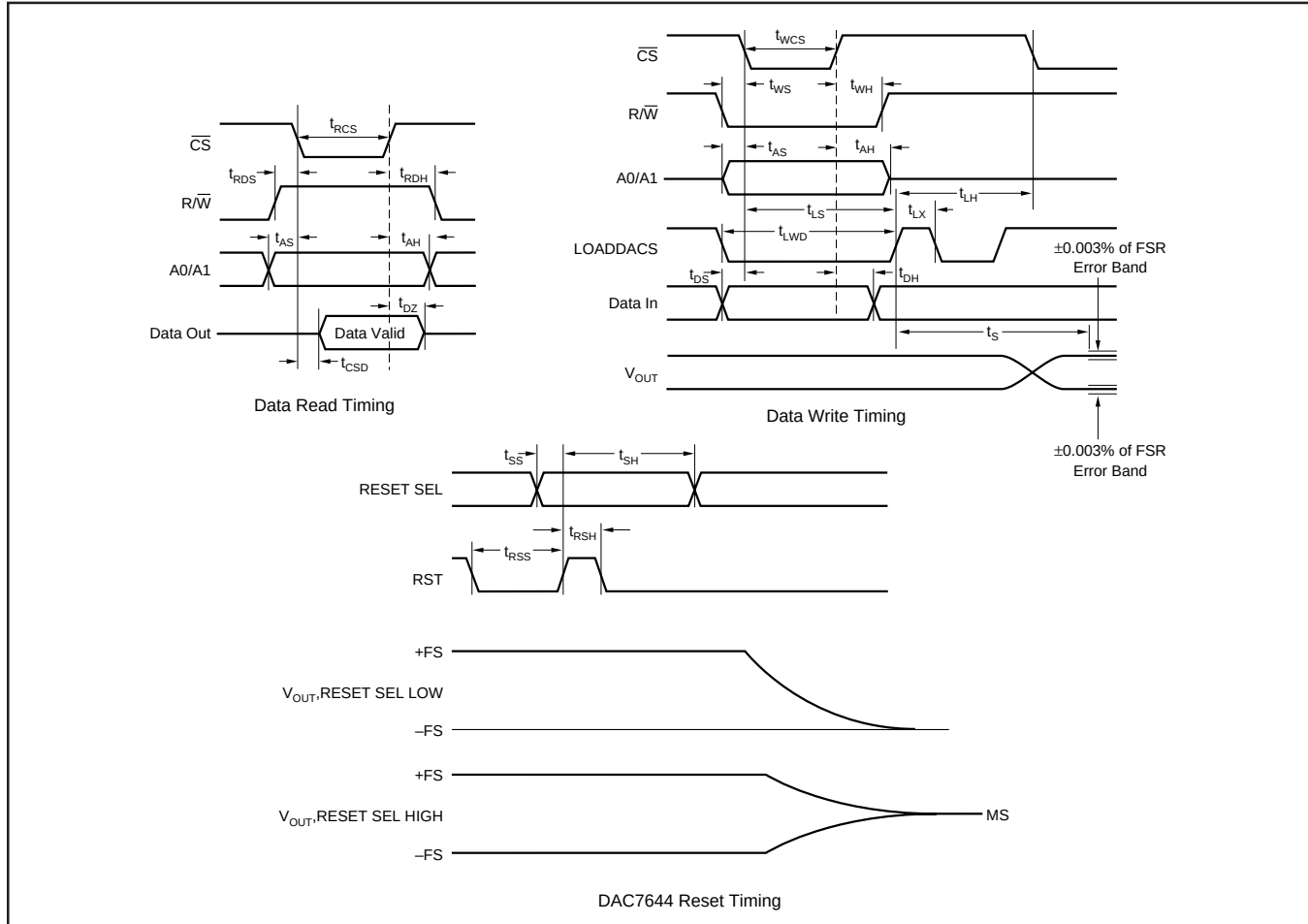


FIGURE 14. Digital Input and Output Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RCS}	$\overline{CS}$ LOW for Read	150			ns
t_{RDS}	$R/\overline{W}$ HIGH to $\overline{CS}$ LOW	10			ns
t_{RDH}	$R/\overline{W}$ HIGH after $\overline{CS}$ HIGH	10			ns
t_{DZ}	$\overline{CS}$ HIGH to Data Bus in High Impedance	10			ns
t_{CSD}	$\overline{CS}$ LOW to Data Bus Valid		100	100	ns
t_{WCS}	$\overline{CS}$ LOW for Write	40		150	ns
t_{WS}	$R/\overline{W}$ LOW to $\overline{CS}$ LOW	0			ns
t_{WH}	$R/\overline{W}$ LOW after $\overline{CS}$ HIGH	10			ns
t_{AS}	Address Valid to $\overline{CS}$ LOW	0			ns
t_{AH}	Address Valid after $\overline{CS}$ HIGH	10			ns
t_{LS}	$\overline{CS}$ LOW to LOADDACS HIGH	30			ns
t_{LH}	$\overline{CS}$ LOW after LOADDACS HIGH	100			ns
t_{LX}	LOADDACS HIGH	100			ns
t_{DS}	Data Valid to $\overline{CS}$ LOW	0			ns
t_{DH}	Data Valid after $\overline{CS}$ HIGH	10			ns
t_{LWD}	LOADDACS LOW	100			ns
t_{SS}	RSTSEL Valid Before RESET HIGH	0			ns
t_{SH}	RSTSEL Valid After RESET HIGH	200			ns
t_{RSS}	RESET LOW Before RESET HIGH	10			ns
t_{RSH}	RESET LOW After RESET HIGH	10			ns
t_S	Settling Time			10	μ s

TABLE II. Timing Specifications ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$).

The DAC7644 offers a unique set of features that allows a wide range of flexibility in designing applications circuits such as programmable current sources. The DAC7644 offers both a differential reference input as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows transistor to be placed within the loop to implement a digitally-programmable, uni-directional current source. The availability of a differential reference also allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

Figure 15 shows a DAC7644 in a 4mA to 20mA current output configuration. The output current can be determined by Equation 3:

At full-scale, the output current is 16mA plus the 4mA for the zero current. At zero scale the output current is the offset current of 4mA ($0.5\text{V}/125\Omega$).

