TOSHIBA

Multi Chip Package

SRAM & FLASH Memory

2M BIT SRAM (×8/×16)

16M BIT FLASH (×8/×16)

Data Sheet

TENTATIVE TOSHIBA MULTI CHIP INTEGRATED CIRCUIT SILICON GATE CMOS

SRAM AND FLASH MEMORY MIXED MULTI CHIP PACKAGE

DESCRIPTION

The TH50VSF1480/1481AASB is a package of mixed 2,097,152-bit Full CMOS SRAM and 16,777,216-bit FLASH memory. Using the CIOS/CIOF inputs, the system can choose the mode which will maximize its performance. The TH50VSF1480/1481AASB operates 2.7 to 3.6V power supply. The TH50VSF1480/1481AASB is available in a 65-pin BGA package to suit a variety of design applications.

FEATURES

- Power supply voltage
  V_{CCs}=2.7 to 3.6V
  V_{CCf}=2.7 to 3.6V
- Data retention supply voltage
  V_{CCs}=1.5 to 3.6V
- Power dissipation
  Operating : 45mA maximum (CMOS level)
  Standby : 7μA maximum (SRAM CMOS level)
  Standby : 5μA maximum (FLASH CMOS level)
- Block erase architecture for FLASH
  1 block by 16,384 words
  2 blocks by 8,192 words
  1 block by 32,768 words
  31 blocks by 65,536 word
- Organization

CIOF	CIOS	Flash	SRAM
V_{CC}	V_{CC}	1,048,576 words by 16 bits	131,072 words by 16 bits
V_{CC}	V_{SS}	1,048,576 words by 16 bits	262,144 words by 8 bits
V_{SS}	V_{SS}	2,097,152 words by 8 bits	262,144 words by 8 bits

- Function mode control for FLASH
  Compatible with JEDEC-standard command
- Function mode for FLASH
  Auto program
  Auto chip erase
  Auto block erase
  Auto multiple block erase
  Block erase suspend
  Block erase resume
  Data polling
  Toggle bit
- Erase and program cycle for FLASH
  10^5 cycles typical
- Boot block architecture for FLASH
  TH50VSF1480AASB : Top boot Block
  TH50VSF1481AASB : Bottom boot Block
- Package:
  P-LFBGA65-1209-0.80A3 (Weight : 0.31g typ)

PIN ASSIGNMENT (TOP VIEW)

· Case : CIOF = V_{CC}, CIOS = V_{CC}

	1	2	3	4	5	6	7	8
A		A7	$\overline{LB}$	NC	$\overline{WE}$	A8	A11	
B	A3	A6	$\overline{UB}$	$\overline{RESET}$	CE2S	A19	A12	A15
C	A2	A5	A18	RY/$\overline{BY}$	NC	A9	A13	NC
D	A1	A4	A17			A10	A14	NC
E	A0	V_{SS}	DQ1			DQ6	DU	A16
F	$\overline{CEF}$	$\overline{OE}$	DQ9	DQ3	DQ4	DQ13	DQ15	CIOF
G	$\overline{CE1S}$	DQ0	DQ10	V_{CCf}	V_{CCs}	DQ12	DQ7	V_{SS}
H		DQ8	DQ2	DQ11	CIOS	DQ5	DQ14	

PIN NAMES

A0 to A20	Address input
A12S	A12 input for SRAM
A12F	A12 input for FLASH
SA	A17 input for SRAM
DQ0 to DQ15	Data input/Output
$\overline{CE1S}$, CE2S	Chip enable input for SRAM
$\overline{CEF}$	Chip enable input for FLASH
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
$\overline{LB}$, $\overline{UB}$	Data Byte Control input
RY/$\overline{BY}$	Ready/Busy output
$\overline{RESET}$	Hardware reset input
CIOS	Word enable input for SRAM
CIOF	Word enable input for FLASH
V_{CCs}	Power supply for SRAM
V_{CCf}	Power supply for FLASH
V_{SS}	Ground
NC	No Connection
DU	Don't Use

980910EBA1

PIN ASSIGNMENT (TOP VIEW)

· Case : CIOF = V_{CC}, CIOS = V_{SS}

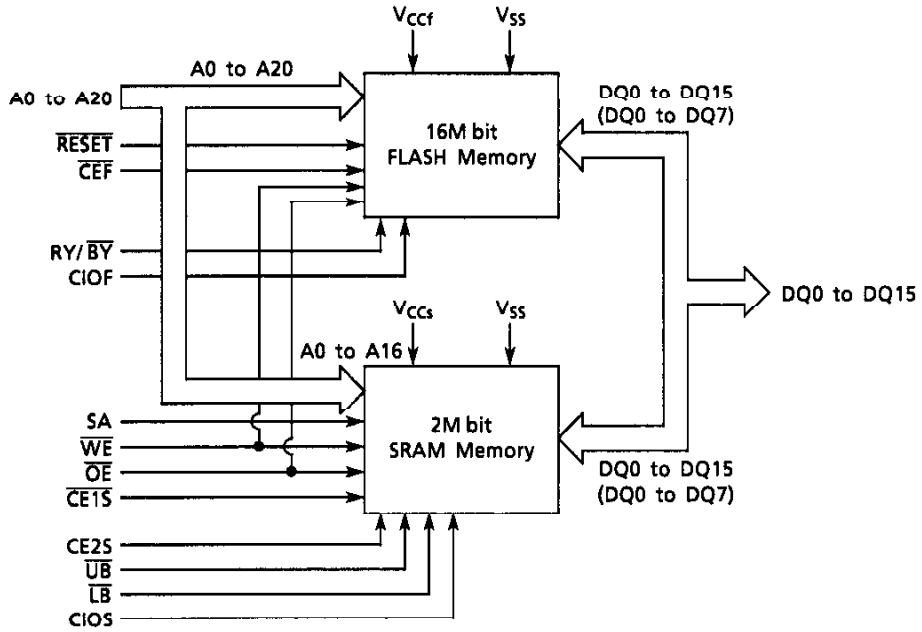
	1	2	3	4	5	6	7	8
A		A7	DU	NC	$\overline{WE}$	A8	A11	
B	A3	A6	DU	$\overline{RESET}$	CE2S	A19	A12	A15
C	A2	A5	A18	RY/$\overline{BY}$	NC	A9	A13	NC
D	A1	A4	A17			A10	A14	NC
E	A0	V_{SS}	DQ1			DQ6	SA	A16
F	$\overline{CEF}$	$\overline{OE}$	DQ9	DQ3	DQ4	DQ13	DQ15	CIOF
G	$\overline{CE1S}$	DQ0	DQ10	V_{CCf}	V_{CCs}	DQ12	DQ7	V_{SS}
H		DQ8	DQ2	DQ11	CIOS	DQ5	DQ14	

· Case : CIOF = V_{SS}, CIOS = V_{SS}

	1	2	3	4	5	6	7	8
A		A7	DU	NC	$\overline{WE}$	A8	A11	
B	A3	A6	DU	$\overline{RESET}$	CE2S	A20	A13	A16
C	A2	A5	A19	RY/$\overline{BY}$	NC	A9	A14	NC
D	A1	A4	A18			A10	A15	NC
E	A0	V_{SS}	DQ1			DQ6	A12S	A17
F	$\overline{CEF}$	$\overline{OE}$	DU	DQ3	DQ4	DU	A12F	CIOF
G	CE1S	DQ0	DU	V_{CCf}	V_{CCs}	DU	DQ7	V_{SS}
H		DU	DQ2	DU	CIOS	DQ5	DU	

Note) A12F and A12S should be wired and used as A12 pin.

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CEF}$	$\overline{CE1S}$	CE2S	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	$\overline{UB}$	$\overline{LB}$	DQ0 to DQ7	DQ8 to DQ15
FLASH Read	L	H	×	L	H	H	×	×	D_{OUT}	D_{OUT}
	L	×	L	L	H	H	×	×	D_{OUT}	D_{OUT}
SRAM Read	H	L	H	L	H	H	L	L	D_{OUT}	D_{OUT}
	H	L	H	L	H	H	H	L	D_{OUT}	High-Z
	H	L	H	L	H	H	L	H	High-Z	D_{OUT}
FLASH Write	L	H	×	H	L	H	×	×	D_{IN}	D_{IN}
	L	×	L	H	L	H	×	×	D_{IN}	D_{IN}
SRAM Write	H	L	H	×	L	H	L	L	D_{IN}	D_{IN}
	H	L	H	×	L	H	H	L	D_{IN}	High-Z
	H	L	H	×	L	H	L	H	High-Z	D_{IN}
FLASH Output Disable	×	H	×	H	H	×	×	×	High-Z	High-Z
	×	×	L	H	H	×	×	×	High-Z	High-Z
SRAM Output Disable	H	×	×	H	H	×	×	×	High-Z	High-Z
	H	×	×	×	×	×	H	H	High-Z	High-Z
FLASH Standby	H	×	×	×	×	H	×	×	S	S
FLASH Hardware Reset/Standby	×	×	×	×	×	L	×	×	S	S
SRAM Standby	×	H	×	×	×	×	×	×	F	F
	×	×	L	×	×	×	×	×	F	F

Note) L : V_{IL}, H : V_{IH}, × : V_{IH} or V_{IL}, F : Depend on FLASH operation mode,
S : Depend on SRAM operation mode
SRAM and FLASH is word mode shown(CIOS=V_{CC}, CIOF=V_{CC})
Don't apply to $\overline{CEF}$=$\overline{CE1S}$=V_{IL} and CE2S=V_{IH} at a time.

ID CODE TABLE

TYPE		A19 to A12	A6	A1	A0	CODE (HEX) (See Note 1)
Manufacturer Code		×	V_{IL}	V_{IL}	V_{IL}	0098h
Device Code	TH50VSF1480AASB	×	V_{IL}	V_{IL}	V_{IH}	00C2h
	TH50VSF1481AASB	×	V_{IL}	V_{IL}	V_{IH}	0043h
Verify Block Protect		BA (See Note 2)	V_{IL}	V_{IH}	V_{IL}	Data (See Note 3)

Note) × : V_{IH} or V_{IL}

1) DQ8 to DQ15 are High-Z in Byte mode
2) BA : Block Address
3) 0001h - Protected Block
   0000h - Unprotected Block

COMMAND SEQUENCE

COMMAND SEQUENCE		BUS WRITE CYCLES REQ'D	FIRST BUS WRITE CYCLE		SECOND BUS WRITE CYCLE		THIRD BUS WRITE CYCLE		FOURTH BUS READ/WRITE CYCLE		FIFTH BUS WRITE CYCLE		SIXTH BUS WRITE CYCLE	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset		1	XXXXH	F0H										
Read/Reset	Word	3	555H	AAH	2AAH	55H	555H	F0H	RA [1]	RD [2]				
	Byte		AAAH		555H		AAAH							
ID Read/ Verify Block Protect	Word	3	555H	AAH	2AAH	55H	555H	90H	IA [3]	ID [4]				
	Byte		AAAH		555H		AAAH							
Auto Program	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA [5]	PD [6]				
	Byte		AAAH		555H		AAAH							
Auto Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
	Byte		AAAH		555H		AAAH		AAAH		555H		AAAH	
Auto Block Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	BA [7]	30H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Block Protect	Word	6	555H	AAH	2AAH	55H	555H	9AH	555H	AAH	2AAH	55H	555H	9AH
	Byte		AAAH		555H		AAAH		AAAH		555H		AAAH	
Block Erase Suspend			Addr: V_{IH} or V_{IL}, Data: B0H											
Block Erase Resume			Addr: V_{IH} or V_{IL}, Data: 30H											

Notes: The system should generate the following address patterns:
Word mode: 555H or 2AAH to addresses A10 to A0
Byte mode: AAAH or 555H to addresses A10 to A0, A12F

DQ8 to DQ15 are ignored in Word mode.

1) RA : Read Address
2) RD : Read Data
3) IA : ID Address (A6, A1, A0)
   00H = Manufacturer Code
   01H = Device Code
   02H = Verify Block Protect (A19 to A12 = Block Address)
4) ID : ID Data
   0098H — Manufacturer Code
   00C2H — Device Code (TH50VSF1480AASB)
   0043H — Device Code (TH50VSF1481AASB)
   0001H — Protected Block
   0000H — Unprotected Block
5) PA : Program Address
6) PD : Program Data
7) BA : Block Address

BLOCK ERASE ADDRESS TABLES

TH50VSF1480AASB (Top Boot Block)

BLOCK #	A19	A18	A17	A16	A15	A14	A13	A12	BYTE MODE		WORD MODE	
									ADDRESS RANGE	SIZE	ADDRESS RANGE	SIZE
BA0	L	L	L	L	L	*	*	*	000000H - 00FFFFH	64 K bytes	00000H - 07FFFH	32 K words
BA1	L	L	L	L	H	*	*	*	010000H - 01FFFFH	64 K bytes	08000H - 0FFFFH	32 K words
BA2	L	L	L	H	L	*	*	*	020000H - 02FFFFH	64 K bytes	10000H - 17FFFH	32 K words
BA3	L	L	L	H	H	*	*	*	030000H - 03FFFFH	64 K bytes	18000H - 1FFFFH	32 K words
BA4	L	L	H	L	L	*	*	*	040000H - 04FFFFH	64 K bytes	20000H - 27FFFH	32 K words
BA5	L	L	H	L	H	*	*	*	050000H - 05FFFFH	64 K bytes	28000H - 2FFFFH	32 K words
BA6	L	L	H	H	L	*	*	*	060000H - 06FFFFH	64 K bytes	30000H - 37FFFH	32 K words
BA7	L	L	H	H	H	*	*	*	070000H - 07FFFFH	64 K bytes	38000H - 3FFFFH	32 K words
BA8	L	H	L	L	L	*	*	*	080000H - 08FFFFH	64 K bytes	40000H - 47FFFH	32 K words
BA9	L	H	L	L	H	*	*	*	090000H - 09FFFFH	64 K bytes	48000H - 4FFFFH	32 K words
BA10	L	H	L	H	L	*	*	*	0A0000H - 0AFFFFH	64 K bytes	50000H - 57FFFH	32 K words
BA11	L	H	L	H	H	*	*	*	0B0000H - 0BFFFFH	64 K bytes	58000H - 5FFFFH	32 K words
BA12	L	H	H	L	L	*	*	*	0C0000H - 0CFFFFH	64 K bytes	60000H - 67FFFH	32 K words
BA13	L	H	H	L	H	*	*	*	0D0000H - 0DFFFFH	64 K bytes	68000H - 6FFFFH	32 K words
BA14	L	H	H	H	L	*	*	*	0E0000H - 0EFFFFH	64 K bytes	70000H - 77FFFH	32 K words
BA15	L	H	H	H	H	*	*	*	0F0000H - 0FFFFFH	64 K bytes	78000H - 7FFFFH	32 K words
BA16	H	L	L	L	L	*	*	*	100000H - 10FFFFH	64 K bytes	80000H - 87FFFH	32 K words
BA17	H	L	L	L	H	*	*	*	110000H - 11FFFFH	64 K bytes	88000H - 8FFFFH	32 K words
BA18	H	L	L	H	L	*	*	*	120000H - 12FFFFH	64 K bytes	90000H - 97FFFH	32 K words
BA19	H	L	L	H	H	*	*	*	130000H - 13FFFFH	64 K bytes	98000H - 9FFFFH	32 K words
BA20	H	L	H	L	L	*	*	*	140000H - 14FFFFH	64 K bytes	A0000H - A7FFFH	32 K words
BA21	H	L	H	L	H	*	*	*	150000H - 15FFFFH	64 K bytes	A8000H - AFFFFH	32 K words
BA22	H	L	H	H	L	*	*	*	160000H - 16FFFFH	64 K bytes	B0000H - B7FFFH	32 K words
BA23	H	L	H	H	H	*	*	*	170000H - 17FFFFH	64 K bytes	B8000H - BFFFFH	32 K words
BA24	H	H	L	L	L	*	*	*	180000H - 18FFFFH	64 K bytes	C0000H - C7FFFH	32 K words
BA25	H	H	L	L	H	*	*	*	190000H - 19FFFFH	64 K bytes	C8000H - CFFFFH	32 K words
BA26	H	H	L	H	L	*	*	*	1A0000H - 1AFFFFH	64 K bytes	D0000H - D7FFFH	32 K words
BA27	H	H	L	H	H	*	*	*	1B0000H - 1BFFFFH	64 K bytes	D8000H - DFFFFH	32 K words
BA28	H	H	H	L	L	*	*	*	1C0000H - 1CFFFFH	64 K bytes	E0000H - E7FFFH	32 K words
BA29	H	H	H	L	H	*	*	*	1D0000H - 1DFFFFH	64 K bytes	E8000H - EFFFFH	32 K words
BA30	H	H	H	H	L	*	*	*	1E0000H - 1EFFFFH	64 K bytes	F0000H - F7FFFH	32 K words
BA31	H	H	H	H	H	L	*	*	1F0000H - 1F7FFFH	32 K bytes	F8000H - FBFFFH	16 K words
BA32	H	H	H	H	H	H	L	L	1F8000H - 1F9FFFH	8 K bytes	FC000H - FCFFFH	4 K words
BA33	H	H	H	H	H	H	L	H	1FA000H - 1FBFFFH	8 K bytes	FD000H - FDFFFH	4 K words
BA34	H	H	H	H	H	H	H	*	1FC000H - 1FFFFFH	16 K bytes	FE000H - FFFFFH	8 K words

BLOCK ERASE ADDRESS TABLES

TH50VSF1481AASB (Bottom Boot Block)

BLOCK #	A19	A18	A17	A16	A15	A14	A13	A12	BYTE MODE		WORD MODE	
									ADDRESS RANGE	SIZE	ADDRESS RANGE	SIZE
BA0	L	L	L	L	L	L	L	*	000000H - 003FFFH	16 K bytes	00000H - 01FFFH	8 K words
BA1	L	L	L	L	L	L	H	L	004000H - 005FFFH	8 K bytes	02000H - 02FFFH	4 K words
BA2	L	L	L	L	L	L	H	H	006000H - 007FFFH	8 K bytes	03000H - 03FFFH	4 K words
BA3	L	L	L	L	L	H	*	*	008000H - 00FFFFH	32 K bytes	04000H - 07FFFH	16 K words
BA4	L	L	L	L	H	*	*	*	010000H - 01FFFFH	64 K bytes	08000H - 0FFFFH	32 K words
BA5	L	L	L	H	L	*	*	*	020000H - 02FFFFH	64 K bytes	10000H - 17FFFH	32 K words
BA6	L	L	L	H	H	*	*	*	030000H - 03FFFFH	64 K bytes	18000H - 1FFFFH	32 K words
BA7	L	L	H	L	L	*	*	*	040000H - 04FFFFH	64 K bytes	20000H - 27FFFH	32 K words
BA8	L	L	H	L	H	*	*	*	050000H - 05FFFFH	64 K bytes	28000H - 2FFFFH	32 K words
BA9	L	L	H	H	L	*	*	*	060000H - 06FFFFH	64 K bytes	30000H - 37FFFH	32 K words
BA10	L	L	H	H	H	*	*	*	070000H - 07FFFFH	64 K bytes	38000H - 3FFFFH	32 K words
BA11	L	H	L	L	L	*	*	*	080000H - 08FFFFH	64 K bytes	40000H - 47FFFH	32 K words
BA12	L	H	L	L	H	*	*	*	090000H - 09FFFFH	64 K bytes	48000H - 4FFFFH	32 K words
BA13	L	H	L	H	L	*	*	*	0A0000H - 0AFFFFH	64 K bytes	50000H - 57FFFH	32 K words
BA14	L	H	L	H	H	*	*	*	0B0000H - 0BFFFFH	64 K bytes	58000H - 5FFFFH	32 K words
BA15	L	H	H	L	L	*	*	*	0C0000H - 0CFFFFH	64 K bytes	60000H - 67FFFH	32 K words
BA16	L	H	H	L	H	*	*	*	0D0000H - 0DFFFFH	64 K bytes	68000H - 6FFFFH	32 K words
BA17	L	H	H	H	L	*	*	*	0E0000H - 0EFFFFH	64 K bytes	70000H - 77FFFH	32 K words
BA18	L	H	H	H	H	*	*	*	0F0000H - 0FFFFFH	64 K bytes	78000H - 7FFFFH	32 K words
BA19	H	L	L	L	L	*	*	*	100000H - 10FFFFH	64 K bytes	80000H - 87FFFH	32 K words
BA20	H	L	L	L	H	*	*	*	110000H - 11FFFFH	64 K bytes	88000H - 8FFFFH	32 K words
BA21	H	L	L	H	L	*	*	*	120000H - 12FFFFH	64 K bytes	90000 - 97FFFH	32 K words
BA22	H	L	L	H	H	*	*	*	130000H - 13FFFFH	64 K bytes	98000H - 9FFFFH	32 K words
BA23	H	L	H	L	L	*	*	*	140000H - 14FFFFH	64 K bytes	A0000H - A7FFFH	32 K words
BA24	H	L	H	L	H	*	*	*	150000H - 15FFFFH	64 K bytes	A8000H - AFFFFH	32 K words
BA25	H	L	H	H	L	*	*	*	160000H - 16FFFFH	64 K bytes	B0000H - B7FFFH	32 K words
BA26	H	L	H	H	H	*	*	*	170000H - 17FFFFH	64 K bytes	B8000H - BFFFFH	32 K words
BA27	H	H	L	L	L	*	*	*	180000H - 18FFFFH	64 K bytes	C0000H - C7FFFH	32 K words
BA28	H	H	L	L	H	*	*	*	190000H - 19FFFFH	64 K bytes	C8000H - CFFFFH	32 K words
BA29	H	H	L	H	L	*	*	*	1A0000H - 1AFFFFH	64 K bytes	D0000H - D7FFFH	32 K words
BA30	H	H	L	H	H	*	*	*	1B0000H - 1BFFFFH	64 K bytes	D8000H - DFFFFH	32 K words
BA31	H	H	H	L	L	*	*	*	1C0000H - 1CFFFFH	64 K bytes	E0000H - E7FFFH	32 K words
BA32	H	H	H	L	H	*	*	*	1D0000H - 1DFFFFH	64 K bytes	E8000H - EFFFFH	32 K words
BA33	H	H	H	H	L	*	*	*	1E0000H - 1EFFFFH	64 K bytes	F0000H - F7FFFH	32 K words
BA34	H	H	H	H	H	*	*	*	1F0000H - 1FFFFFH	64 K bytes	F8000H - FFFFFH	32 K words

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RANGE	UNIT
VCC	VCCs/VCCf Supply	−0.3 to 4.6	V
V_{IN}	Input Voltage (See Note 1)	−0.3 to 4.6	V
$V_{I/O}$	Input/Output Voltage	−0.5 to VCC+0.5	V
T_{OPR}	Operating Temperature	−20 to 85	°C
P_D	Power Dissipation	0.6	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
I_{OSHORT}	Output Short Circuit Current (See Note 2)	100	mA
N_{EW}	Erase/Program Cycling Capability	100,000	Cycle
T_{STRG}	Storage Temperature	−55 to 125	°C

Note) 1) −2V (Pulse width of 20ns Max)
2) Output shorted for no more than one second. No more than one output should be shorted at a time.

HARDWARE STATUS FLAGS

STATUS		DQ7	DQ6	DQ5	DQ3	RY/$\overline{BY}$
In Progress	Auto Programming	DQ7	Toggle	0	0	0
	Auto Erase (Erase Hold Time)	0	Toggle	0	0	0
	Auto Erase	0	Toggle	0	1	0
Exceeded Time Limits	Auto Programming	$\overline{DQ7}$	Toggle	1	1	0
	Auto Erase	0	Toggle	1	1	0

Notes : 1. DQ outputs cell data and RY/$\overline{BY}$ outputs '1' when the operation has completed.
2. DQ0, DQ1, DQ2 are reserved for future use.
3. DQ8 to DQ15 : Output '0' or '1' in Word mode.
4. DQ0 to DQ2, DQ4 : Output '0'.

DC RECOMMENDED OPERATING CONDITIONS (Ta = −20° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CCs}/ V_{CCf}	V_{CC} Supply Voltage	2.7	—	3.6	V
V_{IH}	Input High Level Voltage	2.2	—	V_{CCs} + 0.3 or V_{CCf} + 0.3	V
V_{IL}	Input Low Level Voltage (See Note)	−0.3	—	0.6	V
V_{DH}	Data Retention Voltage for SRAM	1.5	—	3.6	V
V_{LKO}	FLASH Low Lock Voltage	—	—	2.5	V

Note) −2V (Pulse width of 20ns Max)

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance	V_{IN} = GND	—	—	T.B.D	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	—	—	T.B.D	pF

Note) This parameter is periodically sampled and is not 100% tested.

DC CHARACTERISTICS (Ta = −20° to 85°C, V_{CCs}/ V_{CCf} = 2.7 to 3.6V)

SYMBOL	PARAMETER	CONDITION			MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0V to V_{CC}			–	–	±1.0	μA
I_{SOH}	SRAM Output High current	V_{OH} = V_{CCs}−0.5V			−0.5	–	–	mA
I_{SOL}	SRAM Output Low Current	V_{OL} = 0.4V			2.1	–	–	mA
I_{FOH1}	FLASH Output High Current (TTL)	V_{OH} = 2.4V			−0.4	–	–	mA
I_{FOH2}	FLASH Output High Current (CMOS)	V_{OH} = V_{CCf}×0.85			−2.5	–	–	mA
		V_{OH} = V_{CCf}−0.4V			−100	–	–	μA
I_{FOL}	FLASH Output Low Current	V_{OL} = 0.4V			4.0	–	–	mA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}, $\overline{OE}$ = V_{IH}			–	–	±1.0	μA
I_{CCO1}	FLASH Average Read Current	$\overline{CEF}$ = V_{IL}, $\overline{OF}$ = V_{IH} I_{OUT} = 0mA, t_{CYCLE} = t_{RC} (min)			–	–	30	mA
I_{CCO2}	FLASH Average Program/Erase Current	$\overline{CEF}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0mA			–	–	40	mA
I_{CCO3}	SRAM Average Operating Current	$\overline{CE1S}$ = V_{IL}, CE2S = V_{IH}, $\overline{OE}$ = V_{IH} I_{OUT} = 0mA		t_{CYCLE} = t_{RC}	–	–	50	mA
				t_{CYCLE} = 1MHz	–	–	12	
I_{CCO4}		$\overline{CE1S}$ = 0.2V, $\overline{OE}$ = V_{CCs}−0.2V CE2S = V_{CCs}−0.2V, I_{OUT} = 0mA		t_{CYCLE} = t_{RC}	–	–	45	mA
				t_{CYCLE} = 1MHz	–	–	6	
I_{CCS1}	FLASH Standby Current	$\overline{CEF}$ = V_{IH}, $\overline{RESET}$ = V_{IH} or $\overline{RESET}$ = V_{IL}			–	–	250	μA
I_{CCS2}		$\overline{CEF}$ = $\overline{RESET}$ = V_{CCf}±0.2V or $\overline{RESET}$ = ±0.2V			–	–	5	μA
I_{CCS3}	SRAM Standby Current	$\overline{CE1S}$ = V_{IH} or CE2S = V_{IL}			–	–	2	mA
I_{CCS4}		$\overline{CE1S}$ = V_{CCs}−0.2V or CE2S = 0.2V (See Note)	V_{CCs} = 3.0V	Ta = 25°C	–	0.01	0.5	μA
				Ta = −20° to 40°C	–	–	1	
				Ta = −20° to 85°C	–	–	5	
			V_{CCs} = 3V±10%	Ta = 25°C	–	–	0.6	
				Ta = −20° to 85°C	–	–	6	
			V_{CCs} = 3.3V±0.3V	Ta = 25°C	–	–	0.7	
				Ta = −20° to 85°C	–	–	7	

Note) In standby mode with $\overline{CE1S} \geqq V_{CCs} - 0.2V$, these limits are assured for the condition $CE2S \geqq V_{CCs} - 0.2V$ or $CE2S \leqq 0.2V$.

AC CHARACTERISTICS(SRAM) (Ta = −20° to 85°C, V_{CCS} = 2.7 to 3.6V)

READ CYCLE

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{RC}	Read Cycle Time	100	−	ns
t_{ACC}	Address Access Time	−	100	
t_{CO1}	Chip Enable ($\overline{CE1S}$) Access Time	−	100	
t_{CO2}	Chip Enable (CE2S) Access Time	−	100	
t_{OE}	Output Enable Access Time	−	50	
t_{BA}	Data Byte Control Access Time	−	50	
t_{COE}	Chip Enable Low to Output Active	5	−	
t_{OEE}	Output Enable Low to Output Active	0	−	
t_{BE}	Data Byte Control Low to Output Active	0	−	
t_{OD}	Chip Enable High to Output High-Z	−	40	
t_{ODO}	Output Enable High to Output High-Z	−	40	
t_{BD}	Data Byte Control High to Output High-Z	−	40	
t_{OH}	Output Data Hold Time	10	−	
t_{CCR}	CE Recovery Time	0	−	

WRITE CYCLE

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{WC}	Write Cycle Time	100	−	ns
t_{WP}	Write Pulse Width	60	−	
t_{CW}	Chip Enable to End of Write	80	−	
t_{BW}	Data Byte Control to End of Write	60	−	
t_{AS}	Address Setup Time	0	−	
t_{WR}	Write Recovery Time	0	−	
t_{ODW}	$\overline{WE}$ Low to Output High-Z	−	40	
t_{OEW}	$\overline{WE}$ High to Output Active	0	−	
t_{DS}	Data Setup Time	40	−	
t_{DH}	Data Hold Time	0	−	

AC TEST CONDITIONS

PARAMETER	CONDITION
Input Pulse Level	2.4V / 0.4V
Input Pulse Rise and Fall Time (10% to 90%)	5ns
Timing measurement Reference Level (Input)	1.5V / 1.5V
Timing measurement Reference Level (Output)	1.5V / 1.5V
Output Load	CL (100pF) + 1TTL Gate

AC CHARACTERISTICS(FLASH) (Ta = −20° to 85°C, V_{CCf} = 2.7 to 3.6V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{RC}	Read Cycle Time	100	—	ns
t_{ACC}	Address Access Time	—	100	ns
t_{CE}	$\overline{CEF}$ Access Time	—	100	ns
t_{OE}	$\overline{OE}$ Access Time	—	40	ns
t_{CEE}	$\overline{CEF}$ to Output Low-Z	0	—	ns
t_{OEE}	$\overline{OE}$ to Output Low-Z	0	—	ns
t_{OEH}	$\overline{OE}$ Hold Time (Read)	0	—	ns
t_{OH}	Output Data Hold Time	0	—	ns
t_{DF1}	$\overline{CEF}$ to Output High-Z	—	30	ns
t_{DF2}	$\overline{OE}$ to Output High-Z	—	30	ns
t_{CMD}	Command Write Cycle Time	100	—	ns
t_{AS}	Address Setup Time	0	—	ns
t_{AH}	Address Hold Time	50	—	ns
t_{DS}	Data Setup Time	50	—	ns
t_{DH}	Data Hold Time	0	—	ns
t_{WELH}	$\overline{WE}$ Low Level Hold Time ($\overline{WE}$ Control)	50	—	ns
t_{WEHH}	$\overline{WE}$ High Level Hold Time ($\overline{WE}$ Control)	20	—	ns
t_{CES}	$\overline{CEF}$ Setup Time to $\overline{WE}$ Active ($\overline{WE}$ Control)	0	—	ns
t_{CEH}	$\overline{CEF}$ Hold Time from $\overline{WE}$ High Level ($\overline{WE}$ Control)	0	—	ns
t_{CELH}	$\overline{CEF}$ Low Level Hold Time ($\overline{CEF}$ Control)	50	—	ns
t_{CEHH}	$\overline{CEF}$ High Level Hold Time ($\overline{CEF}$ Control)	20	—	ns
t_{WES}	$\overline{WE}$ Setup Time to $\overline{CEF}$ Active ($\overline{CEF}$ Control)	0	—	ns
t_{WEH}	$\overline{WE}$ Hold Time from High Level ($\overline{CEF}$ Control)	0	—	ns
t_{OES}	$\overline{OE}$ Setup to $\overline{WE}$ Active	0	—	ns
t_{OEHP}	$\overline{OE}$ Hold Time (Toggle / Data Polling)	10	—	ns
t_{OEHT}	$\overline{OE}$ High Level Hold Time (Toggle)	20	—	ns
t_{PPW}	Auto Program Time	16 *	3600	µs
t_{PCEW}	Auto Chip Erase Time	50 *	—	s
t_{PBEW}	Auto Block Erase Time	1.5 *	15	s
t_{VCS}	V_{CC} Setup Time	500	—	µs
t_{BUSY}	Program / Erase Valid to RY / $\overline{BY}$ Delay	40	—	ns
t_{RP}	$\overline{RESET}$ Low Level Hold Time	500	—	ns
t_{READY}	$\overline{RESET}$ Low Level to Read Mode	—	20	µs
t_{RB}	RY / $\overline{BY}$ Recovery Time	0	—	ns
t_{RH}	$\overline{RESET}$ Recovery Time	500	—	ns
t_{VPH}	$\overline{OE}$ Hold Time (Block Protect)	8	—	µs
t_{PPLH}	$\overline{WE}$ Low Level Hold Time (Block Protect)	100	—	µs
t_{PAS}	Protect Address Setup Time	0	—	ns
t_{PAH}	Protect Address Hold Time	0	—	ns
t_{CESP}	$\overline{CEF}$ Setup Time (Block Protect)	4	—	µs
t_{CEHP}	$\overline{CEF}$ Hold Time (Block Protect)	8	—	µs
t_{SUS}	Suspend Command to Suspend Mode	—	15	µs
t_{RES}	Resume Command to Erase Mode	—	1	µs
t_{CCR}	CE Recovery Time	0	—	ns

* : Typ

FUNCTION MODE for FLASH

Read Mode

When the device is set to Read mode, it acts as an asynchronous ROM with an access time of 100 ns. The device is set to Read mode at power-on or when an Auto - Program / Erase operation completes. A software or hardware reset is necessary to return the device to Read mode when an Auto Program / Erase operation fails.

Standby Mode

There are two methods of entering Standby mode: the first involves using both $\overline{CEF}$ and $\overline{RESET}$ and the second using only $\overline{RESET}$.

The first method involves using $\overline{CEF}$ and $\overline{RESET}$ for mode control. If $V_{CCf} \pm 0.2$ V (CMOS level) is applied to $\overline{CEF}$ and $\overline{RESET}$ when the device is operating in Read mode, the current is reduced below 5μA. Similarly, if V_{IH} (TTL level) is applied to $\overline{CEF}$ and $\overline{RESET}$, the current is reduced below 250 μA. When using $\overline{CEF}$ for control, make sure that the device is operating in Read mode; otherwise, it is not possible to enter Standby mode.

The second method involves using only $\overline{RESET}$ for mode control. If $V_{SS} \pm 0.2$ V (CMOS level) is applied to $\overline{RESET}$ when the device is operating in Read mode, the current is reduced below 5 μA. Similarly, if V_{IL} (TTL level) is applied to $\overline{RESET}$, the current is reduced below 250 μA. The difference the control method using $\overline{CEF}$ described above, is that if V_{IL} is applied to $\overline{RESET}$ when the device is operating in any mode other than Read mode, it enters Standby mode after stopping the operating which is currently being executed. This is a hardware reset and is described later.

In standby mode, DQ is put in high-impedance state.

Command Write

The TH50VSF1480/1481AASB utilizes the JEDEC command control standard for a single power supply E²PROM. A command is executed by inputting an address and data into the Command register. The command is entered by a $\overline{WE}$ Control Write ($\overline{WE}$ pulse with $\overline{CEF} = V_{IL}$ and $\overline{OE} = V_{IH}$) or a $\overline{CEF}$ Control Write ($\overline{CEF}$ pulse with $\overline{WE} = V_{IL}$ and $\overline{OE} = V_{IH}$). The address is latched on the falling edge of either $\overline{WE}$ or $\overline{CEF}$. The data is latched on the rising edge of either $\overline{WE}$ or $\overline{CEF}$. DQ0 to 7 are valid for data input and DQ8 to 15 are ignored.

A command is when the Reset command is input. The device then enters Read Mode. When an undefined command is input, the Command register is reset and the device enters Read mode.

RESET (Software Reset)

The device does not enter Read mode automatically when a command such as Auto Program / Erase or ID Read is not correctly executed (for example, if Program or Erase fails). The Reset or Read Command is necessary to return the device to Read mode. The Reset and Read commands must also be used to reset the Command register.

RESET (Hardware Reset)

A hardware reset is used for aborting Auto mode operations such as Auto Program/Erase and for resetting the operation mode. The device enters Read mode 20 μs after a 500ns low level input pulse to the $\overline{RESET}$ pin. Data may be corrupted if the device is reset during an auto mode operation.

After a hardware reset the device enters Read mode when $\overline{RESET} = V_{IH}$ and Standby mode when $\overline{RESET} = V_{IL}$. The DQ pins are High-Impedance when $\overline{RESET} = V_{IL}$. The Read operation sequence and input of any command are allowed after the device enters Read mode.

ID Read Mode

The ID Read mode is used to establish the device type. The ID Read mode is set either from the Command mode by inputting a 90H command.

When A0, A1 and A6 = V_{IL}, the data that is read is the manufacturer code (0098H). When A0 = V_{IH} and A1 and A6 = V_{IL}, the data that is read is the device code (TH50VSF1480AASB : 00C2h / TH50VSF1481AASB : 0043h). The access time for an ID Read is the same as that of a normal Read operation. DQ8 to DQ15 are in High-Impedance state in Byte mode.

Auto Program Mode

The TH50VSF1480/1481AASB can be programmed in either byte or word units. The Auto Program mode is set using the Program command. The program address is latched on the falling edge of the $\overline{WE}$ signal and data is latched on the rising edge of the fourth bus cycle. Auto programming starts on the rising edge of the $\overline{WE}$ signal in the fourth bus cycle. The Program and Program Verify commands are automatically executed by the chip. The device status during programming is determined from the Hardware Sequence flag.

Programming of a protected block is ignored. The device enters Read mode 3 μs after the rising edge of the $\overline{WE}$ signal in the fourth bus cycle.

The device allows the programming of memory cells from 1 to 0. The programming of Memory cells from 0 to 1 will fail. A cell must be erased to turn it from 0 to 1.

If an Auto Program operation fails, the device remains in programming state and does not automatically return to Read mode. The device status can be determined from the setting of the Hardware Sequence flag. Either a Reset command or a hardware reset is necessary to return the device to Read mode after a failure.

If a programming operation fails, please do not try to use the block which contains the address to which data could not be programmed.

Auto Chip Erase Mode

The Auto Chip Erase mode is set using the Chip Erase command. The Auto Chip Erase operation starts on the rising edge of $\overline{WE}$ in the sixth bus cycle. All memory cells are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is determined from the Hardware Sequence flag.

Command inputs are ignored during an Auto Chip Erase. The hardware reset allows interruption of an Auto Chip Erase operation. The Auto Chip Erase operation does not complete correctly when interrupted. Hence a further Erase operation is necessary.

An attempt to erase a protected block is ignored. If all blocks are protected, the Auto Erase operation will not be executed and the device will enter Read mode 100 μs after the rising edge of the $\overline{WE}$ signal in the sixth bus cycle.

If an Auto Chip Erase operation fails, the device remains in, erasing state and does not return to Read mode. The device status is determined from the Hardware Sequence flag. Either a Reset command or a hardware reset is necessary to return the device to Read mode after a failure.

Auto Block / Multi Block Erase Mode

The Auto Block and Multi Block Erase modes are set using the Block Erase command. The block address is latched on the falling edge of the $\overline{WE}$ signal in the sixth bus cycle. The Block Erase starts as soon as the hold time has elapsed after the rising edge of the $\overline{WE}$ signal. All memory cells in the selected block are automatically programmed to 0, erased and verified as erased by the chip. The Multi Block Erase operation allows erasing of multiple blocks. Any additional block addresses or Multi Block Erase commands must be input within the Erase Hold Time - that is, within 50 µs of any $\overline{WE}$ signal rising edge. The device status can be determined from the setting of the Hardware Sequence flag.

Commands (except Erase Suspend) are ignored during a Block/Multi Block Erase operation. The operation can be aborted by a hardware reset. The Auto Erase operation does not complete correctly when aborted, therefore, a further Erase operation is necessary.

An attempt to erase a protected block is ignored. If all the selected blocks are protected, the Auto Erase operation is not executed and the device returns to Read mode 100 µs after the rising edge of the $\overline{WE}$ signal in the last bus cycle.

If an Auto Erase operation fails, the device remains in erasing state and does not return to Read mode. The device status is determined from the Hardware Sequence flag. Either a Reset command or a hardware reset is necessary to return the device to Read mode after a failure.

Erase Suspend / Resume Mode

The Erase Suspend mode is used to read data from a block not selected for erasing. The Erase Suspend command is allowed during a Block Erase operation or during the Block Erase Hold Time; it is ignored in other operation modes. A Block Erase operation is also suspended if the Suspend command is input during the Block Erase Hold Time. The device is reset if any command other than Suspend is input. The suspended device recognizes only Read and Resume commands.

The device enters Suspend mode 15 µs after the Erase Suspend command is input. The device then enters a pseudo-Read Mode. Data can be read out from an unselected block but is invalid if the address is set to a block selected for erasing. The device status can be determined from the Hardware Sequence flag. DQ6 (the toggle bit) stops toggling and RY/$\overline{BY}$ outputs 1 once the device is set to pseudo-Read mode. The host processor must track the current device mode since there is no way of telling whether the device is in pseudo-or ordinary Read mode. The device remains in pseudo-Read mode even if a Suspend command is input.

The device restarts the Block Erase operation after receiving a Resume command. The device returns to the status in which the Suspend command was input. The DQ6 output toggles and RY/$\overline{BY}$ outputs a 0.

Block Protect

The TH50VSF1480/1481AASB has a block Protection feature to prevent programing and erasing of protected blocks. The initial device is shipped with all blocks unprotected. A block can also be protected using a software command. Block protection is executed by setting the $\overline{WE}$ signal to Low for t_{PPLH} while $\overline{CEF} = V_{IL}$. After the command input in the sixth bus cycle A12 to A19 = the block address. Block protection can be verified using the Verify Block Protect command.

Verify Block Protect

The Verify Block Protect command is used to check whether a block is protected or unprotected. In Word mode 0001h is output when the block is protected and 0000h is output when it is unprotected. DQ8 to DQ15 are in High-Impedance state in Byte mode. A Verify Block Protection can also be enabled by using a software command.

HARDWARE SEQUENCE FLAG for FLASH

The TH50VSF1480/1481AASB has a Hardware Sequence flag which allows the device status to be determined during Auto operation. The output data is read out with the same timing as Read mode at $\overline{CEF} = \overline{OE} = V_{IL}$. RY/$\overline{BY}$ outputs either High or Low.

The device re-enters the Read mode automatically after Auto operation has completed successfully. The device status is read out from the Hardware Sequence flag and the operation result is verified by comparing the read-out data to the original data.

DQ7 ($\overline{DATA}$ Polling)

The device status can be determined using the data polling function during an Auto Program or Auto Erase operation. $\overline{DATA}$ polling begins on the rising edge of $\overline{WE}$ in the last bus cycle. In an Auto Program operation, DQ7 outputs inverted data during the programming operation and outputs real data after programming has finished. In an Auto Erase operation, DQ7 outputs 0 during the Erase operation and outputs 1 when the Erase operation has finished. If an Auto Program or Auto Erase operation fails, DQ7 simply outputs the data.

The latched address is reset after an operation has finished. The polling data is asynchronous with the $\overline{OE}$ signal.

DQ6 (Toggle Bit)

The device status can be determined by the Toggle Bit function during an Auto Program or Auto Erase operation. The Toggle bit begins toggling on the rising edge of $\overline{WE}$ in the last bus cycle. DQ6 alternately outputs a 0 or a 1 for each attempt ($\overline{OE}$ access) while $\overline{CEF} = V_{IL}$ while the device is busy. When the internal operation has been completed, toggling stops and valid memory cell data can be read by subsequent reading. If the operation failed, the DQ6 output toggles.

DQ6 toggles for around 3 μs when an attempt is made to execute an Auto Program operation on a protected block. It then stops toggling. DQ6 toggles for around 100 μs when an attempt is made to execute an Auto Erase operation on a protected block. It then stops toggling. After toggling stops the device returns to Read mode.

DQ5 (Internal Time-out)

DQ5 outputs a 1 when the Internal Timer has timed out during a Program or Erase operation. This indicates that the operation has not completed within the allotted time.

An attempt to program 1 into a cell containing 0 will fail (see Auto Program mode). DQ5 outputs 1 in this case. Either a hardware reset or a software Reset command is required to put the device into Read mode.

DQ3 (Block Erase Timer)

The Block Erase operation starts 50 μs (Erase Hold Time) after the rising edge of $\overline{WE}$ in the last command cycle. DQ3 outputs a 0 during the Block Erase Hold Time and a 1 when the Erase operation starts. Additional Block Erase commands can only be accepted during this Block Erase Hold Time. Each Block Erase command received within this hold time resets the timer, allowing additional blocks to be marked for erasing. DQ3 outputs a 1 if the Program or Erase operation fails.

RY/$\overline{BY}$ (READY/$\overline{BUSY}$)

TH50VSF1480/1481AASB has a RY/$\overline{BY}$ signal to indicate the device status to the host processor. A 0 (Busy state) indicates that an Auto Program or Auto Erase operation is in progress. A 1 (Ready state) indicates that the operation has finished and that the device can accept a new command. The RY/$\overline{BY}$ signal outputs a 0 when an operation has failed.

The RY/$\overline{BY}$ signal outputs a 0 after the rising edge of $\overline{WE}$ in the last command cycle of a Program operation and during the Erase Hold Time after the last command cycle of an Erase operation.

During an Auto Block Erase operation, commands other than Erase Suspend are ignored. The RY/$\overline{BY}$ signal outputs a 1 during an Erase Suspend operation. The output buffer for the RY/$\overline{BY}$ pin is an open drain type circuit, allowing a wired−OR connection. A pull-up resistor needs to be inserted between V_{CCf} and the RY/$\overline{BY}$ pin.

DATA PROTECTION

The TH50VSF1480/1481AASB utilizes a JEDEC standard command sequence which protects data against accidental alteration due to noise.

V_{CCf} Lock-out Voltage

The device is reset when V_{CCf} is less than V_{LKO} to protect memory cell data against V_{CCf} noise, and during power-up and power-down. An Auto Program or Erase operation stops when V_{CCf} drops below V_{LKO}. An Erase Suspend operation is reset and an Erase operation stops if the device is in Suspend mode. An operation will not complete correctly if it is interrupted by V_{CCf} Lock-out.

$\overline{WE}$ Glitch Pulses

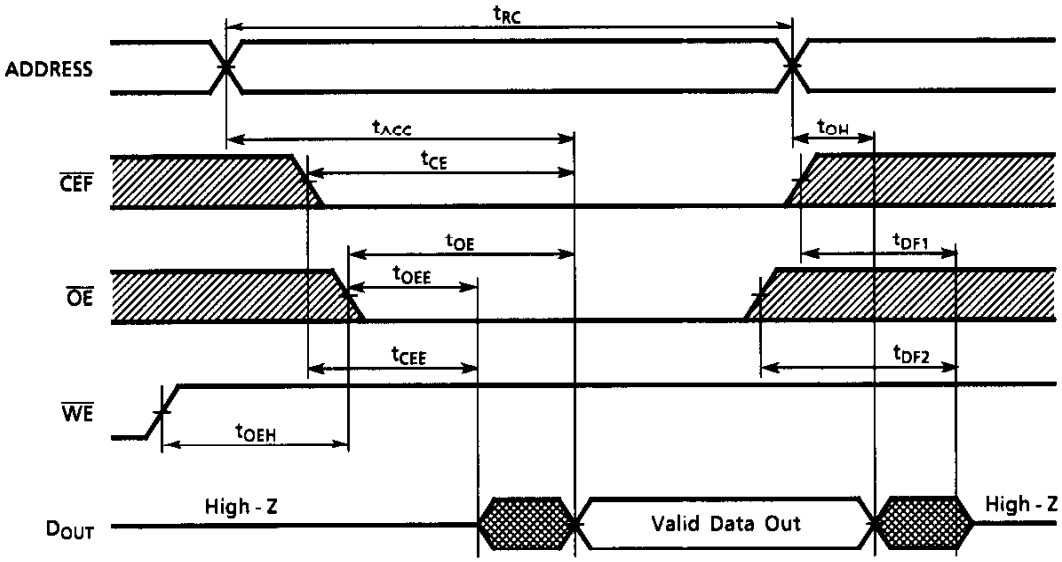
Glitches must be suppressed (to less than 5 ns) in order for operation to proceed smoothly.

Protection at Power-on

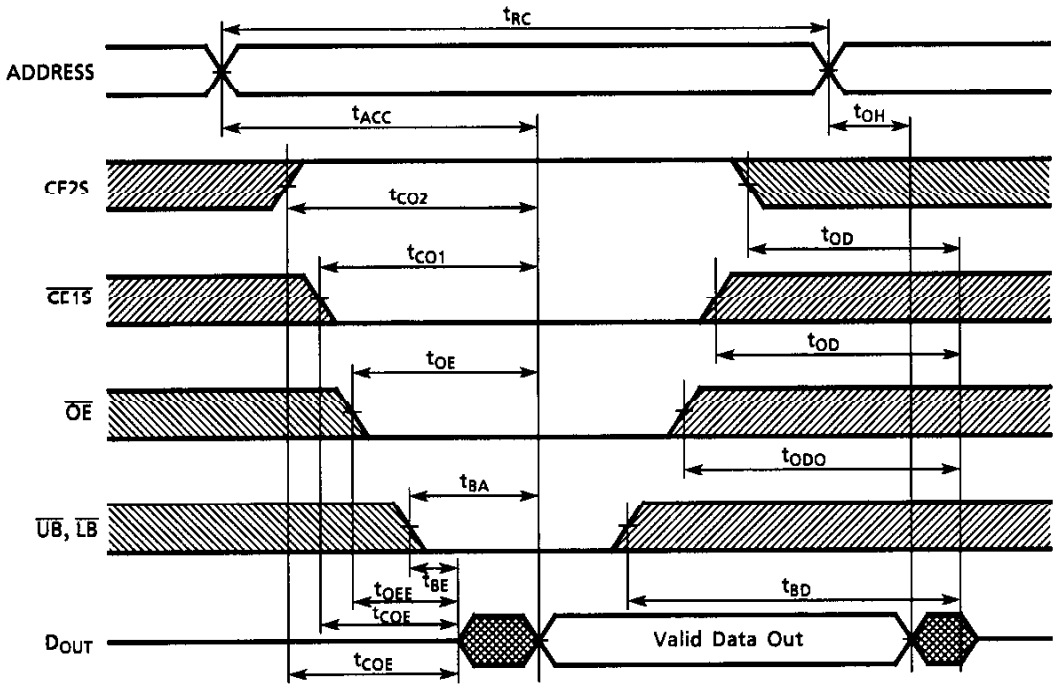
A command is not recognized on the rising edge of $\overline{WE}$ if V_{CCf} rises from 0 V to the operating voltage while $\overline{WE} = V_{IL}$, $CEF = V_{IL}$ and $\overline{OE} = V_{IH}$. In this case the device is reset and enters Read mode.

TIMING DIAGRAM

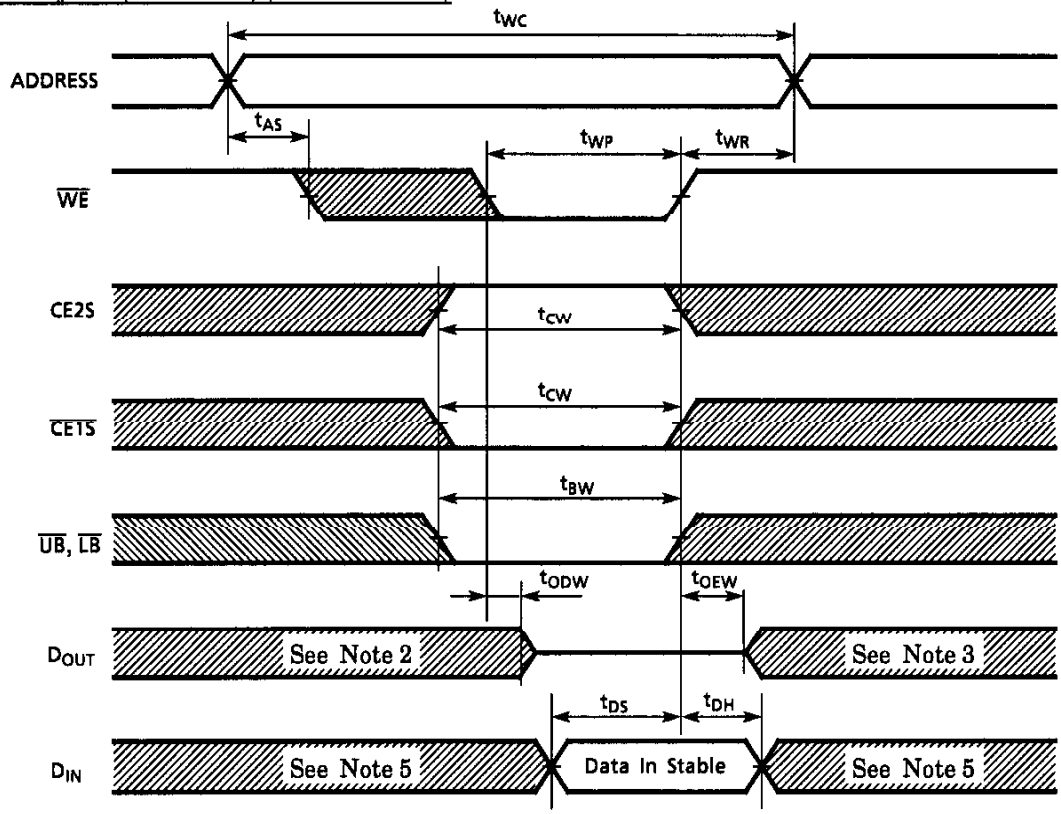
FLASH Read/ID Read Cycle



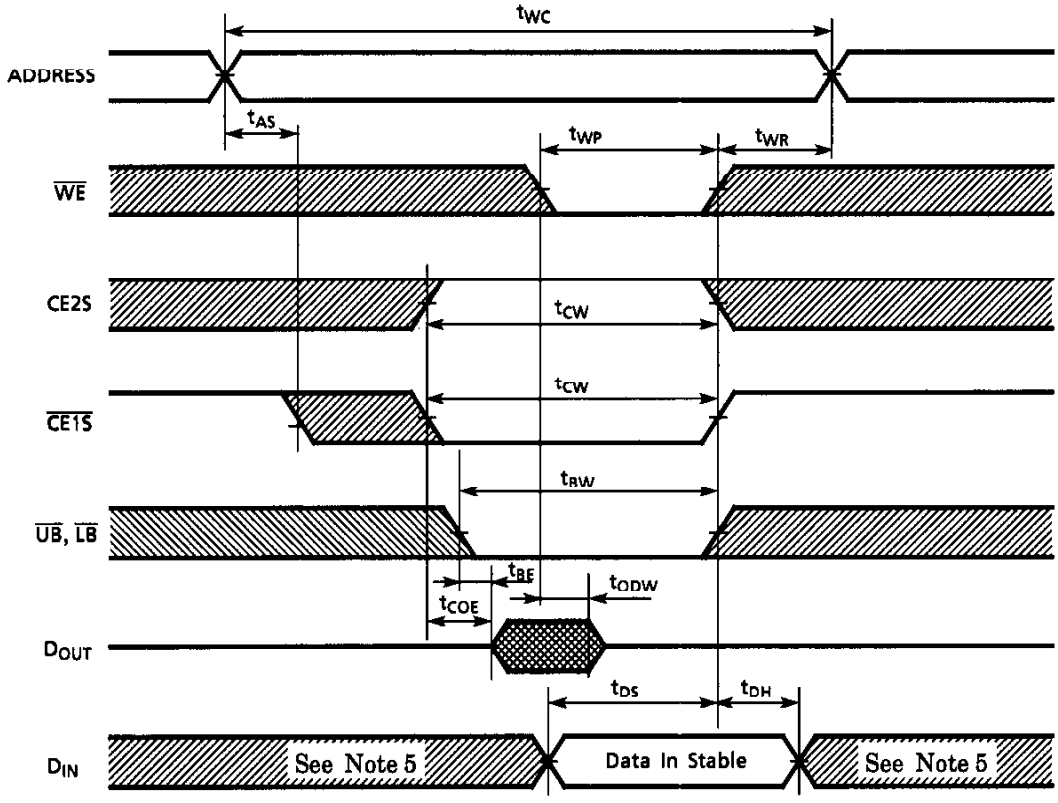
SRAM Read Cycle (See Note 1)



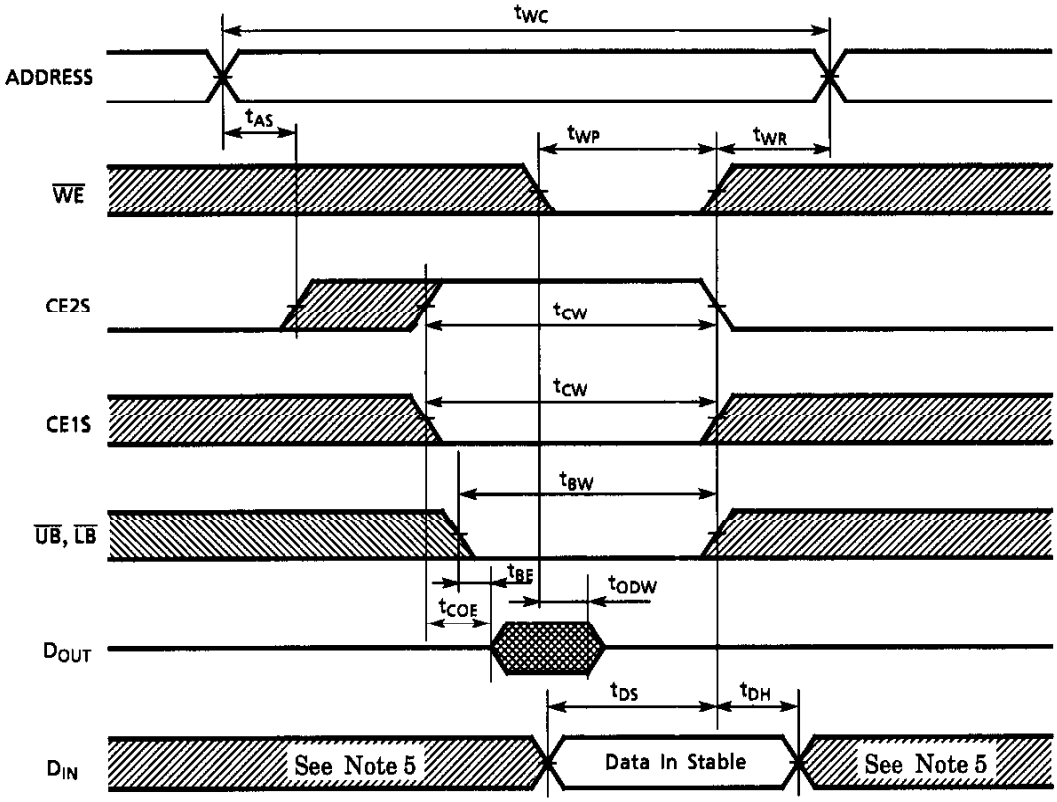
SRAM Write Cycle 1(See Note 4) ($\overline{WE}$ Controlled)



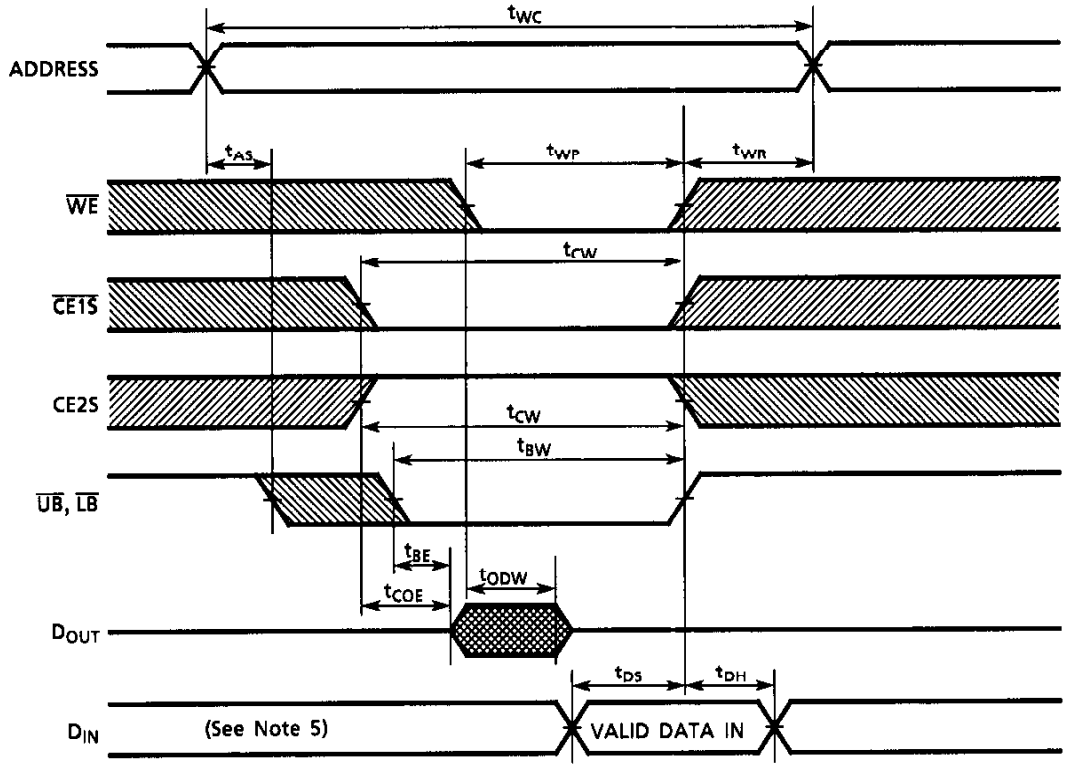
SRAM Write Cycle 2(See Note 4) ($\overline{CE1S}$ Controlled)



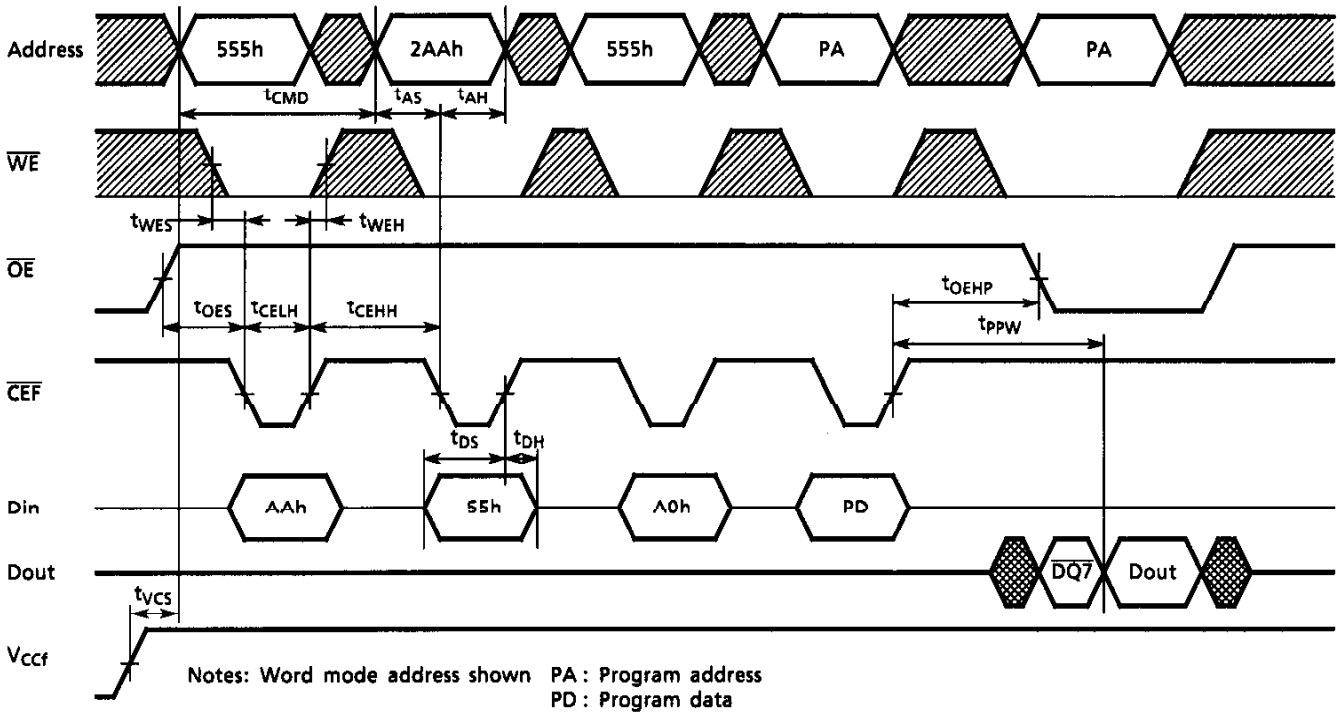
SRAM Write Cycle 3(See Note 4) (CE2S Controlled)



SRAM Write Cycle 4(See Note 4) ($\overline{UB}$, $\overline{LB}$ Controlled)

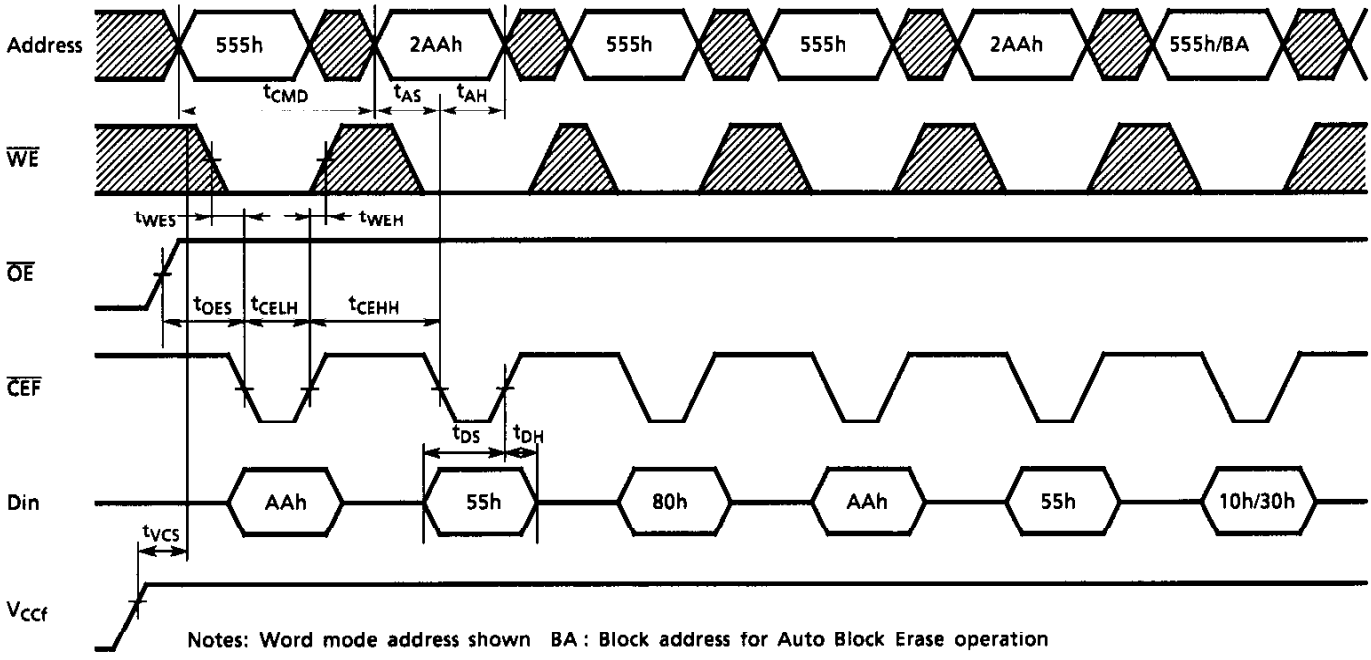


FLASH Auto Program Cycle ($\overline{CEF}$ Control)



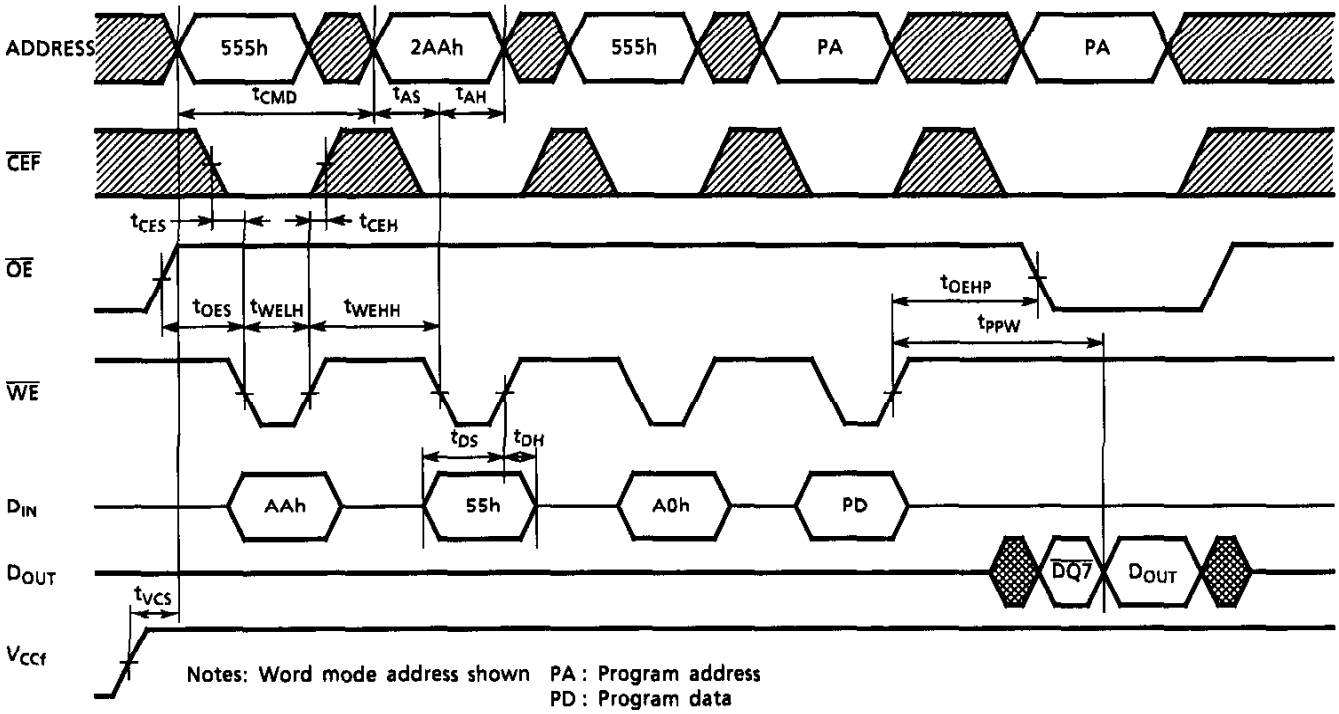
Notes: Word mode address shown PA : Program address
PD : Program data

FLASH Auto Chip Erase / Auto Block Erase Cycle ($\overline{CEF}$ Control)



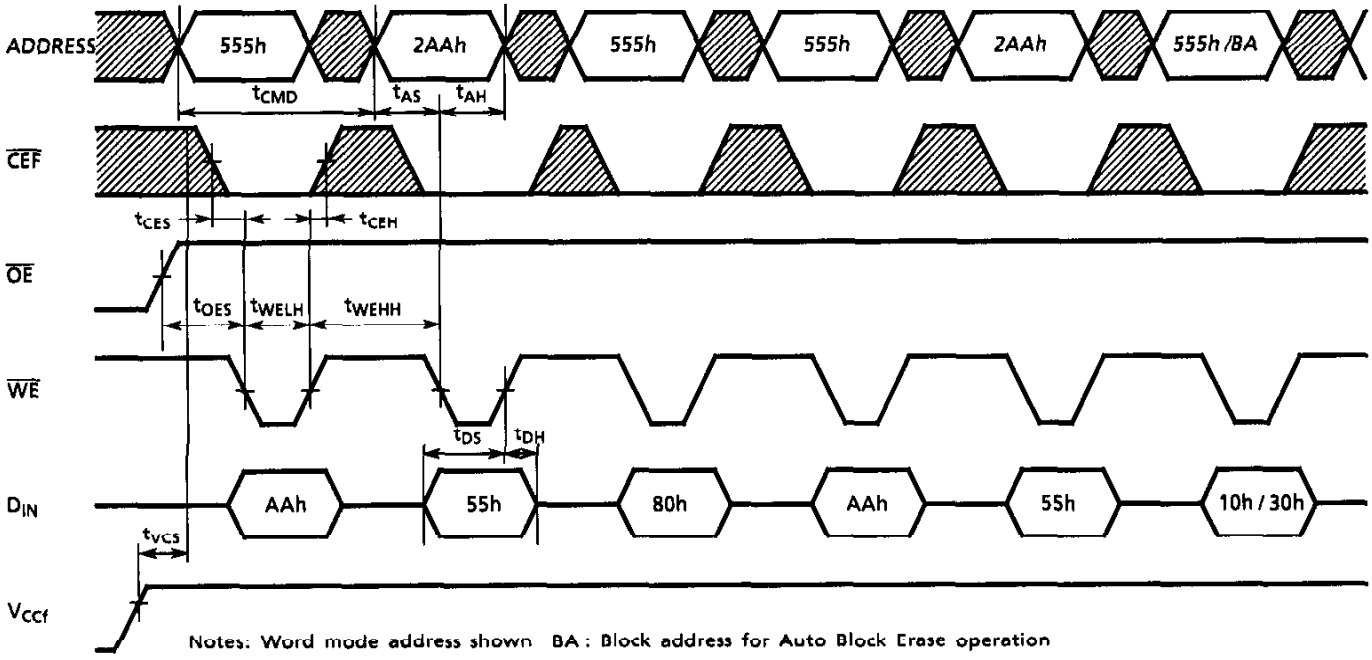
Notes: Word mode address shown BA : Block address for Auto Block Erase operation

FLASH Auto Program Cycle ($\overline{WE}$ Contorlled)



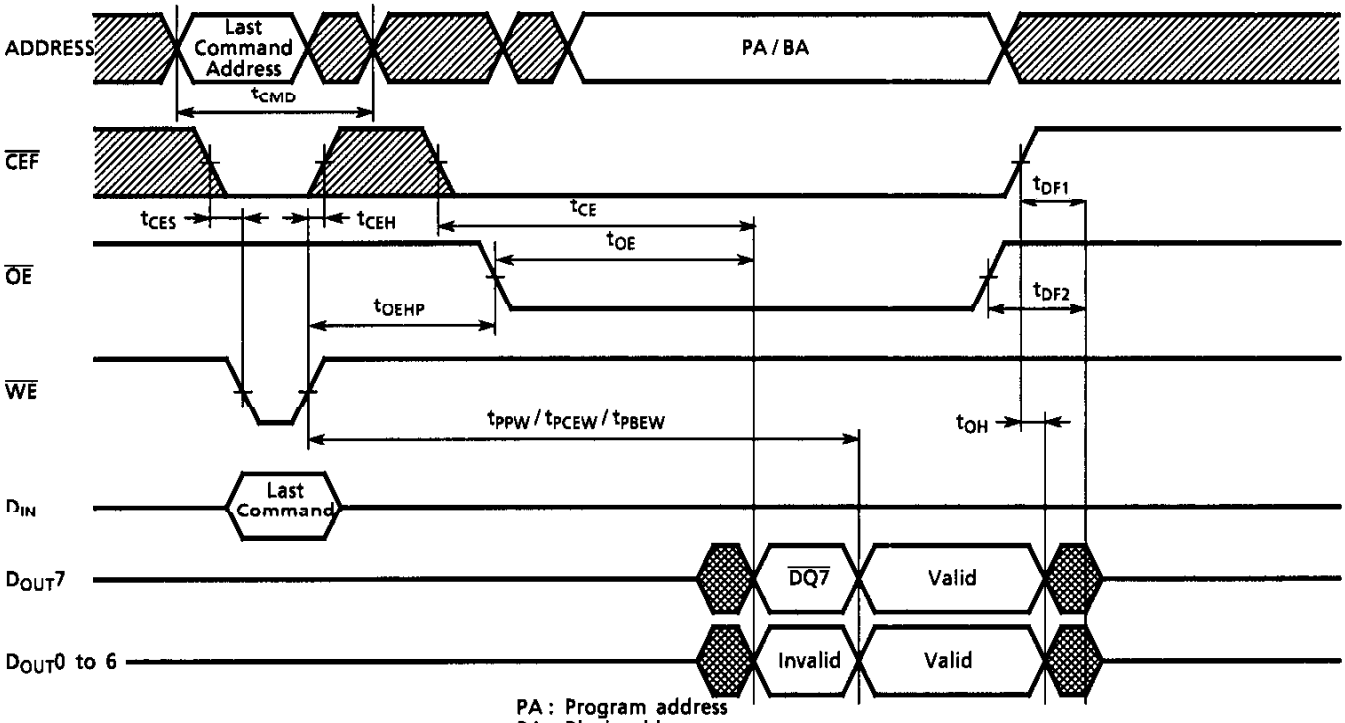
Notes: Word mode address shown PA : Program address
PD : Program data

FLASH Auto Chip Erase / Auto Block Erase Cycle ($\overline{WE}$ Controlled)



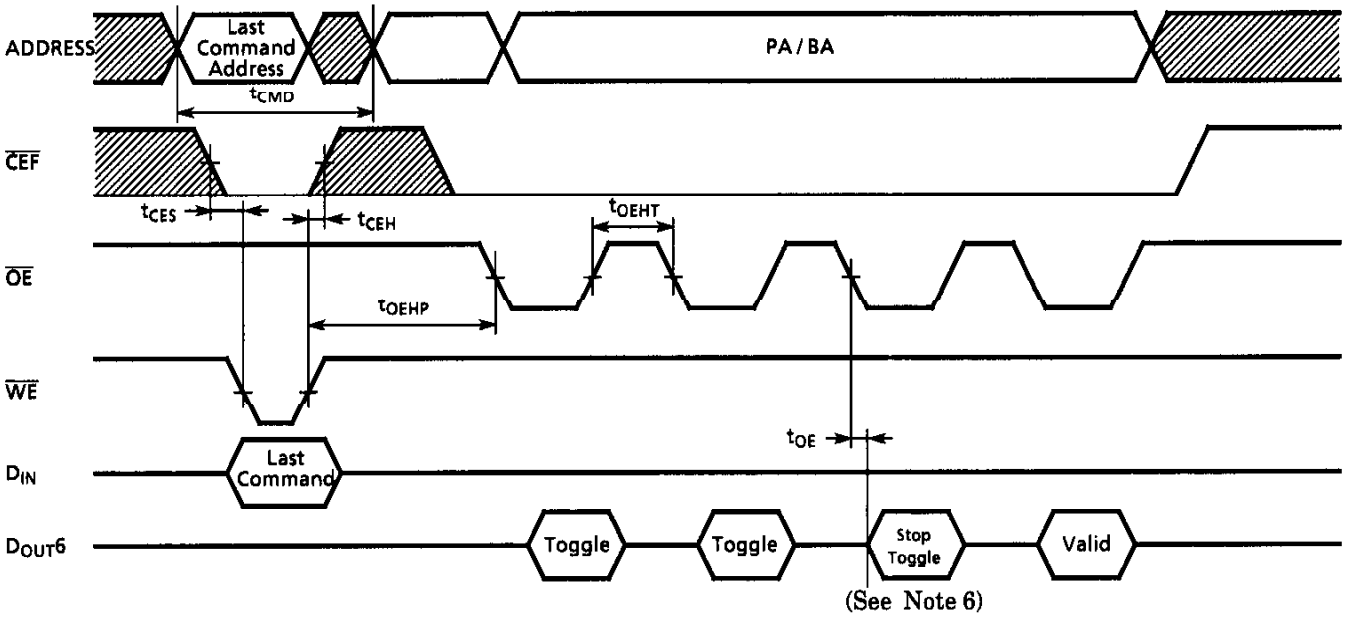
Notes: Word mode address shown BA : Block address for Auto Block Erase operation

FLASH $\overline{\text{DATA}}$ Polling during Program / Erase Cycle



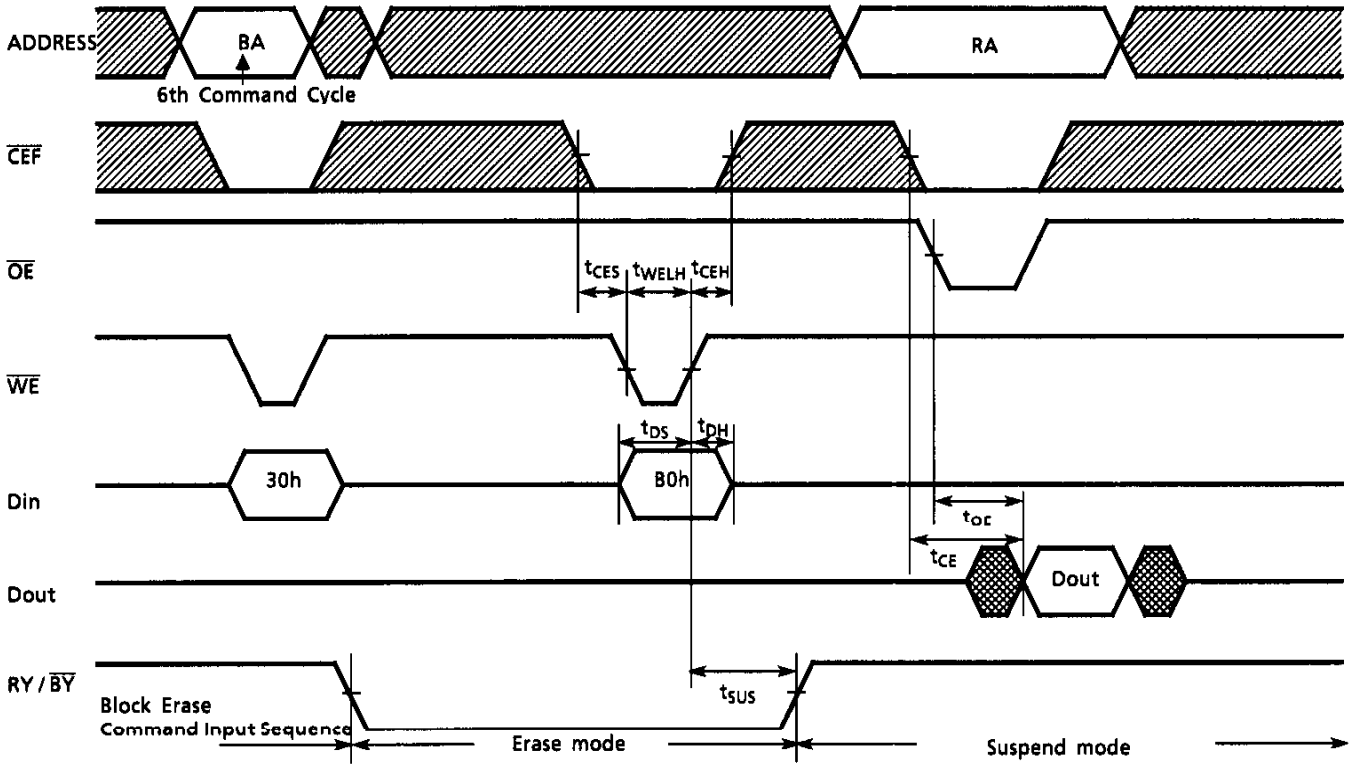
PA : Program address
BA : Block address

FLASH Toggle Bit during Program / Erase Cycle



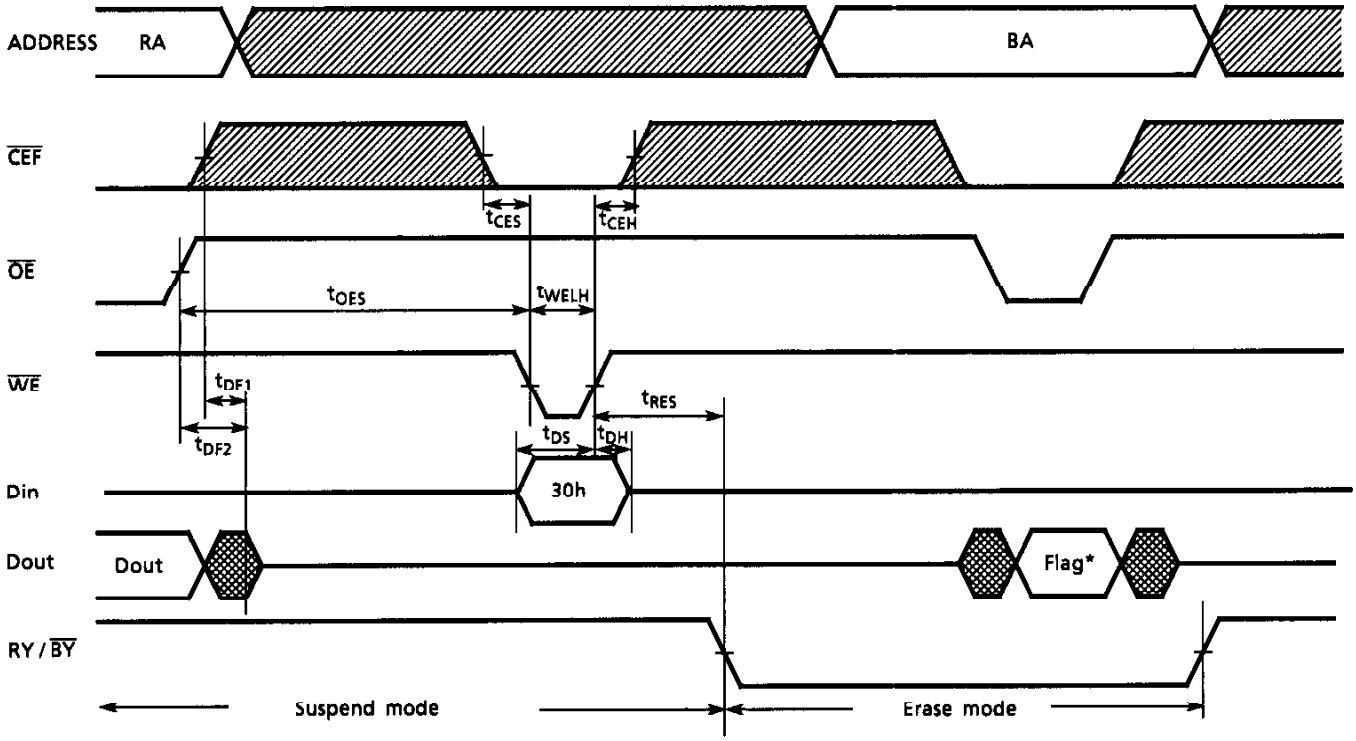
Notes: Word mode address shown PA : Program address
BA : Block address

FLASH ERASE SUSPEND OPERATION



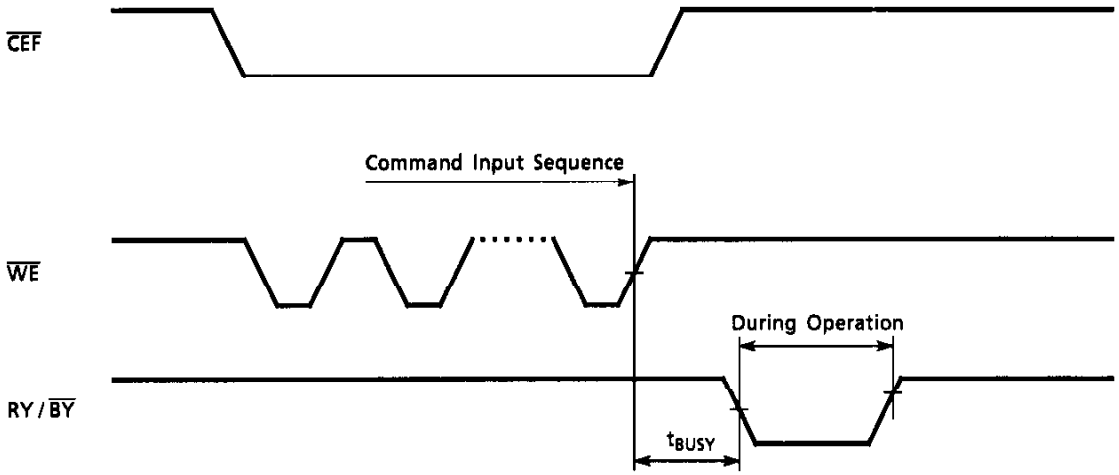
Notes : BA : Block address
RA : Read address

FLASH RESUME OPERATION

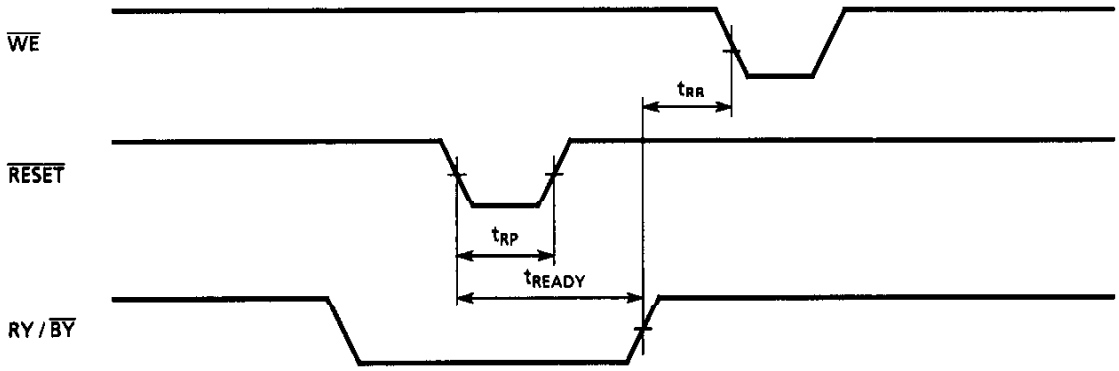


Notes : RA : Read address
BA : Block address
* Flag : Hardware sequence flag

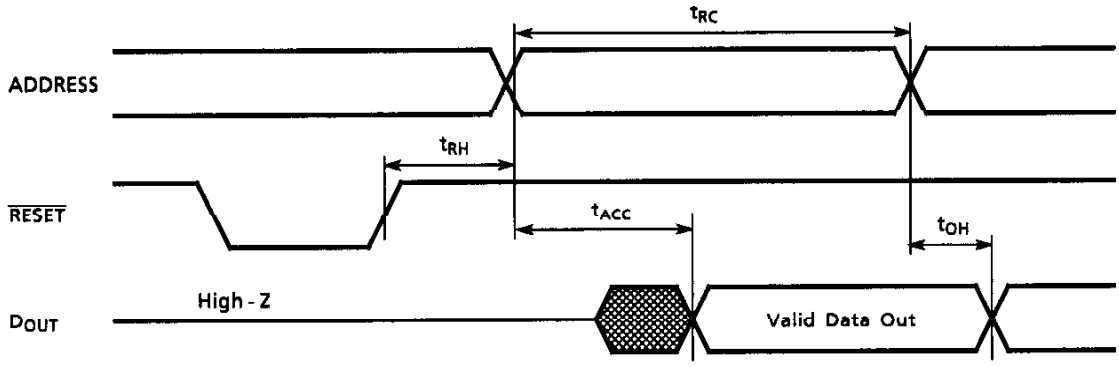
FLASH RY / $\overline{BY}$ during Auto Program / Erase Cycle



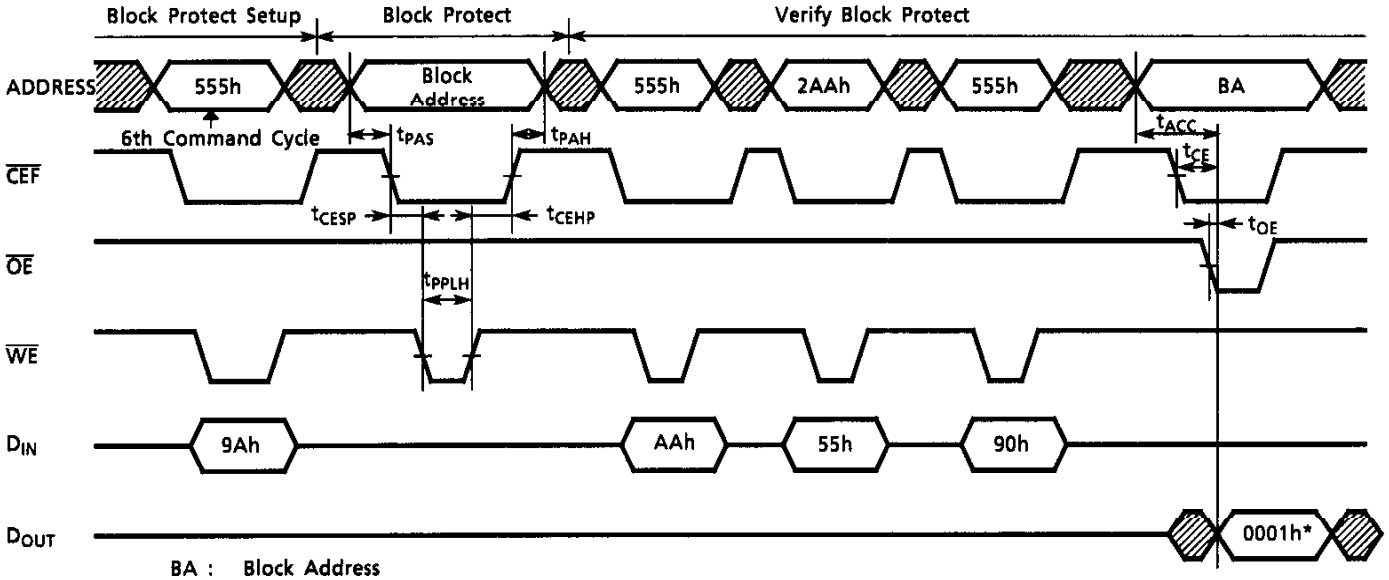
FLASH Hardware Reset Cycle



FLASH Read after $\overline{RESET}$



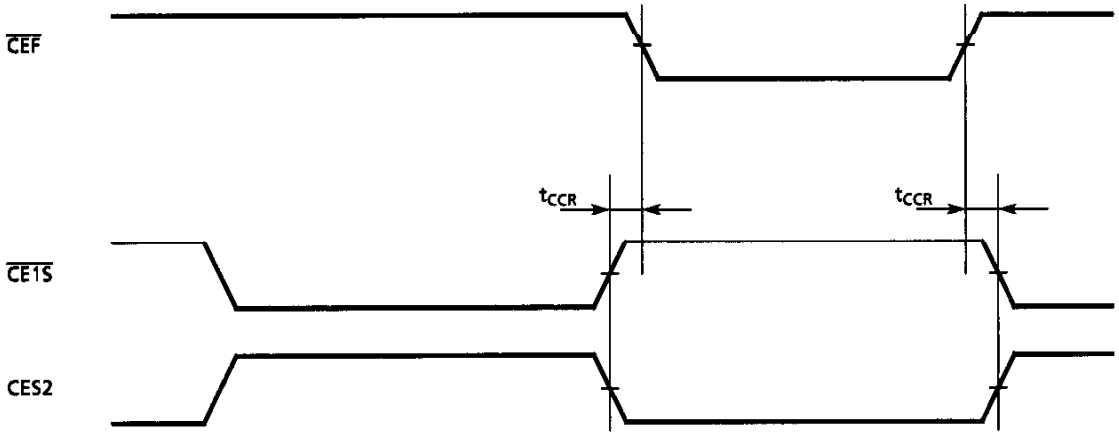
FLASH Block Protect Cycle (Software)



BA : Block Address

* : 0001h indicates that block is protected.

FLASH, SRAM Switching Timing



NOTE :

(1) $\overline{WE}$ remains HIGH for the read cycle.

(2) If $\overline{CE1S}$ goes LOW (or CE2S goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.

(3) If $\overline{CE1S}$ goes HIGH (or CE2S goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.

(4) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

(5) Because DQ signals may be in the output state at this time, input signals of reverse polarity must not be applied.

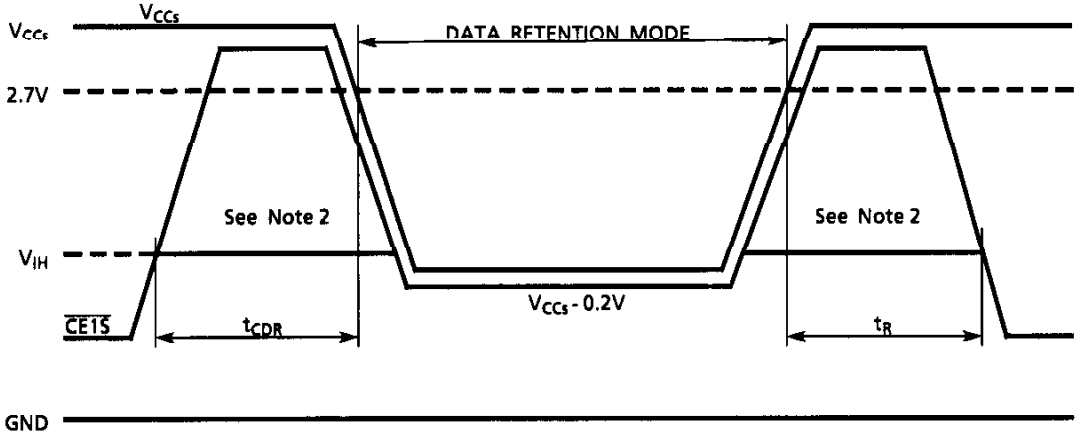
(6) $D_{OUT}6$ stop toggling when the last command has completed.

SRAM DATA RETENTION CHARACTERISTICS (Ta = −20° to 85°C)

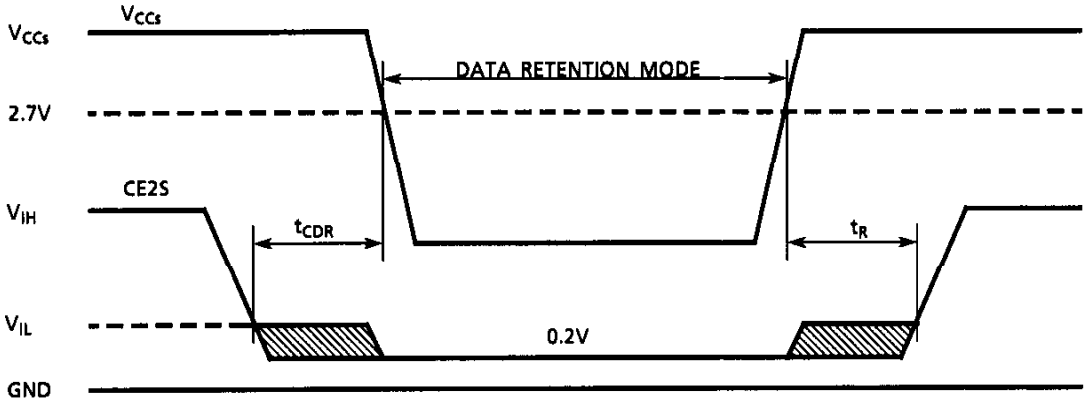
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{DH}	Data Retention Supply Voltage for SRAM		1.5	—	3.6	V
I_{CCS4}	SRAM Standby Current	V_{DH} = 3.0V	—	—	5	μA
		V_{DH} = 3.6V	—	—	7	
t_{CDR}	Chip Deselect to Data Retention Mode Time		0	—	—	nS
t_R	Recovery Time		t_{RC} (See Note)	—	—	nS

Note : Read cycle time

$\overline{CE1S}$ Controlled Data Retention Mode (See Note 1)



CE2S Controlled Data Retention Mode (See Note 3)



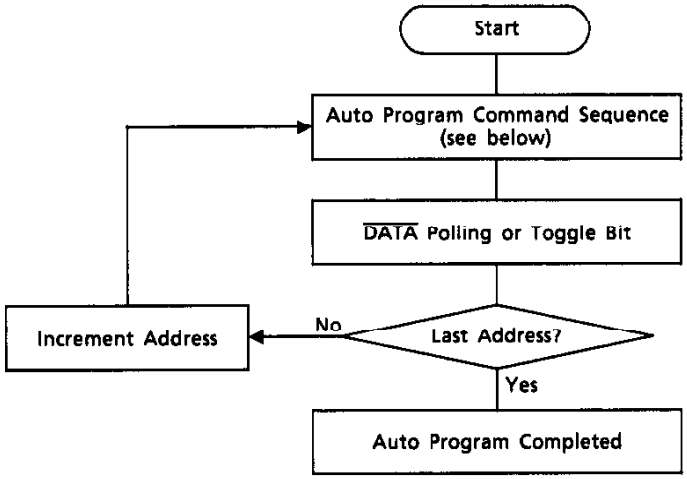
NOTE : 1) In $\overline{CE1S}$ controlled data retention mode, minimum standby current mode is entered when CE2S≦0.2V or CE2S≧V_{CCs}−0.2V.

2) When $\overline{CE1S}$ is operating at the V_{IH} level (2.2V), the SRAM standby current is given by I_{CCS3} during the transition of V_{CCs} from 3.6 to 2.4V.

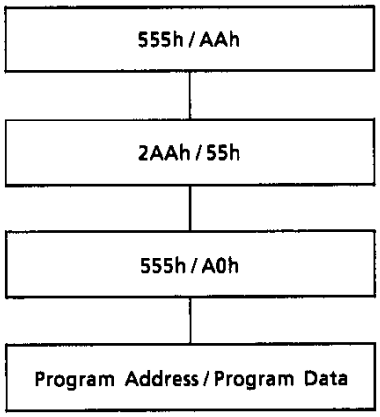
3) In CE2S controlled data retention mode, minimum standby current mode is entered when CE2S≦0.2V.

FLOW CHART for FLASH

Auto Program

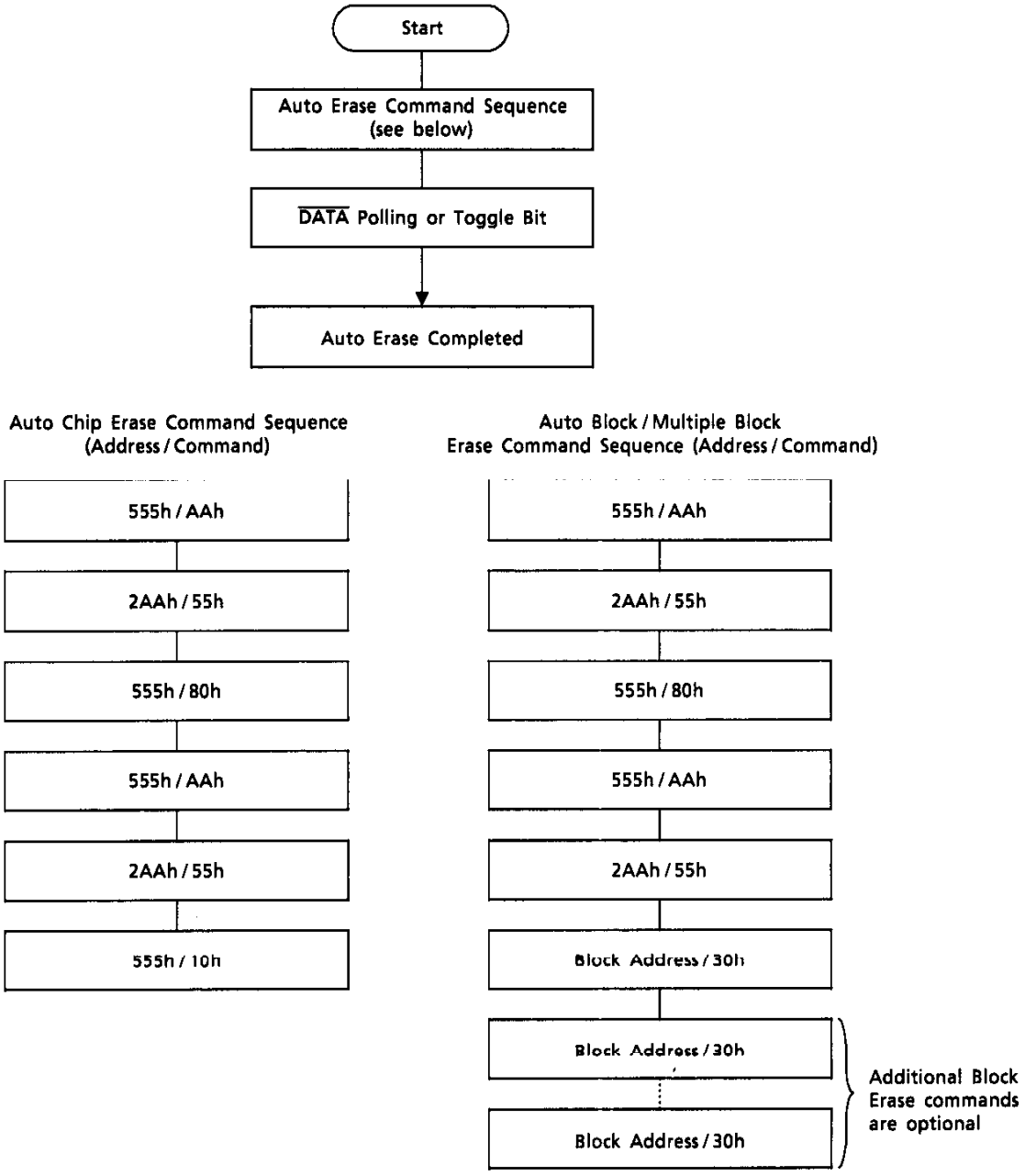


Auto Program Command Sequence (Address / Command)



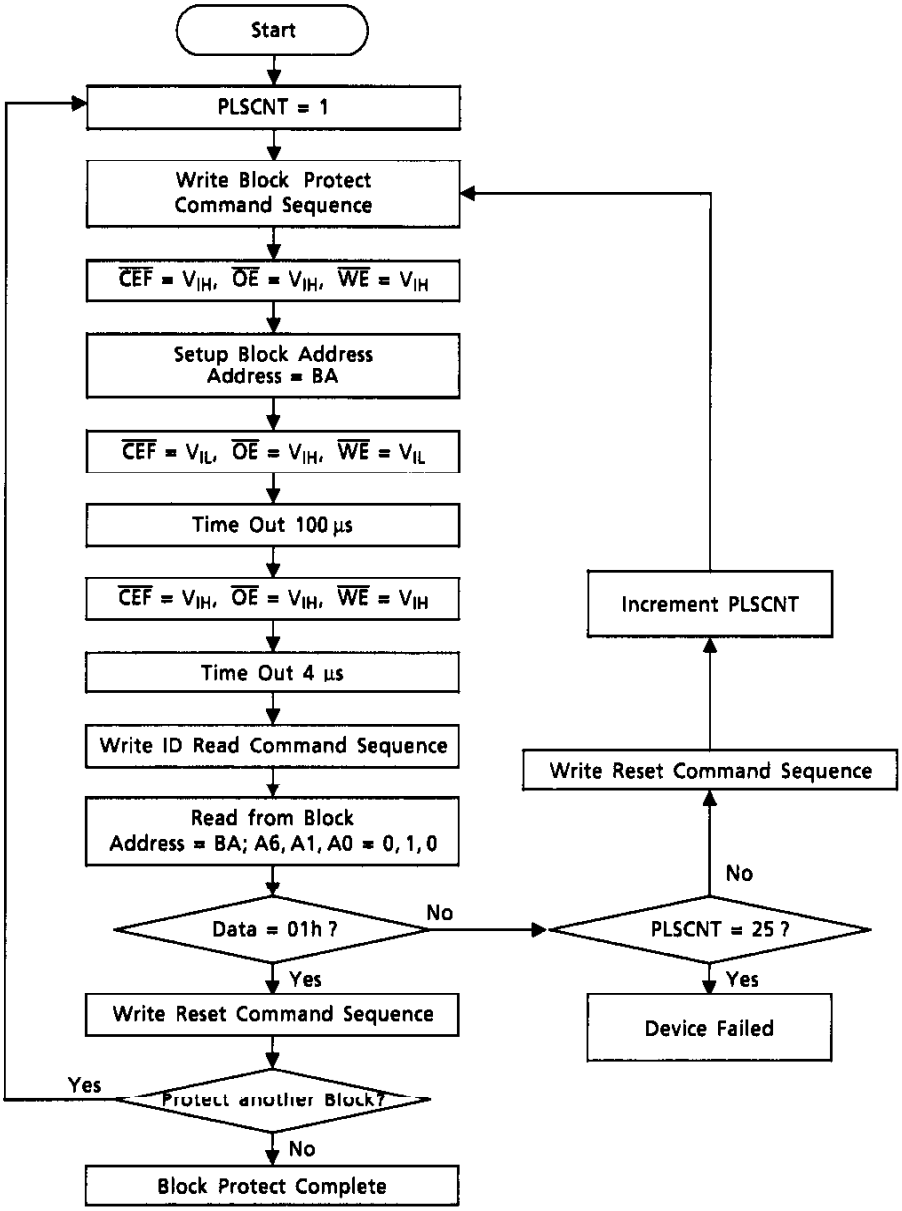
Note : Word mode command sequence is shown.

Auto Erase



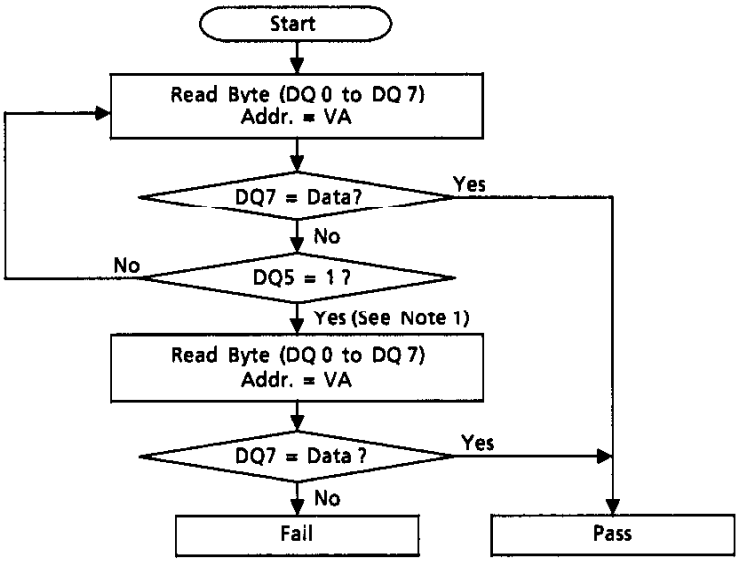
Note : Word mode command sequence is shown.

Block Protect (Software)



BA : Block Address

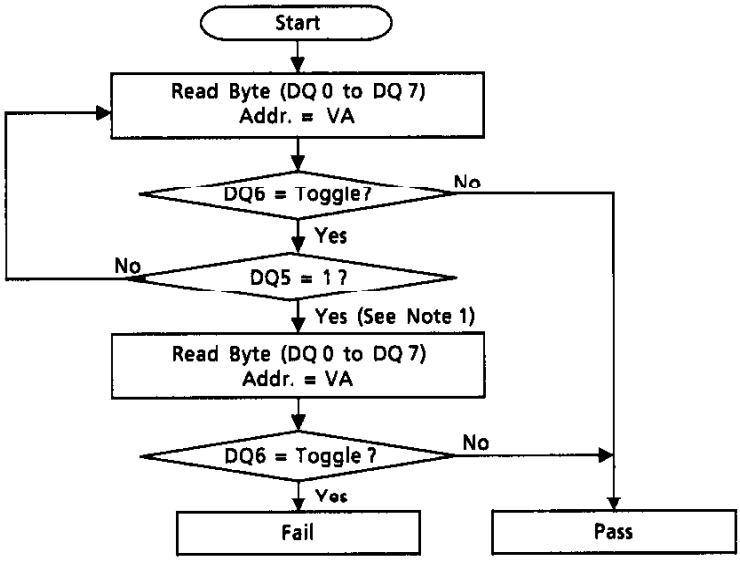
DQ 7 $\overline{\text{DATA}}$ Polling



VA : Byte address for programming.
Any of the addresses within the block being erased during a block erase operation.
Don't care during chip erase operation.

Note : 1) DQ7 must be rechecked even if DQ5 = "1" because DQ7 may change at the same time as DQ5.

DQ 6 Toggle Bit

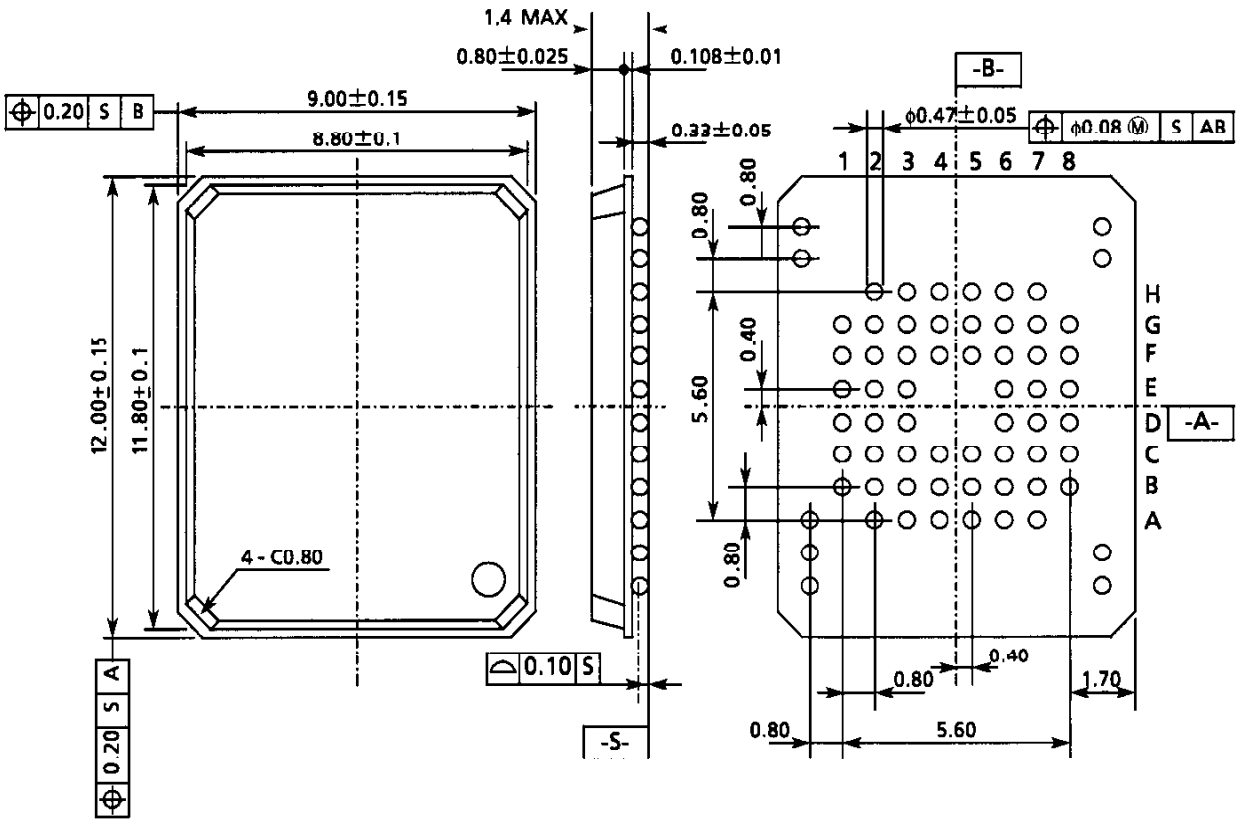


VA : Byte address for programming.
Any of the addresses within the block being erased during a block erase operation.
Don't care during chip erase operation.
Any address not within the current block during an Erase Suspend operation.

Note : 1) DQ 6 must be rechecked even if DQ 5 = "1" because DQ 6 may stop toggling at the same time that DQ 5 changes to "1".

OUTLINE DRAWING (P-LFBGA65-1209-0.80A3) TENTATIVE

Unit in mm



Weight: 0.31g (typ)

NOTE

1. All Dimensions are mm.
2. Unless otherwide specified all tolerance are ±0.05mm.