

MOSFET – Power, N-Channel, DPAK

20 A, 60 V

NTD20N06, NTDV20N06

Description

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

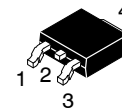
Features

- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Lower and Tighter V_{SD}
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge
- NTDV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

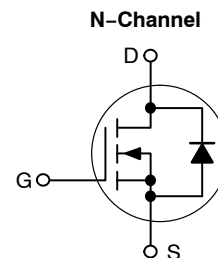
Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

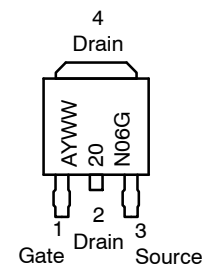
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
60 V	37.5 mΩ	20 A



**DPAK
CASE 369C
STYLE 2**



MARKING DIAGRAM & PIN ASSIGNMENTS



A = Assembly Location*
 20N06 = Device Code
 Y = Year
 WW = Work Week
 G = Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 8.

NTD20N06, NTDV20N06

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Rating	Value	Unit
V_{DSS}	Drain-to-Source Voltage	60	Vdc
V_{DGR}	Drain-to-Gate Voltage ($R_{GS} = 10\text{ M}\Omega$)	60	Vdc
V_{GS} V_{GS}	Gate-to-Source Voltage – Continuous – Non-repetitive ($t_p \leq 10\text{ ms}$)	± 20 ± 30	Vdc
I_D I_D I_{DM}	Drain Current – Continuous @ $T_A = 25^\circ\text{C}$ – Continuous @ $T_A = 100^\circ\text{C}$ – Single Pulse ($t_p \leq 10\text{ }\mu\text{s}$)	20 10 60	Adc Apk
P_D	Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2)	60 0.40 1.88 1.36	W W/ $^\circ\text{C}$ W W
T_J, T_{stg}	Operating and Storage Temperature Range	-55 to 175	$^\circ\text{C}$
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 25\text{ Vdc}$, $V_{GS} = 10\text{ Vdc}$, $L = 1.0\text{ mH}$, $I_L(\text{pk}) = 18.4\text{ A}$, $V_{DS} = 60\text{ Vdc}$)	170	mJ
$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	Thermal Resistance – Junction-to-Case – Junction-to-Ambient (Note 1) – Junction-to-Ambient (Note 2)	2.5 80 110	$^\circ\text{C/W}$
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. When surface mounted to an FR4 board using the 0.5 sq in drain pad size.

NTD20N06, NTDV20N06

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	60 –	71.7 79.4	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	±100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	2.0 –	2.91 6.9	4.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 10 Vdc, I _D = 10 Adc)	R _{DS(on)}	–	37.5	46	mΩ
Static Drain-to-Source On-Voltage (Note 3) (V _{GS} = 10 Vdc, I _D = 20 Adc) (V _{GS} = 10 Vdc, I _D = 10 Adc, T _J = 150°C)	V _{DS(on)}	– –	0.78 1.57	1.10 –	Vdc
Forward Transconductance (Note 3) (V _{DS} = 7.0 Vdc, I _D = 6.0 Adc)	g _{FS}	–	13.2	–	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	725	1015	pF
Output Capacitance		C _{oss}	–	213	300	
Transfer Capacitance		C _{rss}	–	58	120	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{DD} = 30 Vdc, I _D = 20 Adc, V _{GS} = 10 Vdc, R _G = 9.1 Ω) (Note 3)	t _{d(on)}	–	9.5	20	ns
Rise Time		t _r	–	60.5	120	
Turn-Off Delay Time		t _{d(off)}	–	27.1	60	
Fall Time		t _f	–	37.1	80	
Gate Charge	(V _{DS} = 48 Vdc, I _D = 20 Adc, V _{GS} = 10 Vdc) (Note 3)	Q _T	–	21.2	30	nC
		Q ₁	–	5.6	–	
		Q ₂	–	7.3	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 20 Adc, V _{GS} = 0 Vdc) (Note 3) (I _S = 20 Adc, V _{GS} = 0 Vdc, T _J = 150°C)	V _{SD}	– –	1.0 0.87	1.2 –	Vdc
Reverse Recovery Time	(I _S = 20 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs) (Note 3)	t _{rr}	–	42.9	–	ns
		t _a	–	33	–	
		t _b	–	9.9	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.084	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

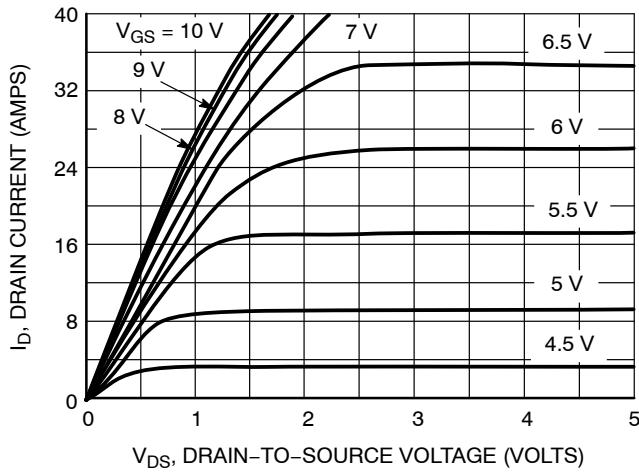


Figure 1. On-Region Characteristics

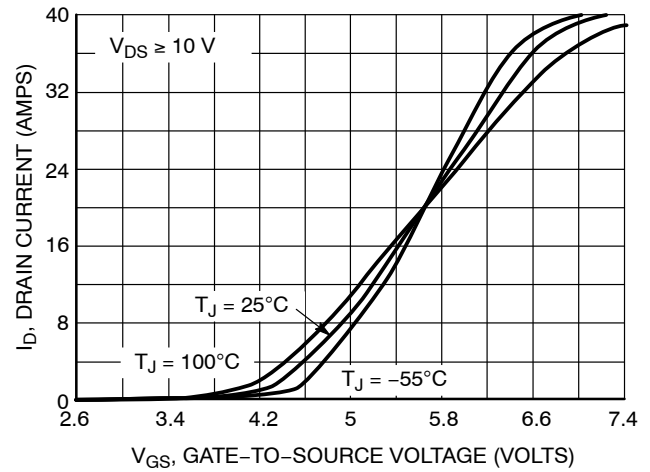


Figure 2. Transfer Characteristics

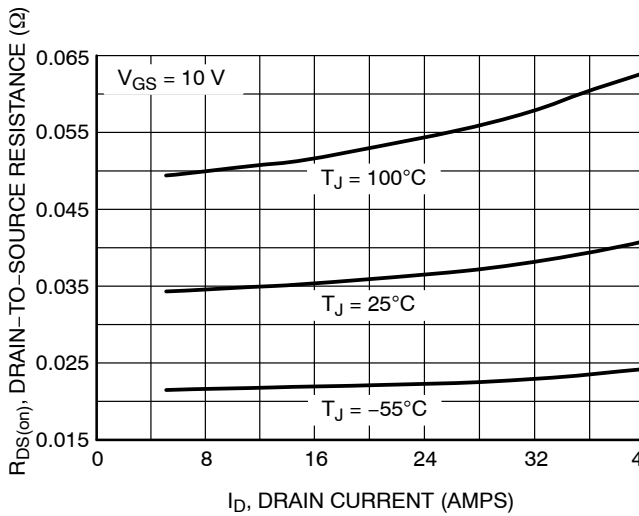


Figure 3. On-Resistance versus Gate-to-Source Voltage

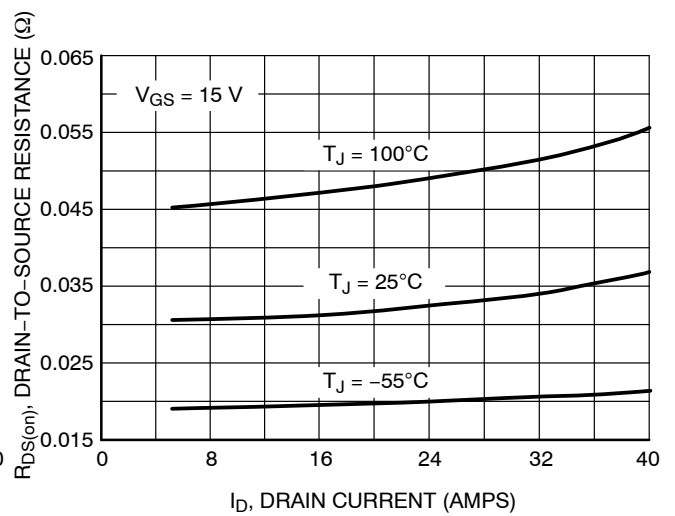


Figure 4. On-Resistance versus Drain Current and Gate Voltage

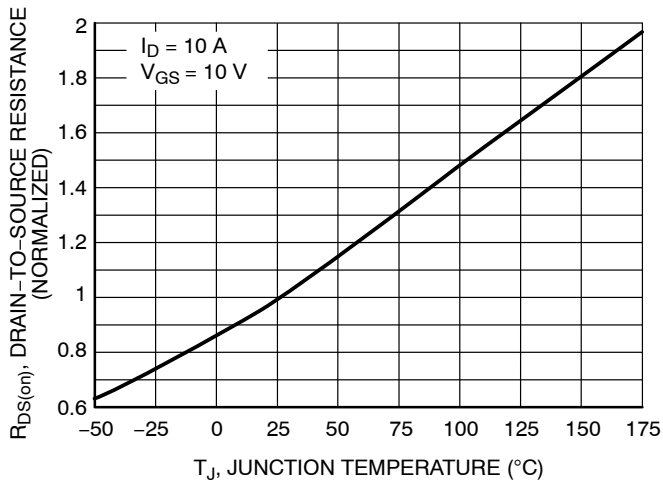


Figure 5. On-Resistance Variation with Temperature

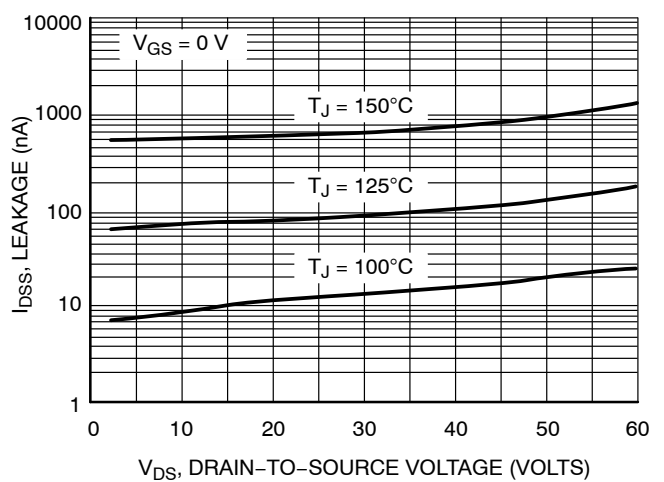


Figure 6. Drain-to-Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP} . Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G / (V_{GG} - V_{SGP})$$

$$t_f = Q_2 \times R_G / V_{SGP}$$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{SGP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{SGP})]$$

$$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{SGP})$$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by $L di/dt$, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

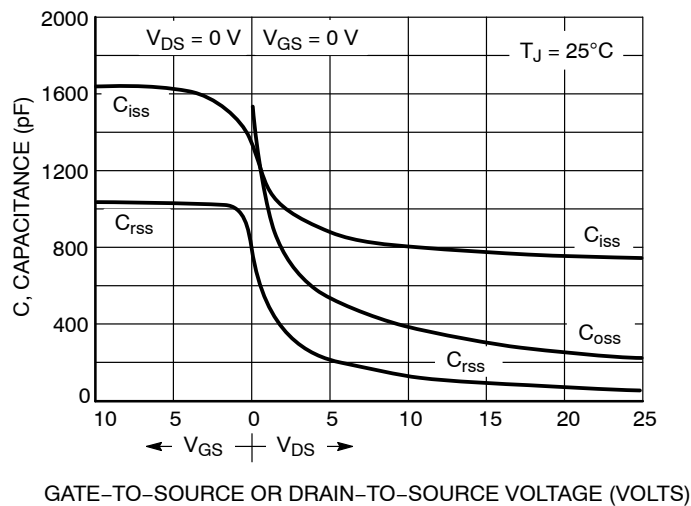


Figure 7. Capacitance Variation

NTD20N06, NTDV20N06

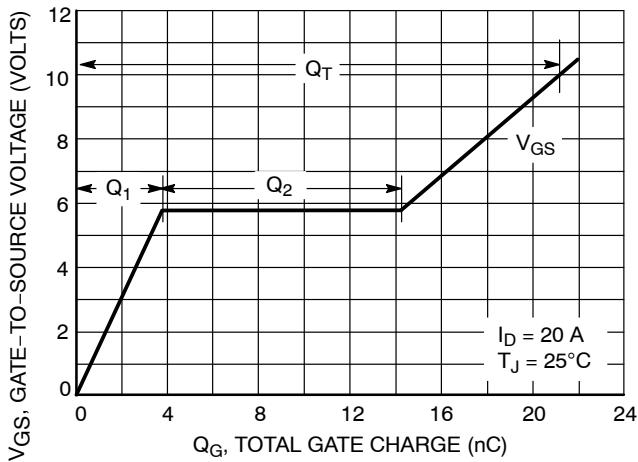


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

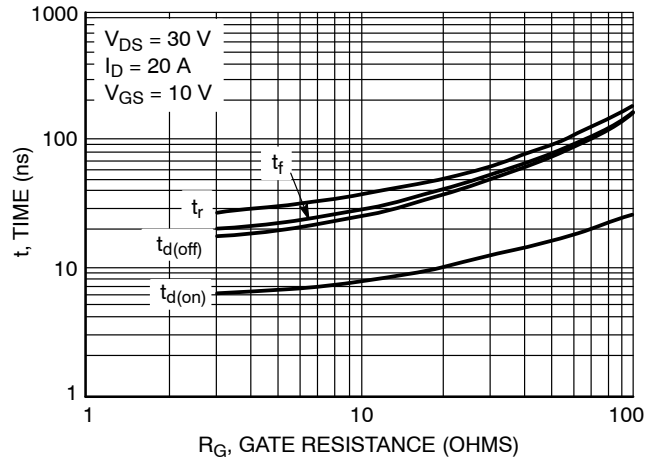


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN-TO-SOURCE DIODE CHARACTERISTICS

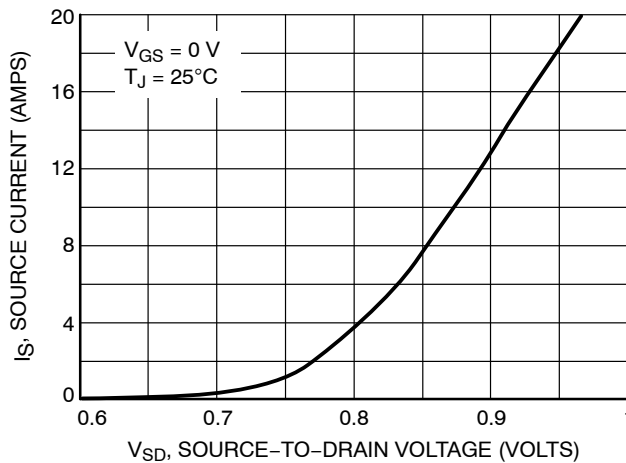


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain-to-source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off-state and the on-state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_b, t_f) do not exceed 10 μ s. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E-FET can be safely used in switching circuits with unclamped inductive loads. For

reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non-linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E-FETs can withstand the stress of drain-to-source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

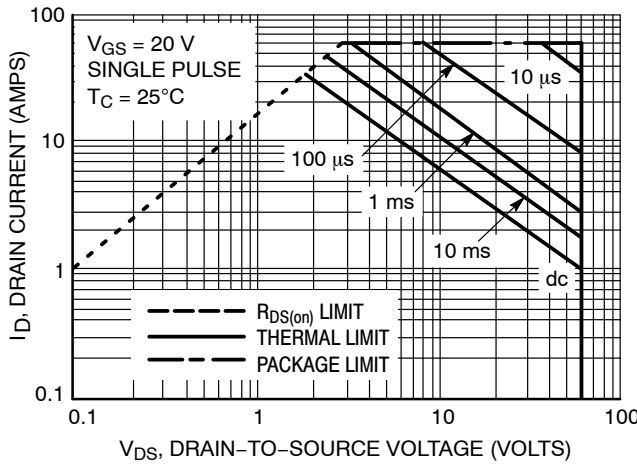


Figure 11. Maximum Rated Forward Biased Safe Operating Area

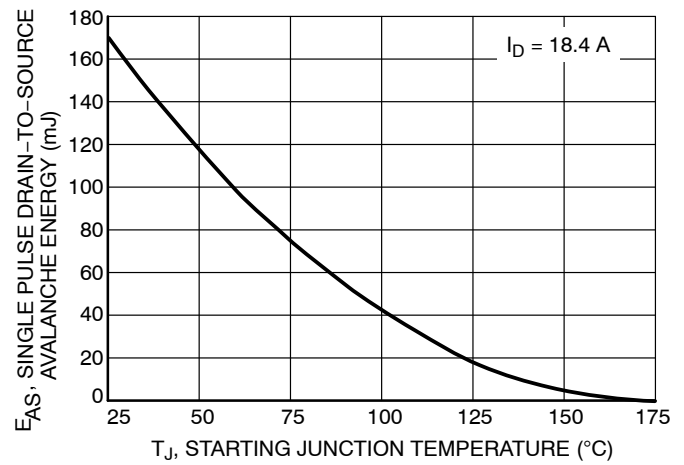


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

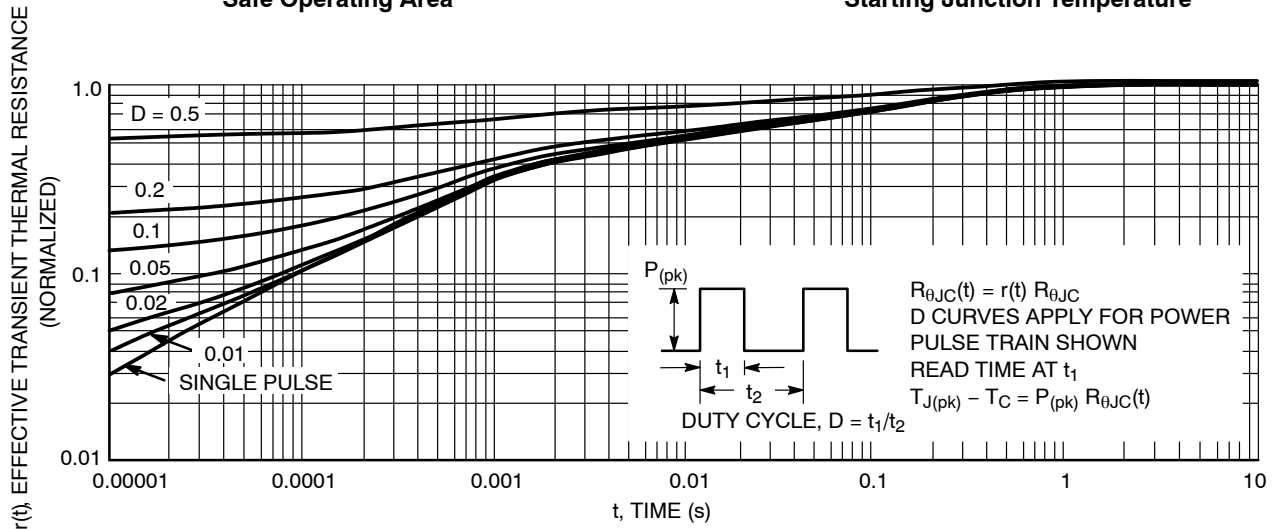


Figure 13. Thermal Response

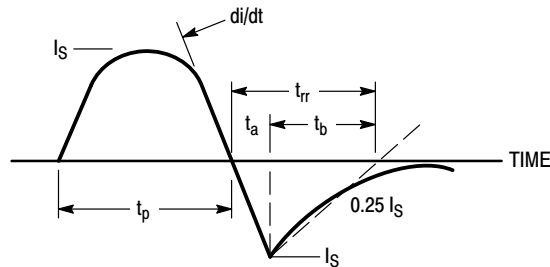


Figure 14. Diode Reverse Recovery Waveform

NTD20N06, NTDV20N06

ORDERING INFORMATION

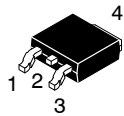
Device	Package	Shipping [†]
NTD20N06T4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTDV20N06T4G-VF01		

DISCONTINUED (Note 5)

NTDV20N06T4G	DPAK (Pb-Free)	2500 / Tape & Reel
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[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

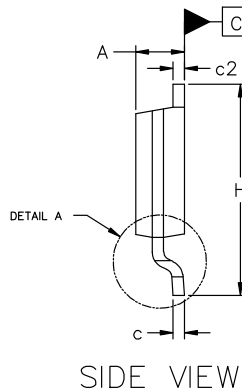
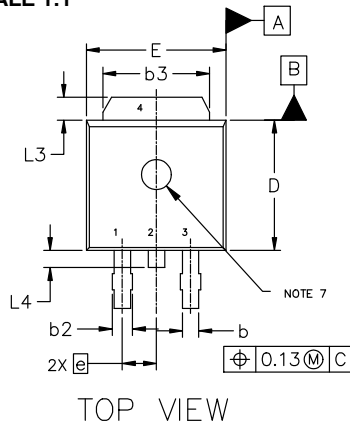
5. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.



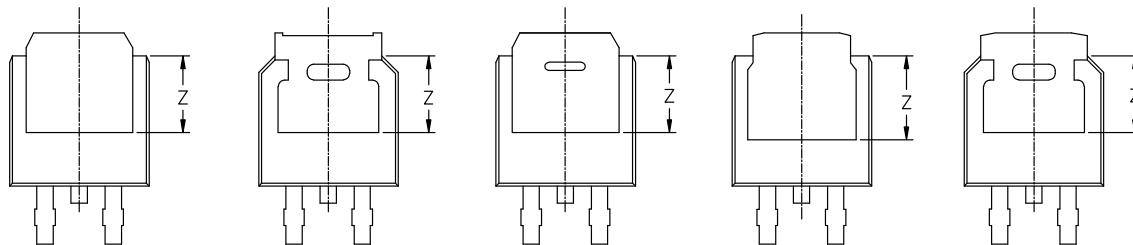
DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

SCALE 1:1

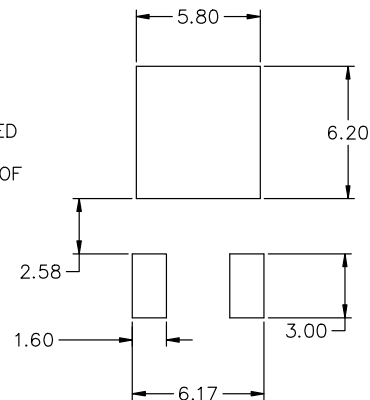
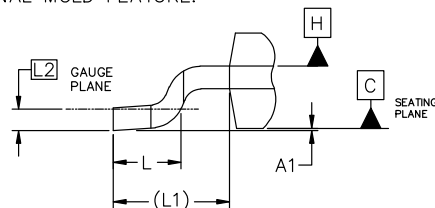


MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

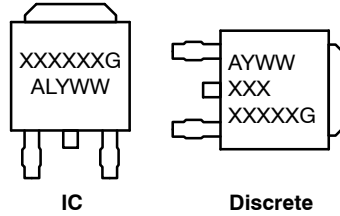
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DESCRIPTION:	DPAK3 6.10x6.54x2.28, 2.29P	PAGE 1 OF 2

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DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

**GENERIC
MARKING DIAGRAM***



XXXXXX = Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE	STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE
STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2	STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE	STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE	STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE

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DESCRIPTION:	DPAK3 6.10x6.54x2.28, 2.29P	PAGE 2 OF 2

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