

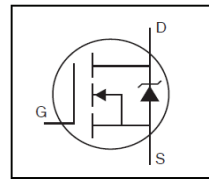
HEXFET® Power MOSFET

**Features**

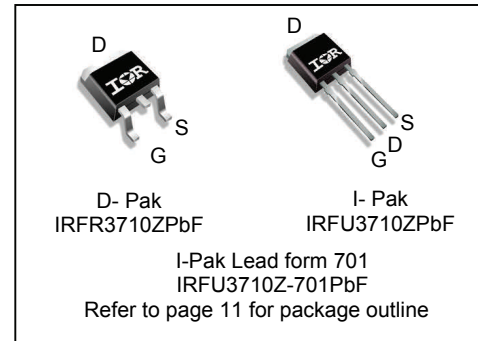
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to  $T_{jmax}$
- Multiple Package Options
- Lead-Free

**Description**

This HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.



|              |             |
|--------------|-------------|
| $V_{DS}$     | <b>100V</b> |
| $R_{DS(on)}$ | <b>18mΩ</b> |
| $I_D$        | <b>42A</b>  |



|          |          |          |
|----------|----------|----------|
| <b>G</b> | <b>D</b> | <b>S</b> |
| Gate     | Drain    | Source   |

| Base part number | Package Type | Standard Pack      |          | Orderable Part Number |
|------------------|--------------|--------------------|----------|-----------------------|
|                  |              | Form               | Quantity |                       |
| IRFU3710ZPbF     | I-Pak        | Tube               | 75       | IRFU3710ZPbF          |
| IRFR3710ZPbF     | D-Pak        | Tube               | 75       | IRFR3710ZPbF          |
|                  |              | Tape and Reel Left | 3000     | IRFR3710ZTRLpbf       |

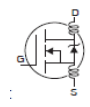
**Absolute Maximum Ratings**

| Symbol                          | Parameter                                                         | Max.                     | Units |
|---------------------------------|-------------------------------------------------------------------|--------------------------|-------|
| $I_D @ T_C = 25^\circ\text{C}$  | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited) | 56                       | A     |
| $I_D @ T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$                   | 39                       |       |
| $I_D @ T_C = 25^\circ\text{C}$  | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited) | 42                       |       |
| $I_{DM}$                        | Pulsed Drain Current ①                                            | 220                      |       |
| $P_D @ T_C = 25^\circ\text{C}$  | Maximum Power Dissipation                                         | 140                      | W     |
|                                 | Linear Derating Factor                                            | 0.95                     | W/°C  |
| $V_{GS}$                        | Gate-to-Source Voltage                                            | $\pm 20$                 | V     |
| $E_{AS}$ (Thermally limited)    | Single Pulse Avalanche Energy②                                    | 150                      | mJ    |
| $E_{AS}$ (Tested )              | Single Pulse Avalanche Energy Tested Value⑥                       | 200                      |       |
| $I_{AR}$                        | Avalanche Current①                                                | See Fig.12a, 12b, 15, 16 | A     |
| $E_{AR}$                        | Repetitive Avalanche Energy ⑤                                     |                          | mJ    |
| $T_J$                           | Operating Junction and                                            | -55 to + 175             | °C    |
| $T_{STG}$                       | Storage Temperature Range                                         |                          |       |
|                                 | Soldering Temperature, for 10 seconds (1.6mm from case)           | 300                      |       |

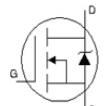
**Thermal Resistance**

| Symbol          | Parameter                          | Typ. | Max. | Units |
|-----------------|------------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case                   | —    | 1.05 | °C/W  |
| $R_{\theta JA}$ | Junction-to-Ambient ( PCB Mount) ② | —    | 50   |       |
| $R_{\theta JA}$ | Junction-to-Ambient                | —    | 110  |       |

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

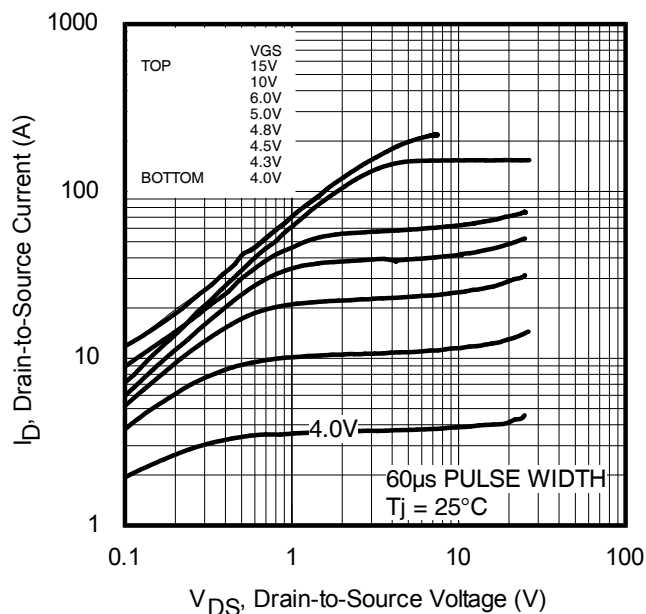
|                                 | Parameter                            | Min. | Typ.  | Max. | Units               | Conditions                                                                                                                                             |
|---------------------------------|--------------------------------------|------|-------|------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| $V_{(BR)DSS}$                   | Drain-to-Source Breakdown Voltage    | 100  | —     | —    | V                   | $V_{GS} = 0V, I_D = 250\mu A$                                                                                                                          |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient  | —    | 0.088 | —    | V/ $^\circ\text{C}$ | Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$                                                                                                   |
| $R_{DS(on)}$                    | Static Drain-to-Source On-Resistance | —    | 15    | 18   | m $\Omega$          | $V_{GS} = 10V, I_D = 33A$ ③                                                                                                                            |
| $V_{GS(th)}$                    | Gate Threshold Voltage               | 2.0  | —     | 4.0  | V                   | $V_{DS} = V_{GS}, I_D = 250\mu A$                                                                                                                      |
| $g_{fs}$                        | Forward Trans conductance            | 39   | —     | —    | S                   | $V_{DS} = 25V, I_D = 33A$                                                                                                                              |
| $I_{DSS}$                       | Drain-to-Source Leakage Current      | —    | —     | 20   | $\mu A$             | $V_{DS} = 100V, V_{GS} = 0V$                                                                                                                           |
|                                 |                                      | —    | —     | 250  |                     | $V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$                                                                                                  |
| $I_{GSS}$                       | Gate-to-Source Forward Leakage       | —    | —     | 200  | nA                  | $V_{GS} = 20V$                                                                                                                                         |
|                                 | Gate-to-Source Reverse Leakage       | —    | —     | -200 |                     | $V_{GS} = -20V$                                                                                                                                        |
| $Q_g$                           | Total Gate Charge                    | —    | 69    | 100  | nC                  | $I_D = 33A$                                                                                                                                            |
| $Q_{gs}$                        | Gate-to-Source Charge                | —    | 15    | —    |                     | $V_{DS} = 80V$                                                                                                                                         |
| $Q_{gd}$                        | Gate-to-Drain ('Miller') Charge      | —    | 25    | —    |                     | $V_{GS} = 10V$ ③                                                                                                                                       |
| $t_{d(on)}$                     | Turn-On Delay Time                   | —    | 14    | —    | ns                  | $V_{DD} = 50V$                                                                                                                                         |
| $t_r$                           | Rise Time                            | —    | 43    | —    |                     | $I_D = 33A$                                                                                                                                            |
| $t_{d(off)}$                    | Turn-Off Delay Time                  | —    | 53    | —    |                     | $R_G = 6.8\Omega$                                                                                                                                      |
| $t_f$                           | Fall Time                            | —    | 42    | —    |                     | $V_{GS} = 10V$ ③                                                                                                                                       |
| $L_D$                           | Internal Drain Inductance            | —    | 4.5   | —    | nH                  | Between lead, 6mm (0.25in.) from package and center of die contact  |
| $L_S$                           | Internal Source Inductance           | —    | 7.5   | —    |                     |                                                                                                                                                        |
| $C_{iss}$                       | Input Capacitance                    | —    | 2930  | —    | pF                  | $V_{GS} = 0V$                                                                                                                                          |
| $C_{oss}$                       | Output Capacitance                   | —    | 290   | —    |                     | $V_{DS} = 25V$                                                                                                                                         |
| $C_{rss}$                       | Reverse Transfer Capacitance         | —    | 180   | —    |                     | $f = 1.0\text{MHz}$                                                                                                                                    |
| $C_{oss}$                       | Output Capacitance                   | —    | 1200  | —    |                     | $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$                                                                                                        |
| $C_{oss}$                       | Output Capacitance                   | —    | 180   | —    |                     | $V_{GS} = 0V, V_{DS} = 80V, f = 1.0\text{MHz}$                                                                                                         |
| $C_{oss \text{ eff.}}$          | Effective Output Capacitance         | —    | 430   | —    |                     | $V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$                                                                                                             |

## Source-Drain Ratings and Characteristics

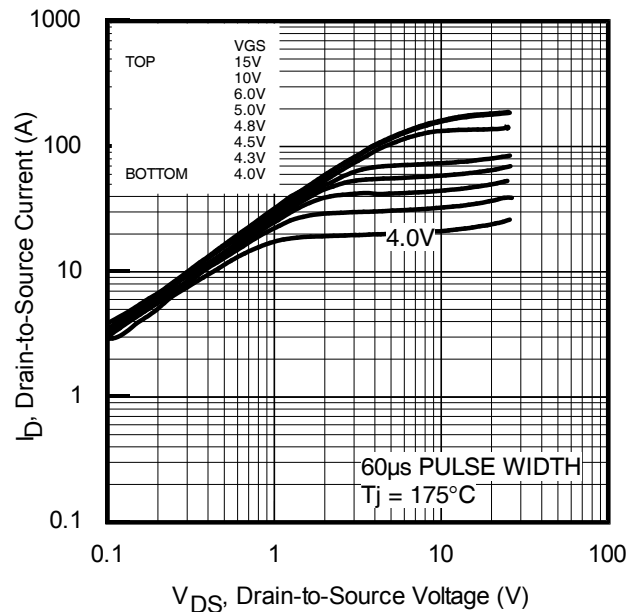
|          | Parameter                              | Min.                                                                        | Typ. | Max. | Units | Conditions                                                                                                                                           |
|----------|----------------------------------------|-----------------------------------------------------------------------------|------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| $I_S$    | Continuous Source Current (Body Diode) | —                                                                           | —    | 56   | A     | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ①   | —                                                                           | —    | 220  |       |                                                                                                                                                      |
| $V_{SD}$ | Diode Forward Voltage                  | —                                                                           | —    | 1.3  | V     | $T_J = 25^\circ\text{C}, I_S = 33A, V_{GS} = 0V$ ③                                                                                                   |
| $t_{rr}$ | Reverse Recovery Time                  | —                                                                           | 35   | 53   | ns    | $T_J = 25^\circ\text{C}, I_F = 33A, V_{DS} = 50V$                                                                                                    |
| $Q_{rr}$ | Reverse Recovery Charge                | —                                                                           | 41   | 62   | nC    | $di/dt = 100A/\mu s$ ③                                                                                                                               |
| $t_{on}$ | Forward Turn-On Time                   | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ ) |      |      |       |                                                                                                                                                      |

### Notes:

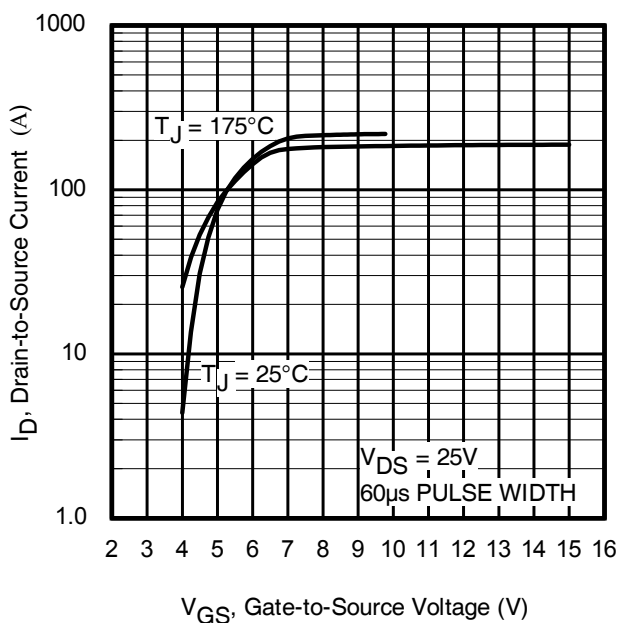
- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.28\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 33A$ ,  $V_{GS} = 10V$ . Part not recommended for use above this value.
- ③ Pulse width  $\leq 1.0\text{ms}$ ; duty cycle  $\leq 2\%$ .
- ④  $C_{oss \text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- ⑤ Limited by  $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ Refer to D-Pak package for Part Marking, Tape and Reel information



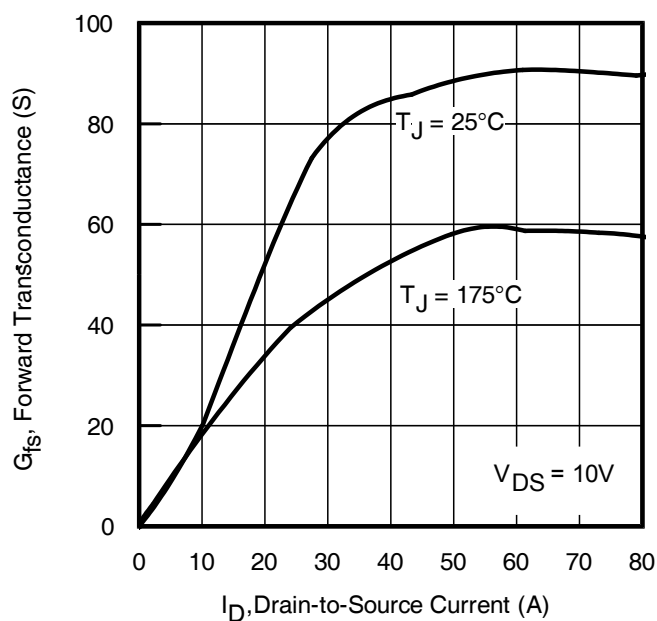
**Fig. 1** Typical Output Characteristics



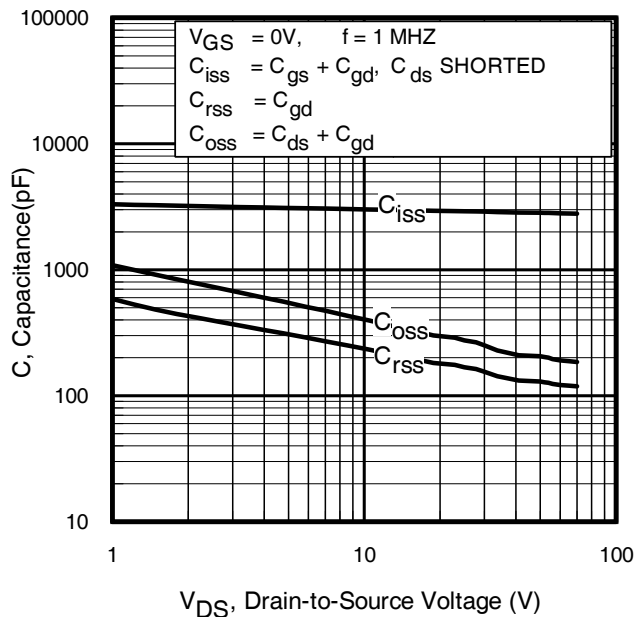
**Fig. 2** Typical Output Characteristics



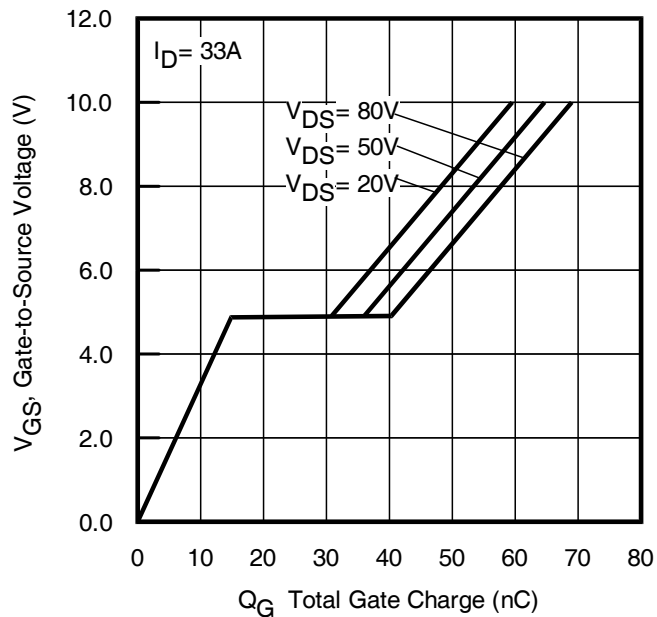
**Fig. 3** Typical Transfer Characteristics



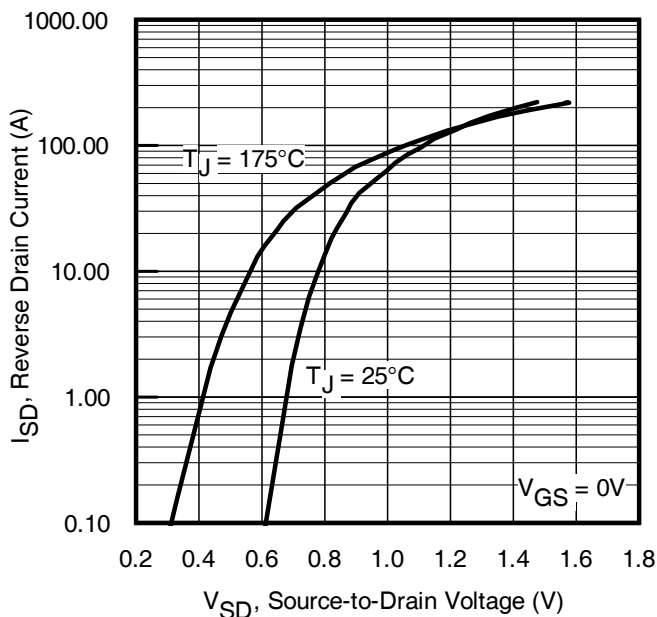
**Fig. 4** Typical Forward Transconductance vs. Drain Current



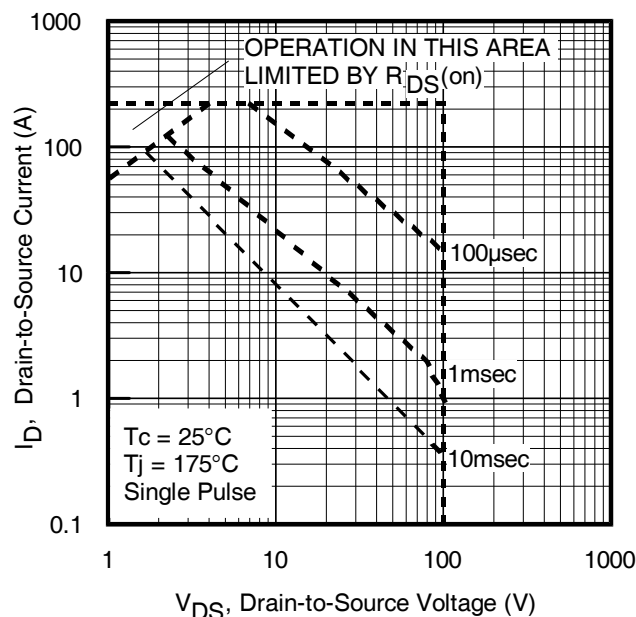
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



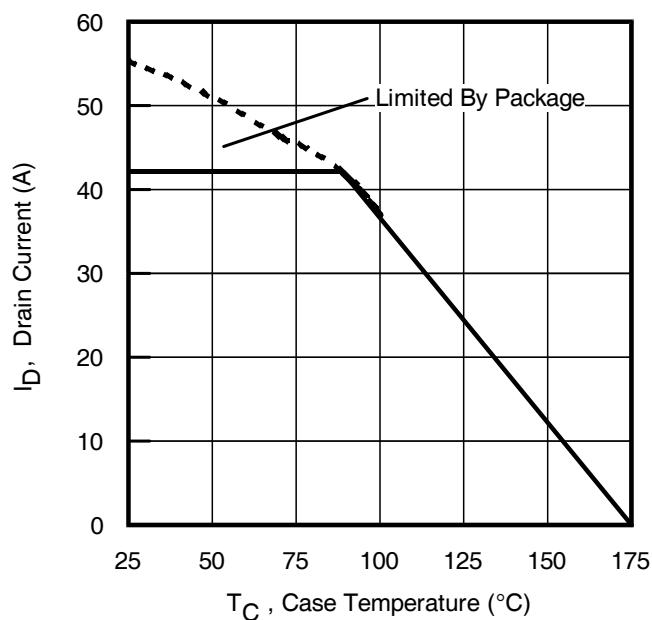
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



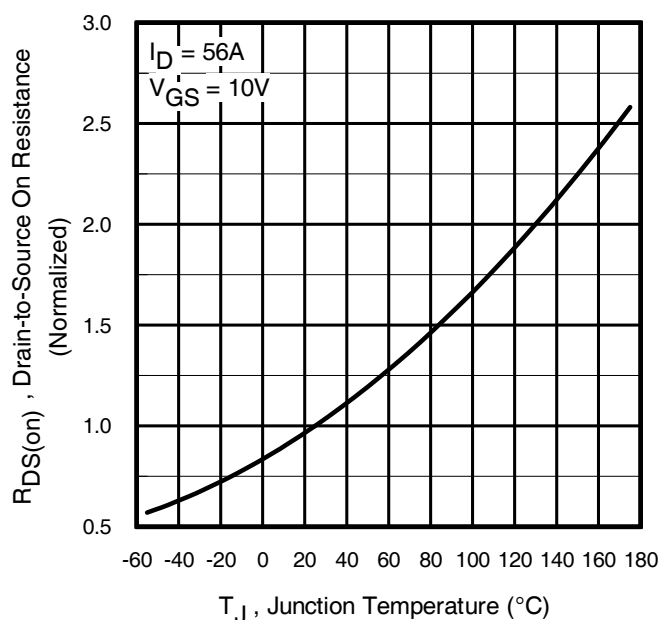
**Fig. 7** Typical Source-to-Drain Diode Forward Voltage



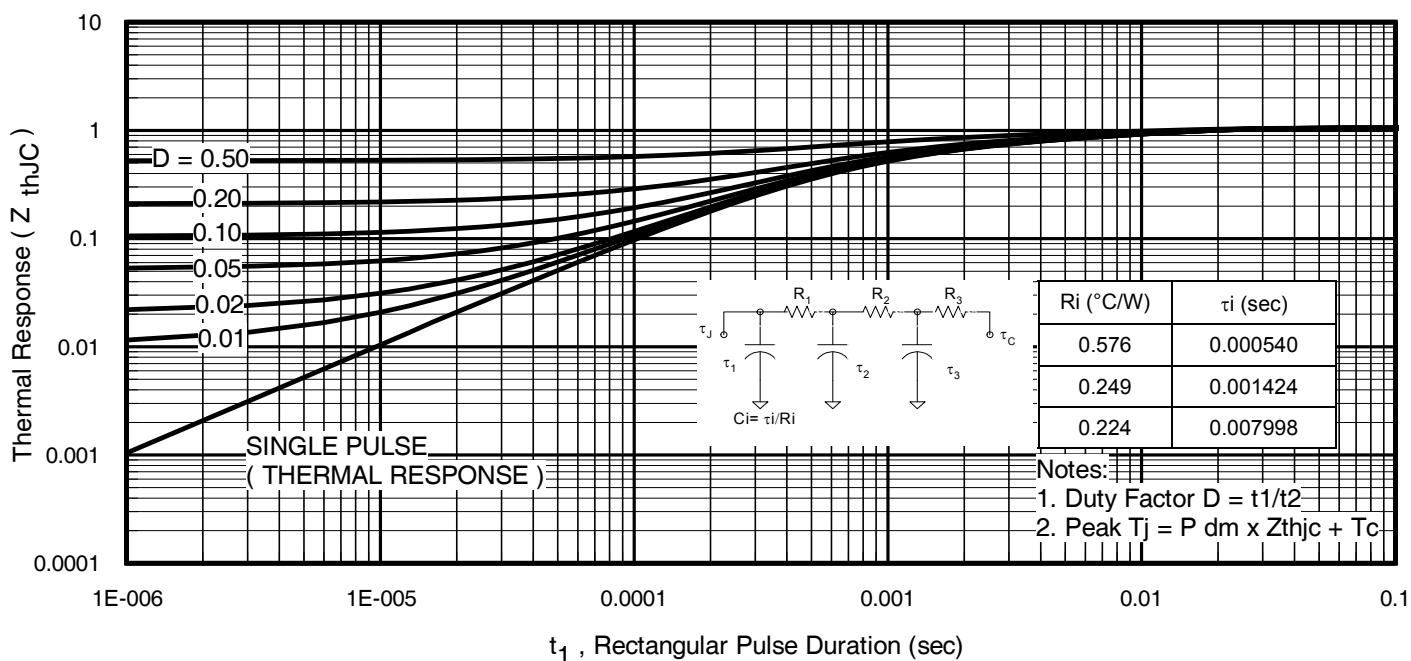
**Fig 8.** Maximum Safe Operating Area



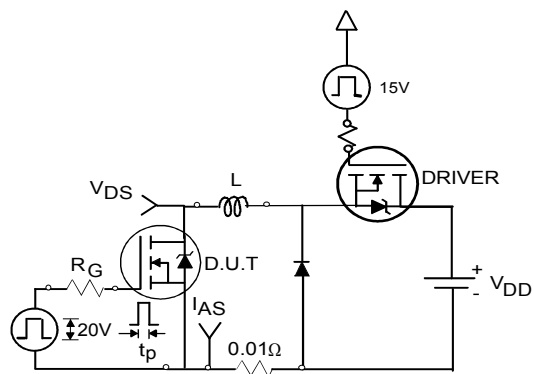
**Fig 9.** Maximum Drain Current vs. Case Temperature



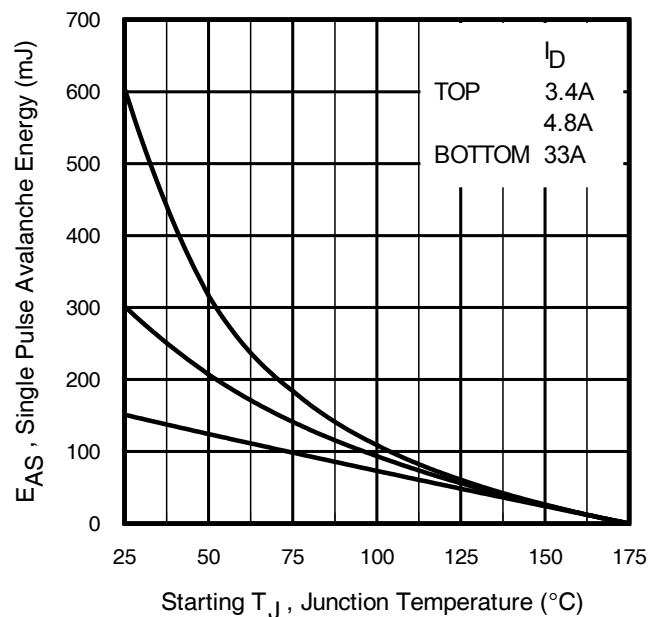
**Fig 10.** Normalized On-Resistance vs. Temperature



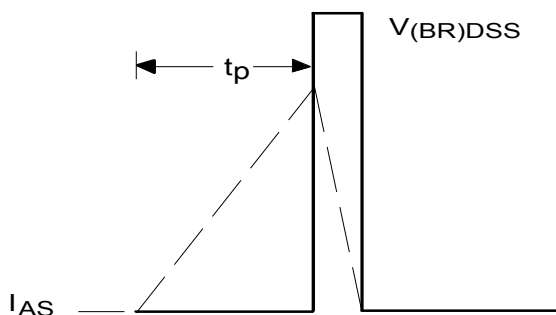
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



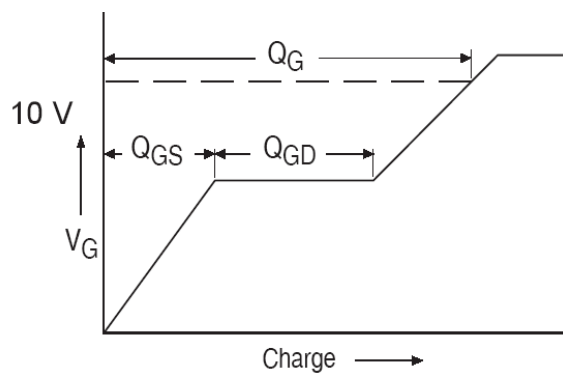
**Fig 12a.** Unclamped Inductive Test Circuit



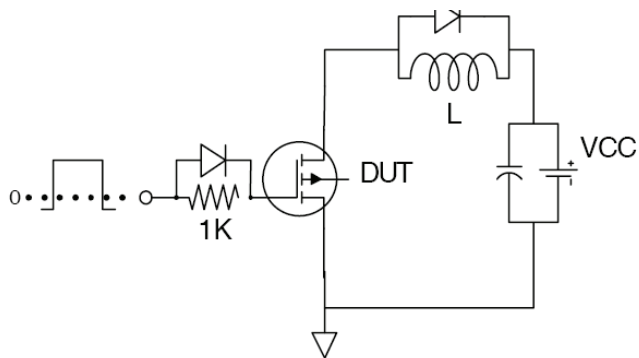
**Fig 12c.** Maximum Avalanche Energy vs. Drain Current



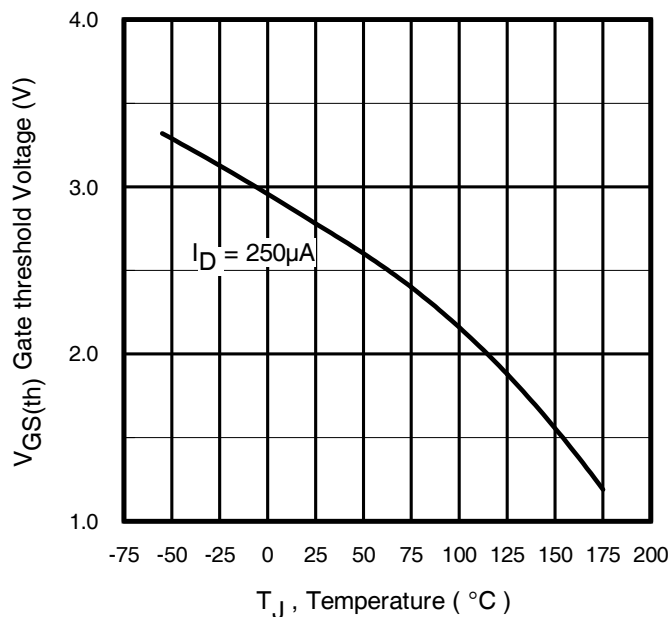
**Fig 12b.** Unclamped Inductive Waveforms



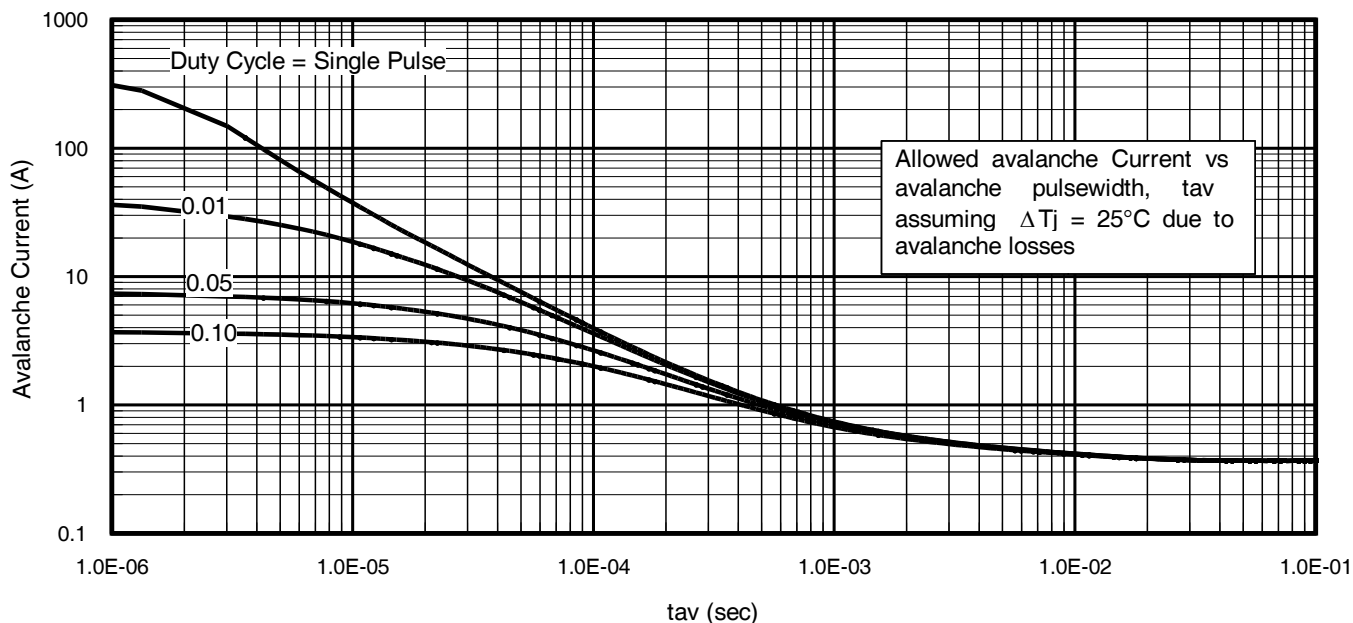
**Fig 13a.** Gate Charge Waveform



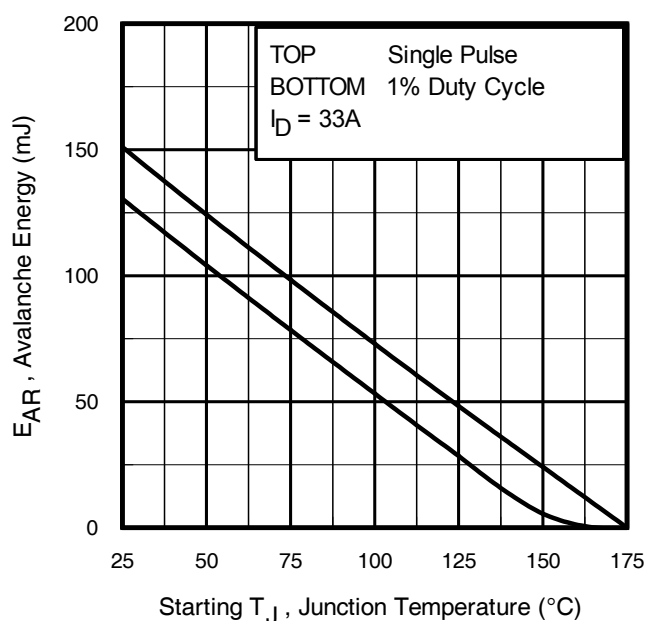
**Fig 13b.** Gate Charge Test Circuit



**Fig 14.** Threshold Voltage vs. Temperature



**Fig 15.** Typical Avalanche Current vs. Pulse width



**Fig 16.** Maximum Avalanche Energy vs. Temperature

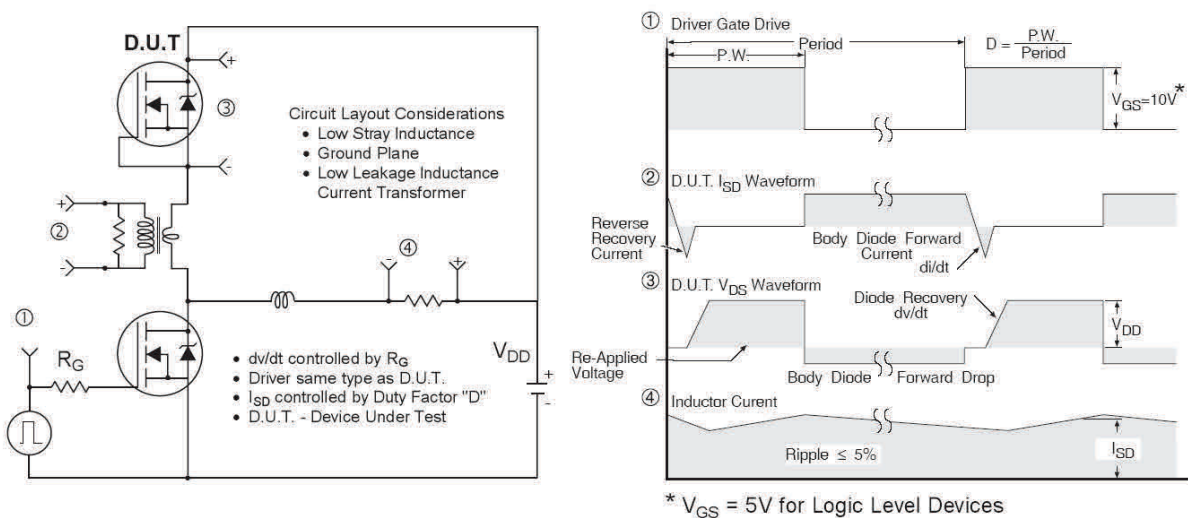
## Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at [www.infineon.com](http://www.infineon.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

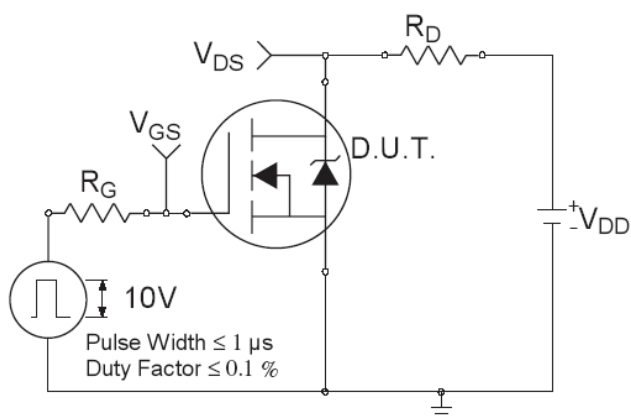
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

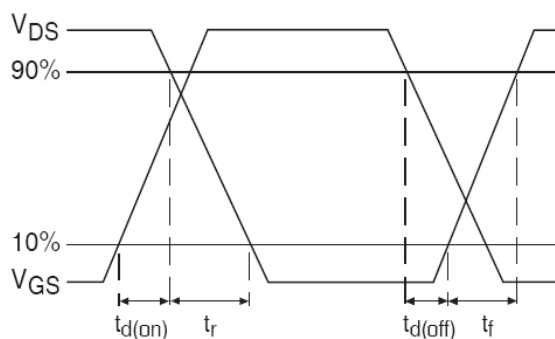
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



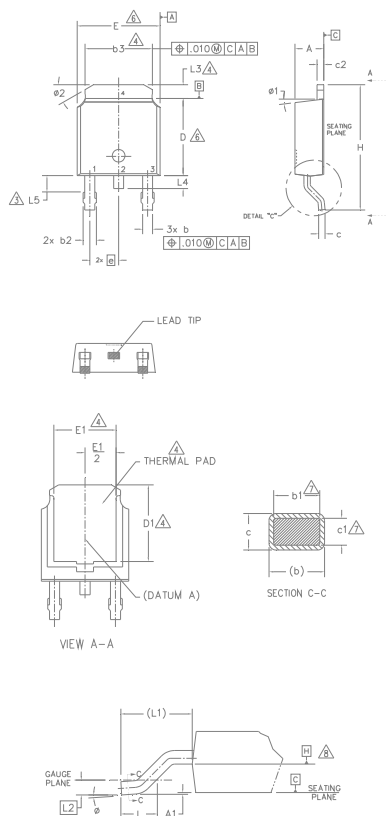
**Fig 18a.** Switching Time Test Circuit



**Fig 18b.** Switching Time Waveforms



**D-Pak (TO-252AA) Package Outline** (Dimensions are shown in millimeters (inches))



NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.15 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

| SYMBOL | DIMENSIONS  |       |        |      | NOTES |
|--------|-------------|-------|--------|------|-------|
|        | MILLIMETERS |       | INCHES |      |       |
|        | MIN.        | MAX.  | MIN.   | MAX. |       |
| A      | 2.18        | 2.39  | .086   | .094 |       |
| 1      | —           | 0.13  | —      | .005 |       |
| b      | 0.64        | 0.89  | .025   | .035 |       |
| b1     | 0.64        | 0.79  | .025   | .031 | 7     |
| b2     | 0.76        | 1.14  | .030   | .045 |       |
| b3     | 4.95        | 5.46  | .195   | .215 | 4     |
| c      | 0.46        | 0.61  | .018   | .024 |       |
| c1     | 0.41        | 0.56  | .016   | .022 | 7     |
| c2     | 0.46        | 0.89  | .018   | .035 |       |
| D      | 5.97        | 6.22  | .235   | .245 | 6     |
| D1     | 5.21        | —     | .205   | —    | 4     |
| E      | 6.35        | 6.73  | .250   | .265 | 6     |
| E1     | 4.32        | —     | .170   | —    | 4     |
| e      | 2.29        | BSC   | .090   | BSC  |       |
| H      | 9.40        | 10.41 | .370   | .410 |       |
| L      | 1.40        | 1.78  | .055   | .070 |       |
| L1     | 2.74        | BSC   | .108   | REF. |       |
| L2     | 0.51        | BSC   | .020   | BSC  |       |
| L3     | 0.89        | 1.27  | .035   | .050 | 4     |
| L4     | —           | 1.02  | —      | .040 |       |
| L5     | 1.14        | 1.52  | .045   | .060 | 3     |
| ø      | 0°          | 10°   | 0°     | 10°  |       |
| ø1     | 0°          | 15°   | 0°     | 15°  |       |
| ø2     | 25°         | 35°   | 25°    | 35°  |       |

## LEAD ASSIGNMENTS

## HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

### D-Pak (TO-252AA) Part Marking Information

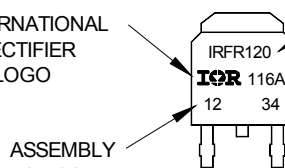
EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 2001  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

"P" in assembly line position indicates  
"Lead-Free" qualification to the consumer-level

OR

INTERNATIONAL  
RECTIFIER  
LOGO

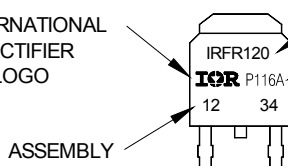


ASSEMBLY  
LOT CODE

PART NUMBER

✓ DATE CODE  
YEAR 1 = 2001  
WEEK 16  
LINE A

INTERNATIONAL  
RECTIFIER  
LOGO



ASSEMBLY  
LOT CODE

PART NUMBER

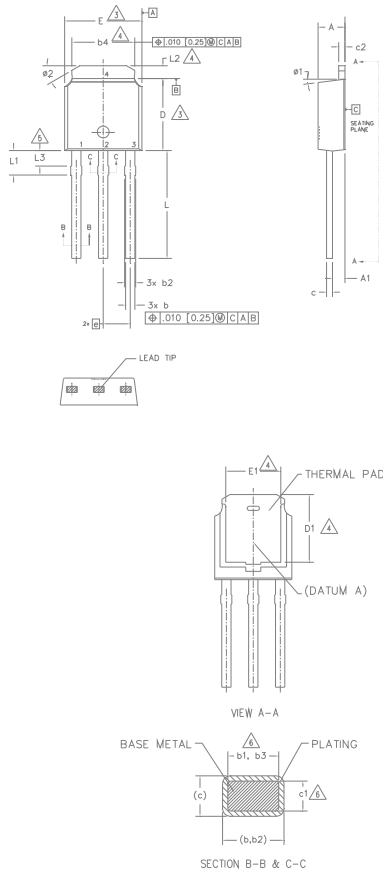
DATE CODE  
P = DESIGNATES LEAD-FREE  
PRODUCT (OPTIONAL)  
 $\bar{P}$  = DESIGNATES LEAD-FREE  
PRODUCT QUALIFIED TO THE  
CONSUMER LEVEL (OPTIONAL)

YEAR 1 = 2001  
WEEK 16  
A = ASSEMBLY SITE CODE

**Notes:**

1. For an Automotive Qualified version of this part please see <http://www.infineon.com/product-info/datasheets/data/auiifr3710z.pdf>
2. For the most current drawing please refer to Infineon website at <http://www.infineon.com/package/>

## I-Pak (TO-251AA) Package Outline Dimensions are shown in millimeters (inches)



### NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
5. LEAD DIMENSION UNCONTROLLED IN L3.
6. DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
- 8.- CONTROLLING DIMENSION : INCHES.

| SYMBOL | DIMENSIONS  |      |          |      | NOTES |
|--------|-------------|------|----------|------|-------|
|        | MILLIMETERS |      | INCHES   |      |       |
|        | MIN.        | MAX. | MIN.     | MAX. |       |
| A      | 2.18        | 2.39 | .086     | .094 | 6     |
| A1     | 0.89        | 1.14 | .035     | .045 |       |
| b      | 0.64        | 0.89 | .025     | .035 |       |
| b1     | 0.65        | 0.79 | .025     | .031 |       |
| b2     | 0.76        | 1.14 | .030     | .045 | 6     |
| b3     | 0.76        | 1.04 | .030     | .041 |       |
| b4     | 4.95        | 5.46 | .195     | .215 | 4     |
| c      | 0.46        | 0.61 | .018     | .024 | 6     |
| c1     | 0.41        | 0.56 | .016     | .022 |       |
| c2     | 0.46        | 0.89 | .018     | .035 |       |
| D      | 5.97        | 6.22 | .235     | .245 | 3     |
| D1     | 5.21        | —    | .205     | —    | 4     |
| E      | 6.35        | 6.73 | .250     | .265 | 3     |
| E1     | 4.32        | —    | .170     | —    | 4     |
| e      | 2.29 BSC    |      | .090 BSC |      |       |
| L      | 8.89        | 9.65 | .350     | .380 |       |
| L1     | 1.91        | 2.29 | .045     | .090 |       |
| L2     | 0.89        | 1.27 | .035     | .050 | 4     |
| L3     | 0.89        | 1.52 | .035     | .060 | 5     |
| ø1     | 0"          | 15"  | 0"       | 15"  |       |
| ø2     | 25"         | 35"  | 25"      | 35"  |       |

### LEAD ASSIGNMENTS

### HEXFET

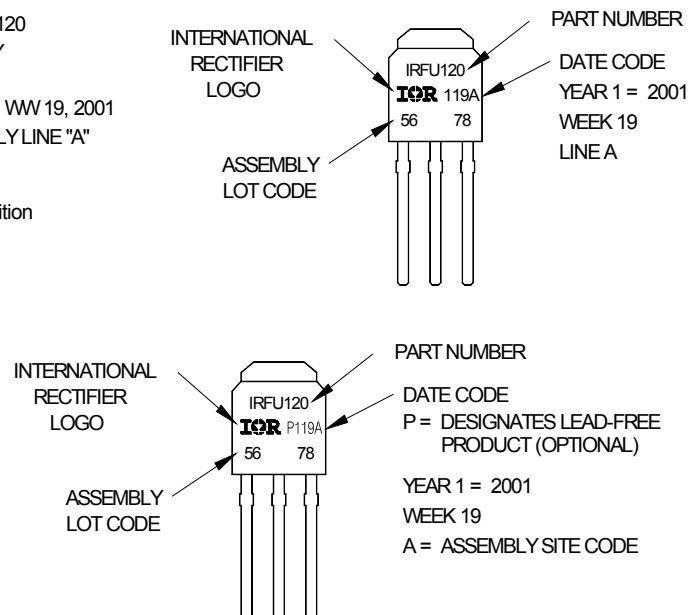
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 2001  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates Lead-Free

OR

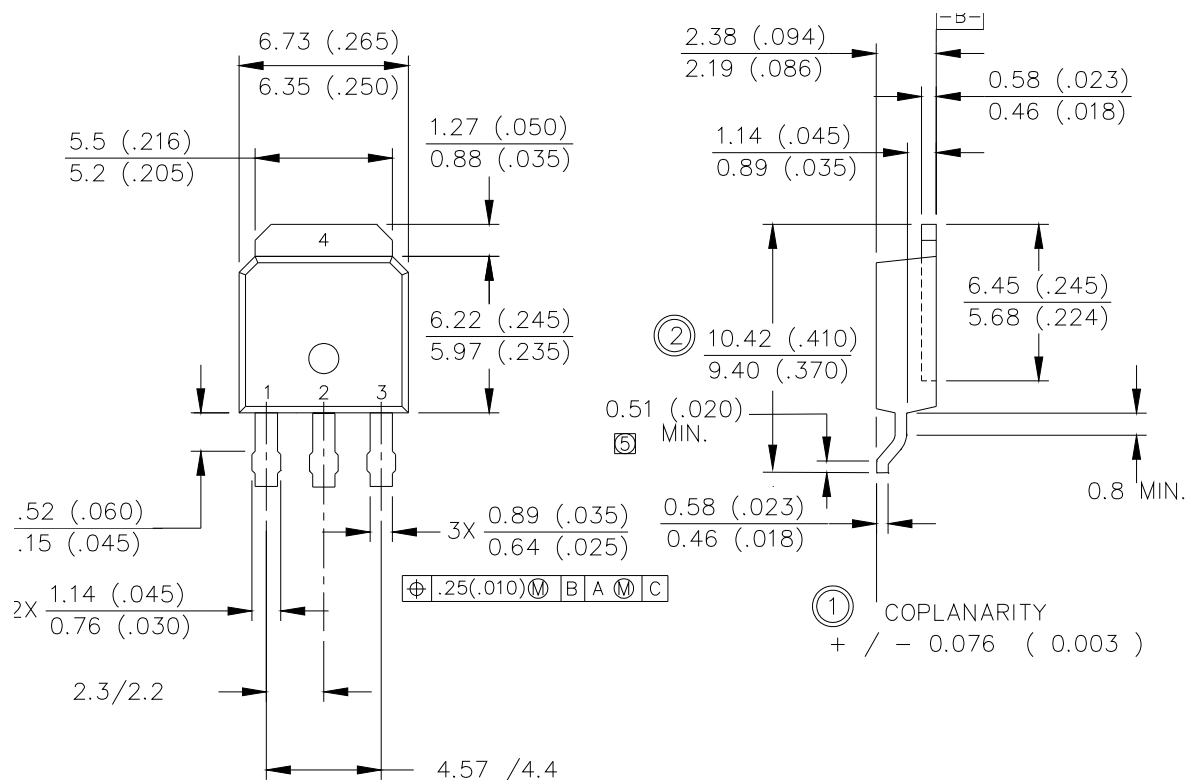


### Notes:

1. For an Automotive Qualified version of this part please see <http://www.infineon.com/product-info/auto/>
2. For the most current drawing please refer to Infineon website at <http://www.infineon.com/package/>

**I-Pak Leadform Option 701 Package Outline ⑧**

Dimensions are shown in millimeters (inches)

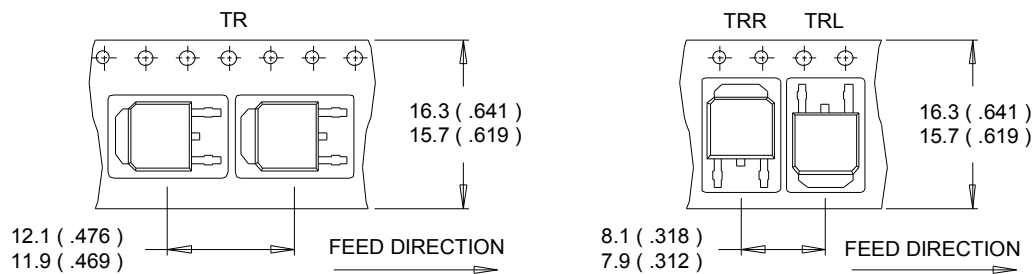


- 1-. GATE
- 2-. DRAIN
- 3-. SOURCE
- 4-. DRAIN

**NOTES:**

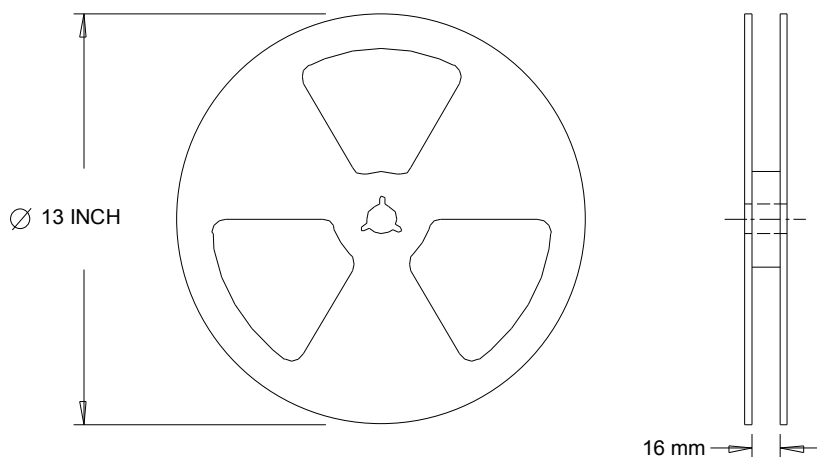
- 1.0 CONTROL DIMENSIONS IN INCHES
- 2.0 PARALLELISM AND ANGULARITY MAX. 0.076 (0.003)
- 3.0 LEADFORM CRITICAL DIMENSIONS DOUBLE RINGED

**D-Pak (TO-252AA) Tape & Reel Information Dimensions are shown in millimeters (inches)**



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to Infineon's web site [www.infineon.com](http://www.infineon.com)

## Qualification Information<sup>†</sup>

| Qualification Level        | Industrial<br>(per JEDEC JESD47F) <sup>††</sup> |                                              |
|----------------------------|-------------------------------------------------|----------------------------------------------|
| Moisture Sensitivity Level | D-Pak                                           | MSL1<br>(per JEDEC J-STD-020D) <sup>††</sup> |
|                            | I-Pak                                           |                                              |
| RoHS Compliant             | Yes                                             |                                              |

† Qualification standards can be found at Infineon's web site [www.infineon.com](http://www.infineon.com)

†† Applicable version of JEDEC standard at the time of product release.

## Revision History

| Date      | Comments                                                                                                                             |
|-----------|--------------------------------------------------------------------------------------------------------------------------------------|
| 5/31/2016 | <ul style="list-style-type: none"> <li>Updated datasheet with corporate template.</li> <li>Added disclaimer on last page.</li> </ul> |

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