P-Channel NexFET™ Power MOSFET

FEATURES

- Dual P-Ch MOSFETs
- Common Source Configuration
- Small Footprint 1mm × 1.5mm
- Gate-Source Voltage Clamp
- Gate ESD Protection –3kV
- Pb Free
- RoHS Compliant
- Halogen Free

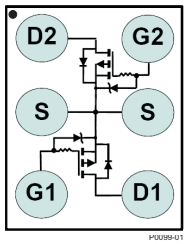
APPLICATIONS

- Battery Management
- Load Switch
- Battery Protection

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile. Low on resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.

Figure 1. Top View



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	–20		V
Q_g	Gate Charge Total (-4.5V)	1.6		nC
Q_{gd}	Gate Charge Gate to Drain	0.4		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = –1.8V	145	mΩ
		V_{GS} = –2.5V	115	mΩ
		V_{GS} = –4.5V	95	mΩ
$R_{D1D2(on)}$	Drain to Drain On Resistance	V_{GS} = -1.8V	245	mΩ
		V_{GS} = -2.5V	180	mΩ
		V_{GS} = -4.5V	140	mΩ
$V_{GS(th)}$	Threshold Voltage	–0.65		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD75205W1015	1-mm × 1.5-mm Wafer Level Package	7-Inch Reel	3000	Tape and Reel

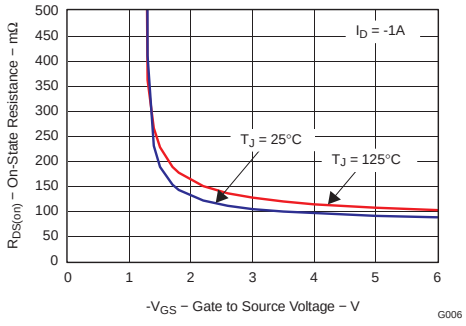
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	–20	V
V_{GS}	Gate to Source Voltage	-6	V
I_{DS}	Continuous Drain to Source Current, T_C = 25°C(1)	–1.2	A
	Pulsed Drain to Source Current, T_C = 25°C(2)	-9.6	A
I_S	Continuous Source Pin Current	-2.3	A
	Pulsed Source Pin Current(2)	-30	A
I_G	Continuous Gate Clamp Current	-0.5	A
	Pulsed Gate Clamp Current(2)	-7	A
P_D	Power Dissipation(1)	0.75	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C

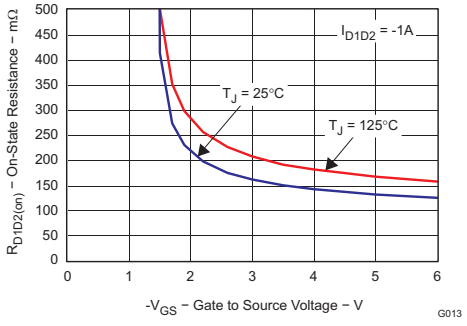
(1) Per device, both sides in conduction

(2) Pulse duration 10µs, duty cycle ≤2%

$R_{DS(on)}$ vs V_{GS}



$R_{D1D2(on)}$ vs V_{GS}



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

T_A = 25°C unless otherwise stated

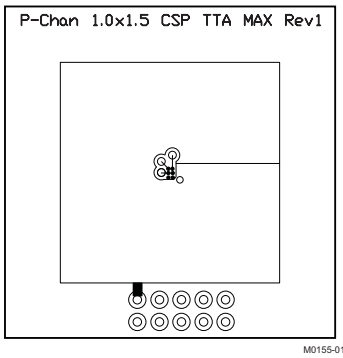
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_{DS} = –250µA	–20			V
BV_{GSS}	Gate to Source Voltage	V_{DS} = 0V, I_G = -250µA	-6.1		-7.2	V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = –16V			–1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = -6V			–100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = –250µA	–0.45	–0.65	–0.85	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = –1.8V, I_D = –1A		145	180	mΩ
		V_{GS} = –2.5V, I_D = –1A		115	145	mΩ
		V_{GS} = –4.5V, I_D = –1A		95	120	mΩ
$R_{D1D2(on)}$	Source to Drain On Resistance	V_{GS} = -1.8V, I_{D1D2} = –1A		245	305	mΩ
		V_{GS} = -2.5V, I_{D1D2} = –1A		180	225	mΩ
		V_{GS} = -4.5V, I_{D1D2} = –1A		140	175	mΩ
g_{fs}	Transconductance	V_{DS} = –10V, I_D = –1A		5		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = –10V, f = 1MHz		205	265	pF
C_{OSS}	Output Capacitance			80	105	pF
C_{RSS}	Reverse Transfer Capacitance			25	33	pF
Q_g	Gate Charge Total (–4.5V)	V_{DS} = –10V, I_{DS} = –1A		1.6	2.2	nC
Q_{gd}	Gate Charge - Gate to Drain			0.4		nC
Q_{gs}	Gate Charge - Gate to Source			0.3		nC
$Q_{g(th)}$	Gate Charge at Vth			0.12		nC
Q_{OSS}	Output Charge	V_{DS} = –10.25V, V_{GS} = 0V		1.5		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10V, V_{GS} = –4.5V, I_{DS} = –1A, R_G = 10Ω		6.3		ns
t_r	Rise Time			5.3		ns
$t_{d(off)}$	Turn Off Delay Time			32		ns
t_f	Fall Time			17		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{DS} = –1A, V_{GS} = 0V		–0.75	–1	V
Q_{rr}	Reverse Recovery Charge	V_{dd} = –10.25V, I_F = –1A, di/dt = 200A/µs		5.7		nC
t_{rr}	Reverse Recovery Time	V_{dd} = –10.25V, I_F = –1A, di/dt = 200A/µs		15.7		ns

THERMAL CHARACTERISTICS

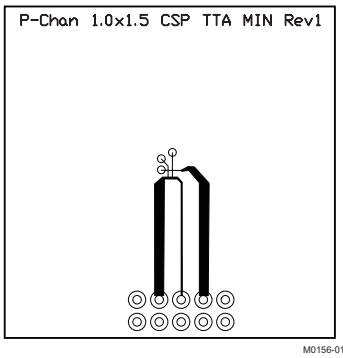
T_A = 25°C unless otherwise stated

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1) (2)			212	°C/W
	Thermal Resistance Junction to Ambient(2) (3)			119	°C/W

(1) Device mounted on FR4 material with Minimum Cu mounting area
(2) Measured with both devices biased in a parallel condition.
(3) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 119°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 212°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

Graphs are Per MOSFET at T_A = 25°C, unless stated otherwise. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

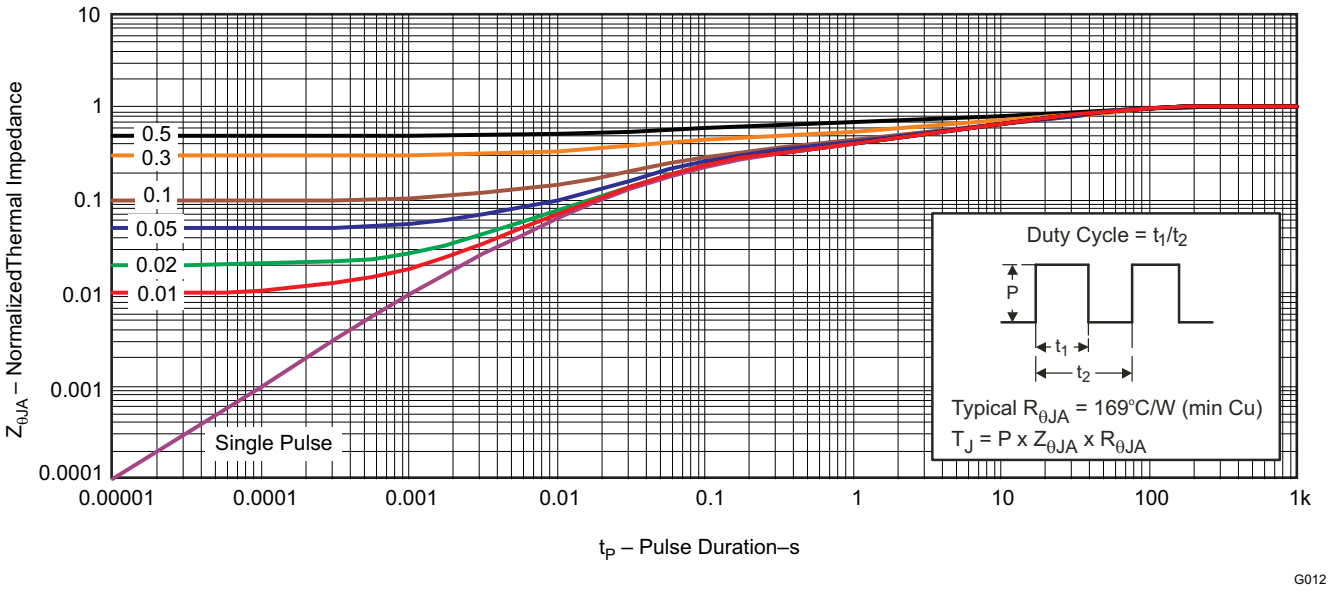


Figure 2. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

Graphs are Per MOSFET at T_A = 25°C, unless stated otherwise. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

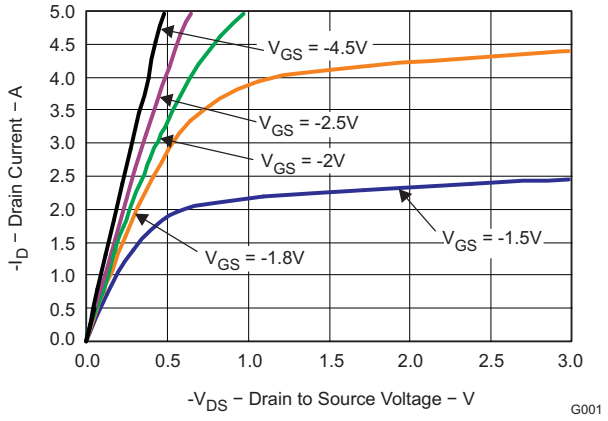


Figure 3. Saturation Characteristics

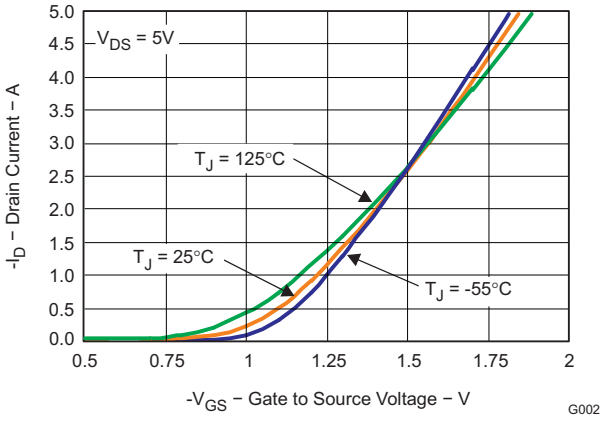


Figure 4. Transfer Characteristics

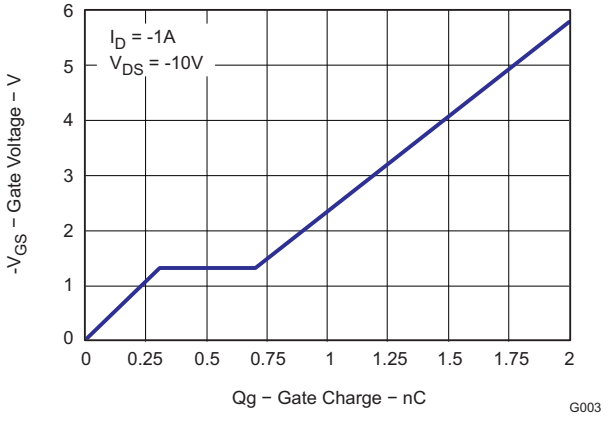


Figure 5. Gate Charge

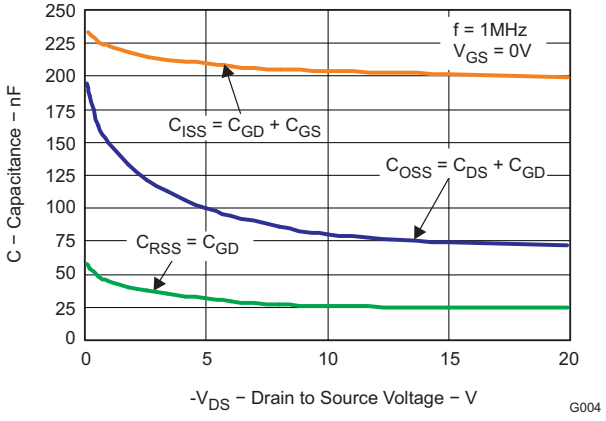


Figure 6. Capacitance

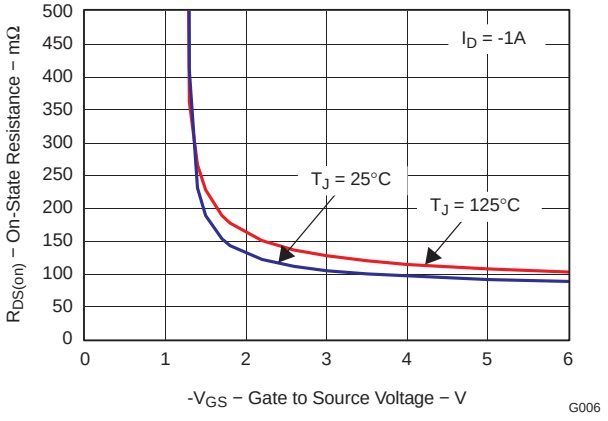


Figure 7. On-State Resistance vs. Gate Voltage

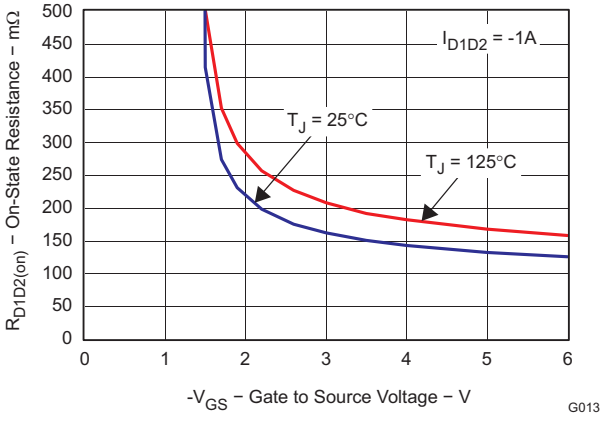


Figure 8. On-State Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

Graphs are Per MOSFET at T_A = 25°C, unless stated otherwise. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

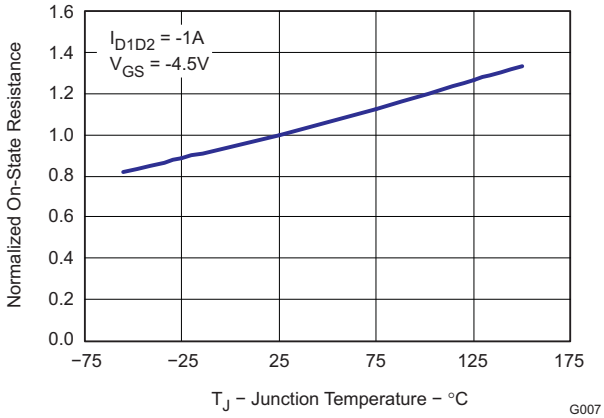


Figure 9. Normalized On-State Resistance vs. Temperature

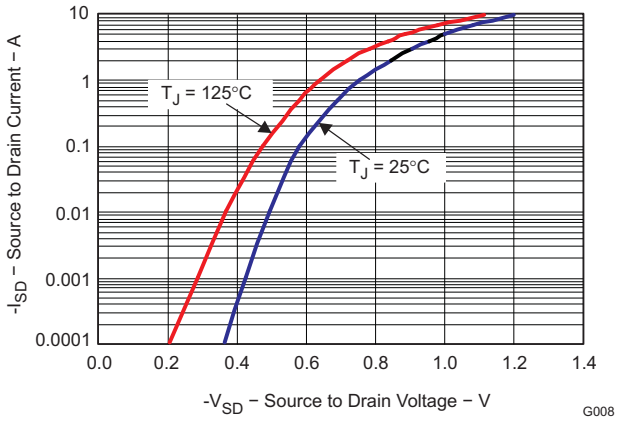


Figure 10. Typical Diode Forward Voltage

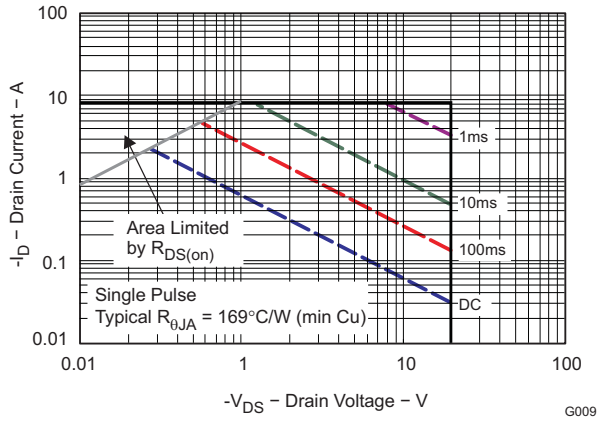


Figure 11. Maximum Safe Operating Area

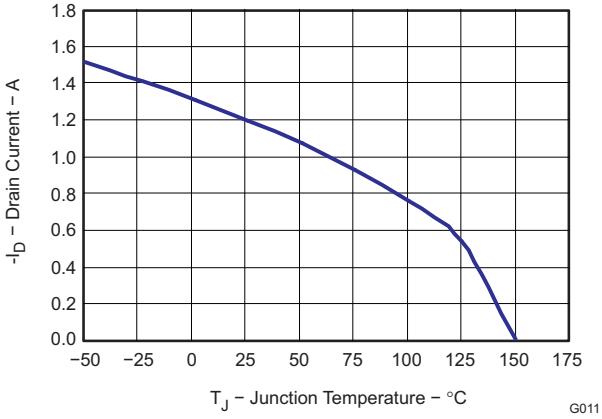


Figure 12. Maximum Drain Current vs. Temperature

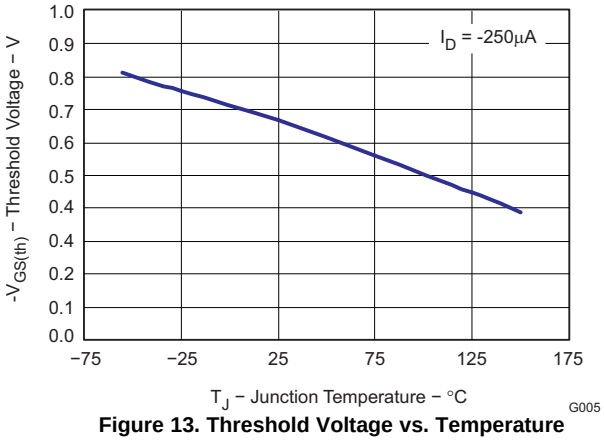
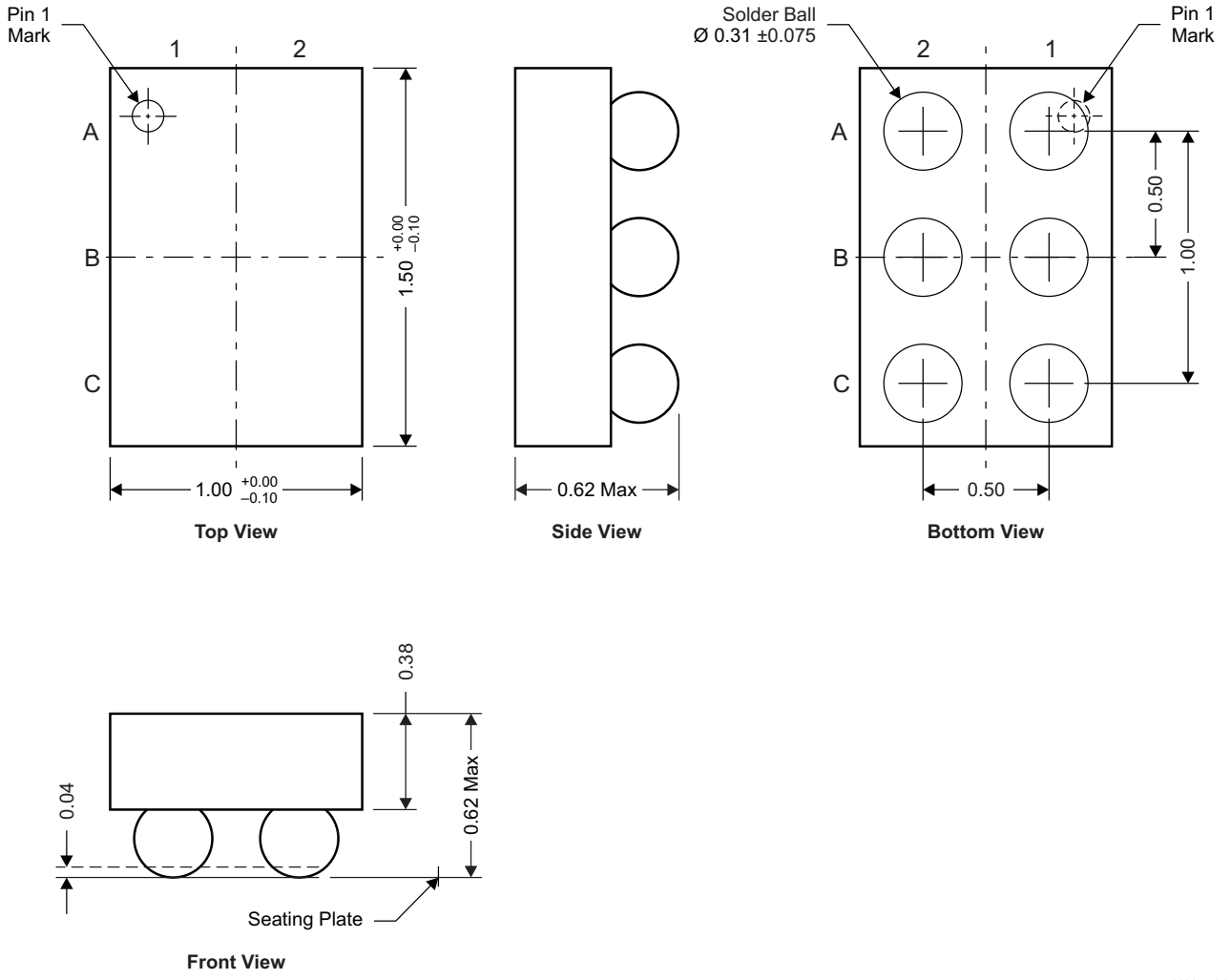


Figure 13. Threshold Voltage vs. Temperature

MECHANICAL DATA

CSD75205W1015 Package Dimensions

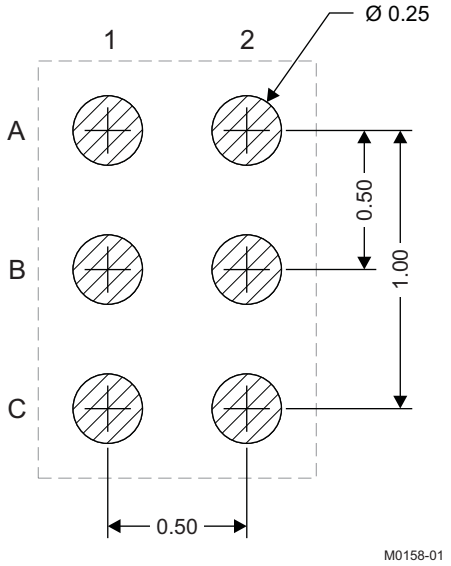


NOTE: All dimensions are in mm (unless otherwise specified)

Pinout

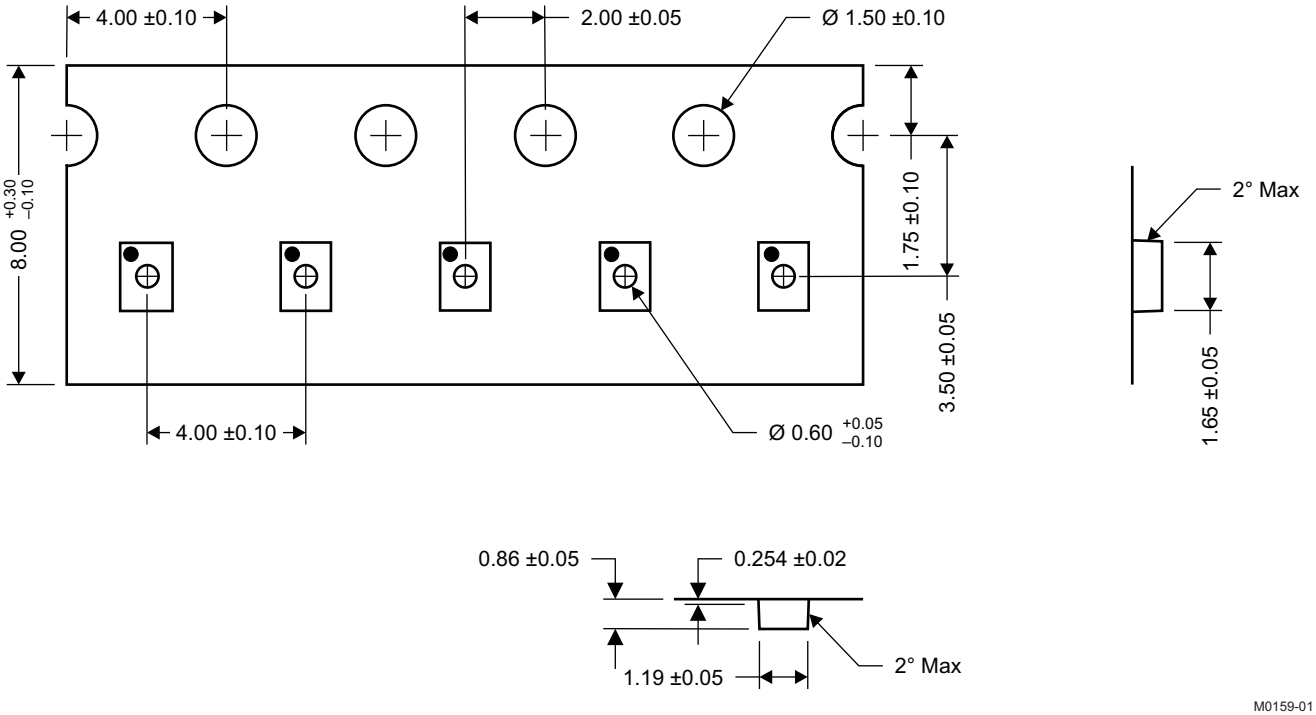
POSITION	DESIGNATION
B1, B2	Source
C1	Gate1
C2	Drain1
A2	Gate2
A1	Drain2

Figure 14. Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified)

REVISION HISTORY

Changes from Original (October 2009) to Revision A	Page
• Deleted the Package Marking Information section	7

Changes from Revision A (October 2009) to Revision B	Page
• Changed the CSD75205W1015 Package Dimensions section. Top View From: 15.00 To: 1.50	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD75205W1015	OBSOLETE	DSBGA	YZC	6		TBD	Call TI	Call TI	-55 to 150		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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