Dual 12-Bit, 80Msps Low Power 3V ADC

FEATURES

- **Integrated Dual 12-Bit ADCs**
- **Sample Rate: 80Msps**
- **Single 3V Supply (2.7V to 3.4V)**
- **Low Power: 422mW**
- **70.6dB SNR at 70MHz Input**
- **90dB SFDR at 70MHz Input**
- 110dB Channel Isolation at 100MHz
- Multiplexed or Separate Data Bus
- Flexible Input: $1V_{P-P}$ to $2V_{P-P}$ Range
- 575MHz Full Power Bandwidth S/H
- Clock Duty Cycle Stabilizer
- Shutdown and Nap Modes
- Pin Compatible Family
  105Msps: LTC2282 (12-Bit), LTC2284 (14-Bit)
  80Msps: LTC2294 (12-Bit), LTC2299 (14-Bit)
  65Msps: LTC2293 (12-Bit), LTC2298 (14-Bit)
  40Msps: LTC2292 (12-Bit), LTC2297 (14-Bit)
  25Msps: LTC2291 (12-Bit), LTC2296 (14-Bit)
  10Msps: LTC2290 (12-Bit), LTC2295 (14-Bit)
- 64-Pin (9mm × 9mm) QFN Package

APPLICATIONS

- Wireless and Wired Broadband Communication
- Imaging Systems
- Spectral Analysis
- Portable Instrumentation

DESCRIPTION

The LTC®2294 is a 12-bit 80Msps, low power dual 3V A/D converter designed for digitizing high frequency, wide dynamic range signals. The LTC2294 is perfect for demanding imaging and communications applications with AC performance that includes 70.6dB SNR and 90dB SFDR for signals well beyond the Nyquist frequency.

DC specs include ±0.4LSB INL (typ), ±0.2LSB DNL (typ) and no missing codes over temperature. The transition noise is a low $0.3LSB_{RMS}$.

A single 3V supply allows low power operation. A separate output supply allows the outputs to drive 0.5V to 3.6V logic. An optional multiplexer allows both channels to share a digital output bus.

A single-ended CLK input controls converter operation. An optional clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

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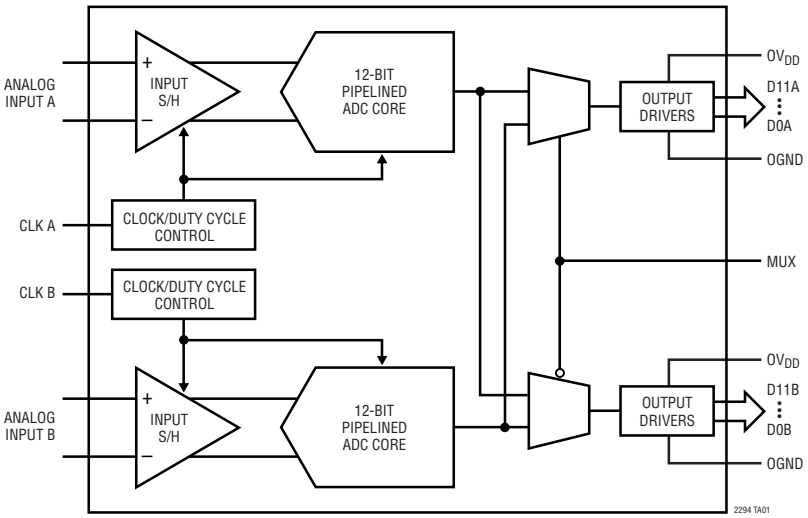
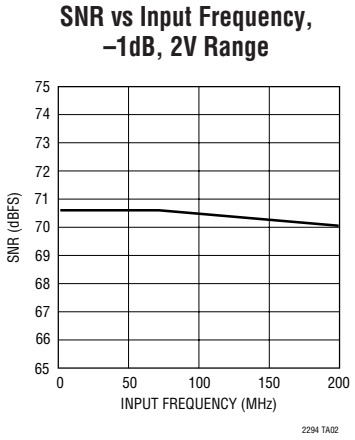
TYPICAL APPLICATION



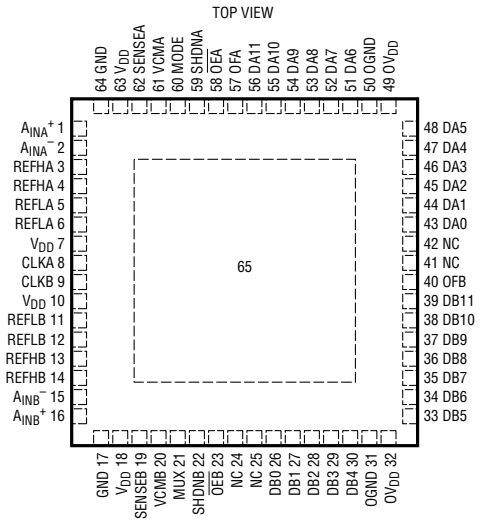


ABSOLUTE MAXIMUM RATINGS

OV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 4V
Digital Output Ground Voltage (OGND) .....–0.3V to 1V
Analog Input Voltage (Note 3) ..... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage ..... –0.3V to (V_{DD} + 0.3V)
Digital Output Voltage .....–0.3V to (OV_{DD} + 0.3V)
Power Dissipation 1500mW
Operating Temperature Range
LTC2294C .....0°C to 70°C
LTC2294I .....–40°C to 85°C
Storage Temperature Range .....–65°C to 125°C

PACKAGE/ORDER INFORMATION



UP PACKAGE
64-LEAD (9mm × 9mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 20°C/W
EXPOSED PAD (PIN 65) IS GND AND MUST BE SOLDERED TO PCB

ORDER PART NUMBER	QFN PART* MARKING
LTC2294IUP LTC2294CUP	LTC2294UP

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.
*The temperature grade is identified by a label on the shipping container.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	Differential Analog Input (Note 5)	●	–1.4	±0.4	1.4	LSB
Differential Linearity Error	Differential Analog Input	●	–0.8	±0.2	0.8	LSB
Offset Error	(Note 6)	●	–12	±2	12	mV
Gain Error	External Reference	●	–2.5	±0.5	2.5	%FS
Offset Drift				±10		µV/°C
Full-Scale Drift	Internal Reference			±30		ppm/°C
	External Reference			±5		ppm/°C
Gain Matching	External Reference			±0.3		%FS
Offset Matching				±2		mV
Transition Noise	SENSE = 1V			0.3		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ - A_{IN}^-$)	2.7V < V_{DD} < 3.4V (Note 7)	●		±0.5 to ±1		V
$V_{IN,CM}$	Analog Input Common Mode ($A_{IN}^+ + A_{IN}^-$)/2	Differential Input (Note 7)	●	1	1.5	1.9	V
		Single Ended Input (Note 7)	●	0.5	1.5	2	V
I_{IN}	Analog Input Leakage Current	0V < A_{IN}^+, A_{IN}^- < V_{DD}	●	–1		1	µA
I_{SENSE}	SENSEA, SENSEB Input Leakage	0V < SENSEA, SENSEB < 1V	●	–3		3	µA
I_{MODE}	MODE Input Leakage Current	0V < MODE < V_{DD}	●	–3		3	µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter				0.2		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio				80		dB
	Full Power Bandwidth	Figure 8 Test Circuit			575		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input			70.6		dB
		40MHz Input	●	69.1	70.6		dB
		70MHz Input			70.6		dB
		140MHz Input			70.3		dB
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	5MHz Input			90		dB
		40MHz Input	●	74	90		dB
		70MHz Input			90		dB
		140MHz Input			85		dB
SFDR	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input			90		dB
		40MHz Input	●	79	90		dB
		70MHz Input			90		dB
		140MHz Input			90		dB
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input			70.6		dB
		40MHz Input	●	68.7	70.5		dB
		70MHz Input			70.5		dB
		140MHz Input			70		dB
I_{MD}	Intermodulation Distortion	f_{IN} = 40MHz, 41MHz			90		dB
	Crosstalk	f_{IN} = 100MHz			–110		dB

INTERNAL REFERENCE CHARACTERISTICS (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0	1.475	1.500	1.525	V
V_{CM} Output Tempco			±25		ppm/°C
V_{CM} Line Regulation	2.7V < V_{DD} < 3.4V		3		mV/V
V_{CM} Output Resistance	–1mA < I_{OUT} < 1mA		4		Ω

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS (CLK, $\overline{OE}$, SHDN, MUX)							
V_{IH}	High Level Input Voltage	V_{DD} = 3V	●	2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 3V	●			0.8	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 7)			3		pF
LOGIC OUTPUTS							
OV_{DD} = 3V							
C_{OZ}	Hi-Z Output Capacitance	$\overline{OE}$ = High (Note 7)			3		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			50		mA
I_{SINK}	Output Sink Current	V_{OUT} = 3V			50		mA
V_{OH}	High Level Output Voltage	I_O = –10µA I_O = –200µA	 ●	 2.7	2.995 2.99		V V
V_{OL}	Low Level Output Voltage	I_O = 10µA I_O = 1.6mA	 ●		0.005 0.09	 0.4	V V
OV_{DD} = 2.5V							
V_{OH}	High Level Output Voltage	I_O = –200µA			2.49		V
V_{OL}	Low Level Output Voltage	I_O = 1.6mA			0.09		V
OV_{DD} = 1.8V							
V_{OH}	High Level Output Voltage	I_O = –200µA			1.79		V
V_{OL}	Low Level Output Voltage	I_O = 1.6mA			0.09		V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Analog Supply Voltage	(Note 9)	●	2.7	3	3.4	V
OV_{DD}	Output Supply Voltage	(Note 9)	●	0.5	3	3.6	V
IV_{DD}	Supply Current	Both ADCs at $f_{S(MAX)}$	●		141	165	mA
P_{DISS}	Power Dissipation	Both ADCs at $f_{S(MAX)}$	●		422	495	mW
P_{SHDN}	Shutdown Power (Each Channel)	SHDN = H, OE = H, No CLK			2		mW
P_{NAP}	Nap Mode Power (Each Channel)	SHDN = H, OE = L, No CLK			15		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_s	Sampling Frequency	(Note 9)	●	1		80	MHz
t_L	CLK Low Time	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On (Note 7)	● ●	5.9 5	6.25 6.25	500 500	ns ns
t_H	CLK High Time	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On (Note 7)	● ●	5.9 5	6.25 6.25	500 500	ns ns
t_{AP}	Sample-and-Hold Aperture Delay				0		ns
t_D	CLK to DATA Delay	C_L = 5pF (Note 7)	●	1.4	2.7	5.4	ns
t_{MD}	MUX to DATA Delay	C_L = 5pF (Note 7)	●	1.4	2.7	5.4	ns
	Data Access Time After $\overline{OE}\downarrow$	C_L = 5pF (Note 7)	●		4.3	10	ns
	BUS Relinquish Time	(Note 7)	●		3.3	8.5	ns
Pipeline Latency					5		Cycles

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: V_{DD} = 3V, f_{SAMPLE} = 80MHz, input range = $2V_{P-P}$ with differential drive, unless otherwise noted.

Note 5: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Offset error is the offset voltage measured from –0.5 LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

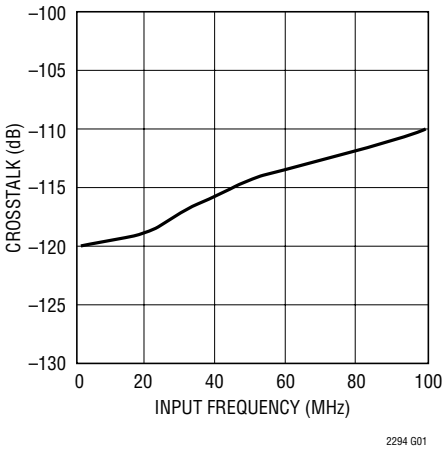
Note 7: Guaranteed by design, not subject to test.

Note 8: V_{DD} = 3V, f_{SAMPLE} = 80MHz, input range = $1V_{P-P}$ with differential drive. The supply current and power dissipation are the sum total for both channels with both channels active.

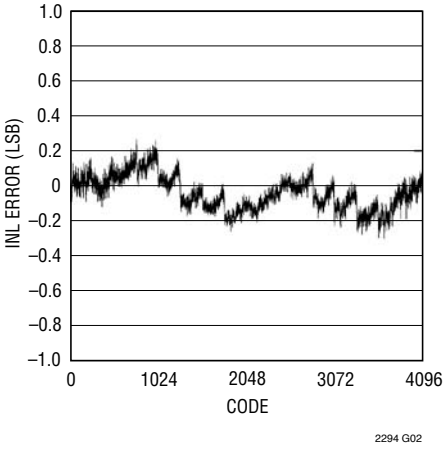
Note 9: Recommended operating conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

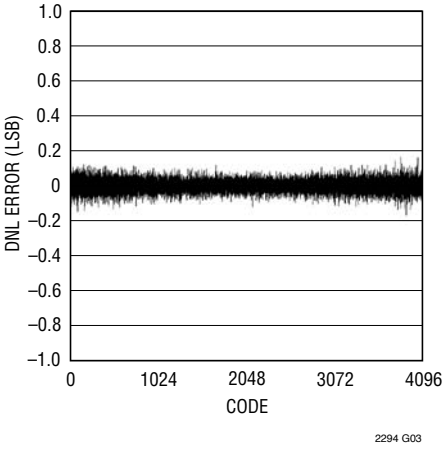
Crosstalk vs Input Frequency



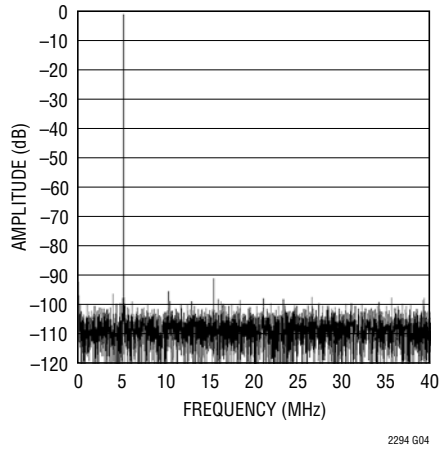
Typical INL, 2V Range, 80Msps



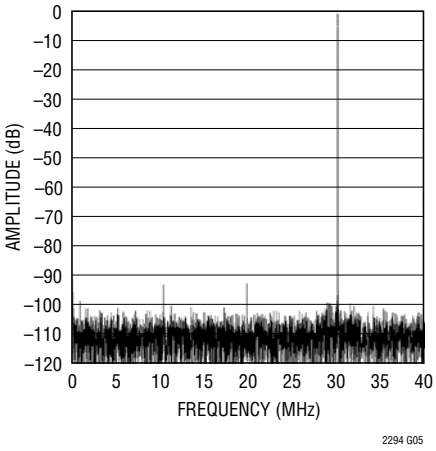
Typical DNL, 2V Range, 80Msps



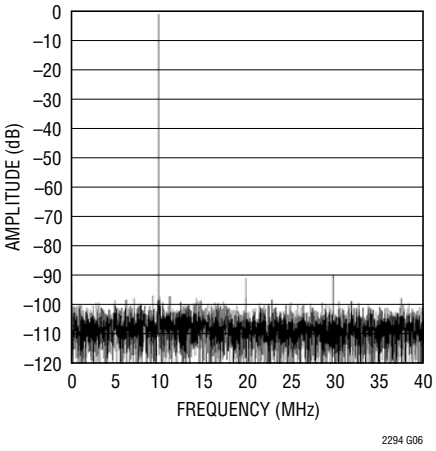
8192 Point FFT, f_{IN} = 5MHz, –1dB, 2V Range, 80Msps



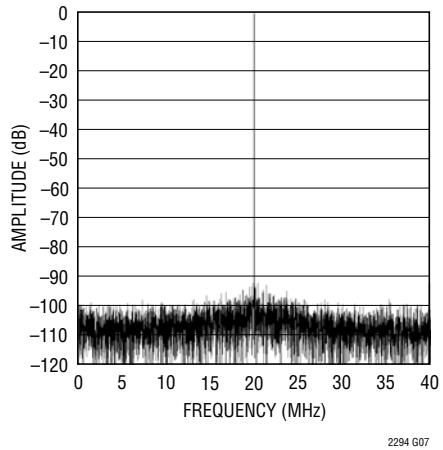
8192 Point FFT, f_{IN} = 30MHz, –1dB, 2V Range, 80Msps



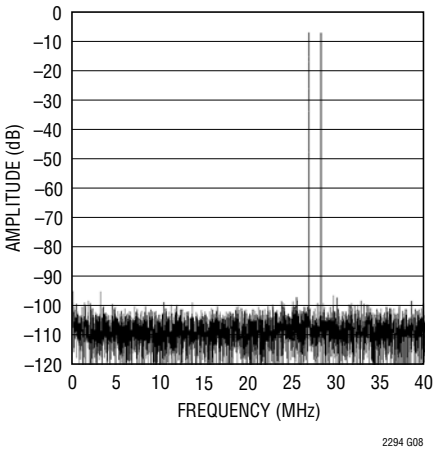
8192 Point FFT, f_{IN} = 70MHz, –1dB, 2V Range, 80Msps



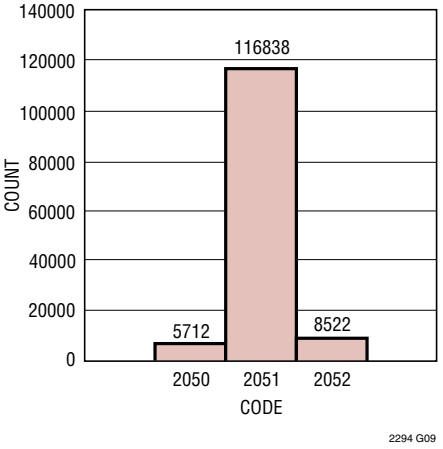
8192 Point FFT, f_{IN} = 140MHz, –1dB, 2V Range, 80Msps



8192 Point 2-Tone FFT, f_{IN} = 28.2MHz and 26.8MHz, –1dB, 2V Range

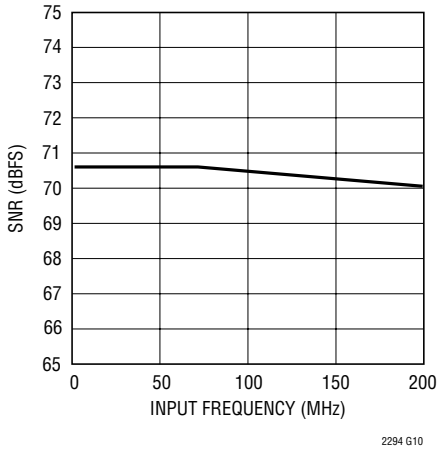


Grounded Input Histogram, 80Msps

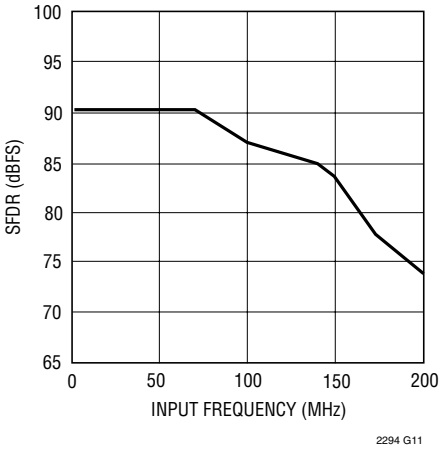


TYPICAL PERFORMANCE CHARACTERISTICS

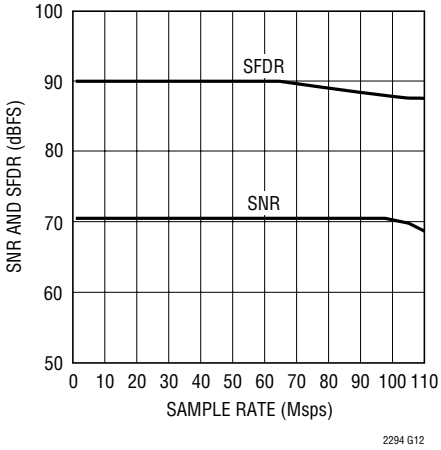
SNR vs Input Frequency, –1dB, 2V Range, 80Msps



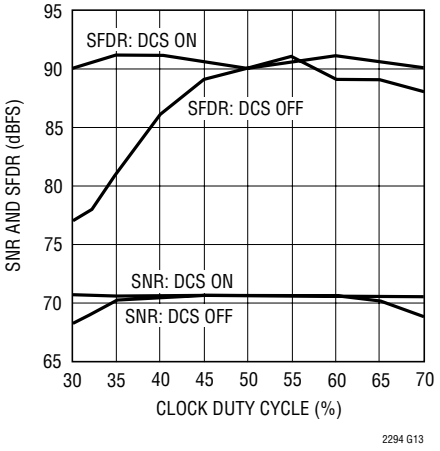
SFDR vs Input Frequency, –1dB, 2V Range, 80Msps



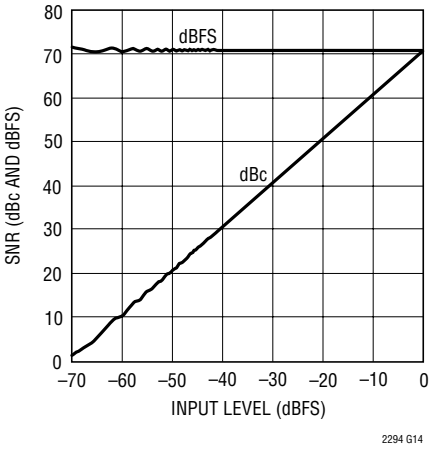
SNR and SFDR vs Sample Rate, 2V Range, f_{IN} = 5MHz, –1dB



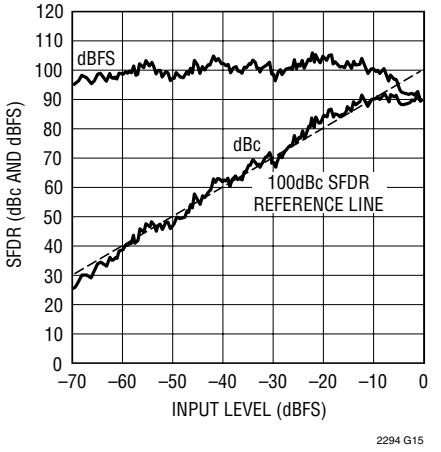
SNR and SFDR vs Clock Duty Cycle, 80Msps



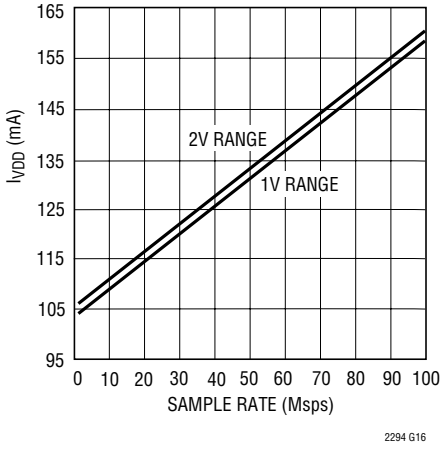
SNR vs Input Level, f_{IN} = 70MHz, 2V Range, 80Msps



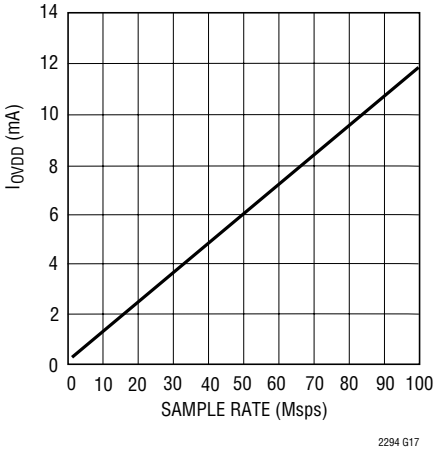
SFDR vs Input Level, f_{IN} = 70MHz, 2V Range, 80Msps



I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB



I_{OVDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB, O_{VDD} = 1.8V



PIN FUNCTIONS

A_{INA}^+ (Pin 1): Channel A Positive Differential Analog Input.

A_{INA}^- (Pin 2): Channel A Negative Differential Analog Input.

REFHA (Pins 3, 4): Channel A High Reference. Short together and bypass to Pins 5, 6 with a 0.1µF ceramic chip capacitor as close to the pin as possible. Also bypass to Pins 5, 6 with an additional 2.2µF ceramic chip capacitor and to ground with a 1µF ceramic chip capacitor.

REFLA (Pins 5, 6): Channel A Low Reference. Short together and bypass to Pins 3, 4 with a 0.1µF ceramic chip capacitor as close to the pin as possible. Also bypass to Pins 3, 4 with an additional 2.2µF ceramic chip capacitor and to ground with a 1µF ceramic chip capacitor.

V_{DD} (Pins 7, 10, 18, 63): Analog 3V Supply. Bypass to GND with 0.1µF ceramic chip capacitors.

CLKA (Pin 8): Channel A Clock Input. The input sample starts on the positive edge.

CLKB (Pin 9): Channel B Clock Input. The input sample starts on the positive edge.

REFLB (Pins 11, 12): Channel B Low Reference. Short together and bypass to Pins 13, 14 with a 0.1µF ceramic chip capacitor as close to the pin as possible. Also bypass to Pins 13, 14 with an additional 2.2µF ceramic chip capacitor and to ground with a 1µF ceramic chip capacitor.

REFHB (Pins 13, 14): Channel B High Reference. Short together and bypass to Pins 11, 12 with a 0.1µF ceramic chip capacitor as close to the pin as possible. Also bypass to Pins 11, 12 with an additional 2.2µF ceramic chip capacitor and to ground with a 1µF ceramic chip capacitor.

A_{INB}^- (Pin 15): Channel B Negative Differential Analog Input.

A_{INB}^+ (Pin 16): Channel B Positive Differential Analog Input.

GND (Pins 17, 64): ADC Power Ground.

SENSEB (Pin 19): Channel B Reference Programming Pin. Connecting SENSEB to V_{CMB} selects the internal reference and a ±0.5V input range. V_{DD} selects the internal reference and a ±1V input range. An external reference greater than 0.5V and less than 1V applied to SENSEB selects an input range of $\pm V_{SENSEB}$. ±1V is the largest valid input range.

V_{CMB} (Pin 20): Channel B 1.5V Output and Input Common Mode Bias. Bypass to ground with 2.2µF ceramic chip capacitor. Do not connect to V_{CMA}.

MUX (Pin 21): Digital Output Multiplexer Control. If MUX is High, Channel A comes out on DA0-DA13, OFA; Channel B comes out on DB0-DB13, OFB. If MUX is Low, the output busses are swapped and Channel A comes out on DB0-DB13, OFB; Channel B comes out on DA0-DA13, OFA. To multiplex both channels onto a single output bus, connect MUX, CLKA and CLKB together.

SHDNB (Pin 22): Channel B Shutdown Mode Selection Pin. Connecting SHDNB to GND and $\overline{OEB}$ to GND results in normal operation with the outputs enabled. Connecting SHDNB to GND and $\overline{OEB}$ to V_{DD} results in normal operation with the outputs at high impedance. Connecting SHDNB to V_{DD} and $\overline{OEB}$ to GND results in nap mode with the outputs at high impedance. Connecting SHDNB to V_{DD} and $\overline{OEB}$ to V_{DD} results in sleep mode with the outputs at high impedance.

$\overline{OEB}$ (Pin 23): Channel B Output Enable Pin. Refer to SHDNB pin function.

NC (Pins 24, 25, 41, 42): Do Not Connect These Pins.

DB0 – DB11 (Pins 26 to 30, 33 to 39): Channel B Digital Outputs. DB11 is the MSB.

OGND (Pins 31, 50): Output Driver Ground.

OV_{DD} (Pins 32, 49): Positive Supply for the Output Drivers. Bypass to ground with 0.1µF ceramic chip capacitor.

OFB (Pin 40): Channel B Overflow/Underflow Output. High when an overflow or underflow has occurred.

DA0 – DA11 (Pins 43 to 48, 51 to 56): Channel A Digital Outputs. DA11 is the MSB.

OFA (Pin 57): Channel A Overflow/Underflow Output. High when an overflow or underflow has occurred.

$\overline{OEA}$ (Pin 58): Channel A Output Enable Pin. Refer to SHDNA pin function.

PIN FUNCTIONS

SHDNA (Pin 59): Channel A Shutdown Mode Selection Pin. Connecting SHDNA to GND and $\overline{OEA}$ to GND results in normal operation with the outputs enabled. Connecting SHDNA to GND and $\overline{OEA}$ to V_{DD} results in normal operation with the outputs at high impedance. Connecting SHDNA to V_{DD} and $\overline{OEA}$ to GND results in nap mode with the outputs at high impedance. Connecting SHDNA to V_{DD} and $\overline{OEA}$ to V_{DD} results in sleep mode with the outputs at high impedance.

MODE (Pin 60): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Note that MODE controls both channels. Connecting MODE to GND selects offset binary output format and turns the clock duty cycle stabilizer off. 1/3 V_{DD} selects offset binary output format and turns the clock duty cycle stabilizer on. 2/3 V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer on. V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer off.

V_{CMA} (Pin 61): Channel A 1.5V Output and Input Common Mode Bias. Bypass to ground with 2.2µF ceramic chip capacitor. Do not connect to V_{CMB}.

SENSEA (Pin 62): Channel A Reference Programming Pin. Connecting SENSEA to V_{CMA} selects the internal reference and a ±0.5V input range. V_{DD} selects the internal reference and a ±1V input range. An external reference greater than 0.5V and less than 1V applied to SENSEA selects an input range of $\pm V_{SENSEA}$. ±1V is the largest valid input range.

GND (Exposed Pad) (Pin 65): ADC Power Ground. The Exposed Pad on the bottom of the package needs to be soldered to ground.

FUNCTIONAL BLOCK DIAGRAM

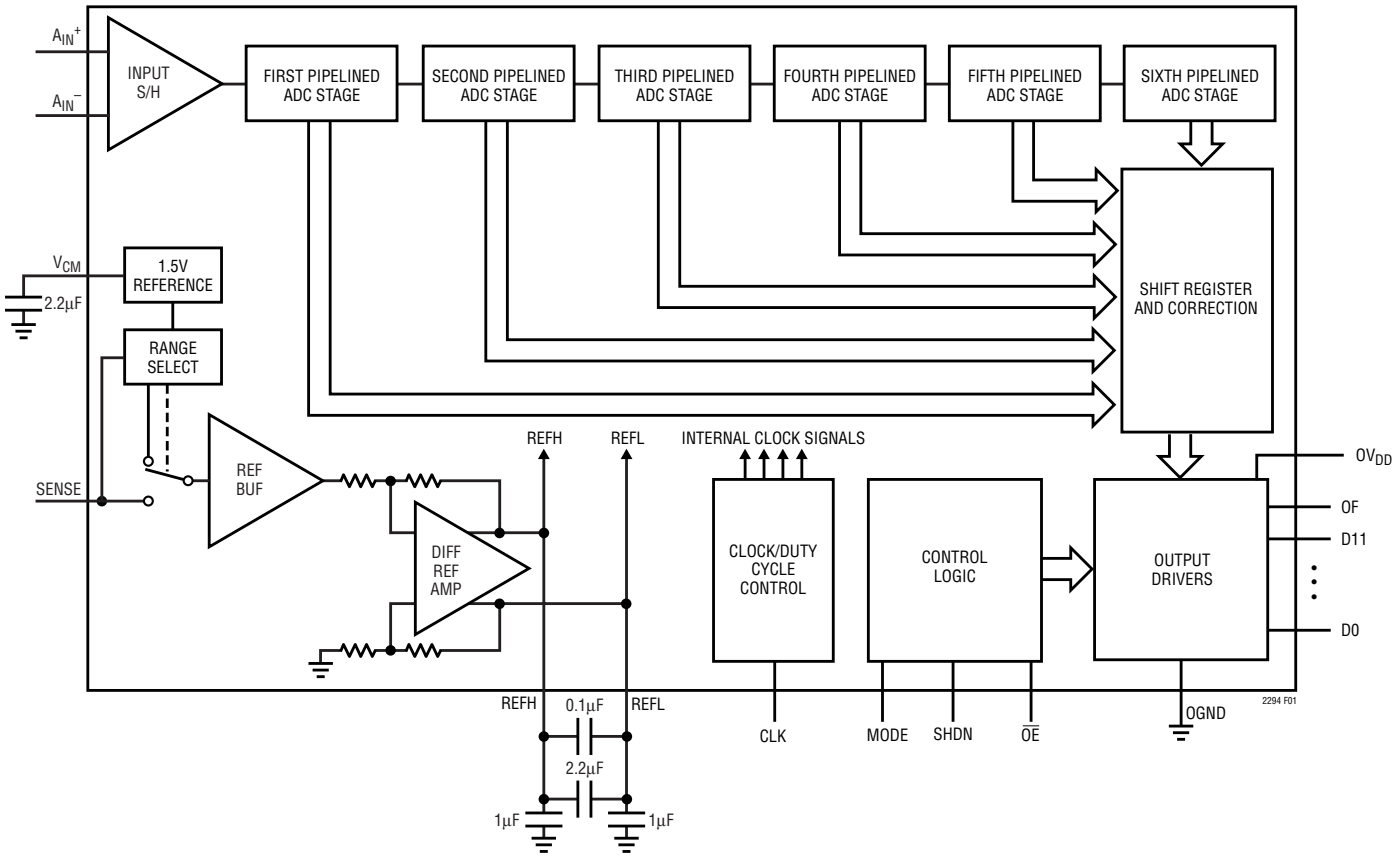
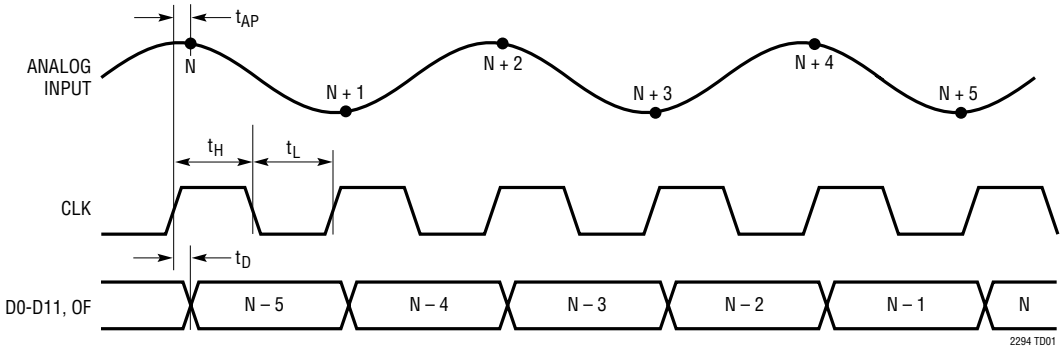


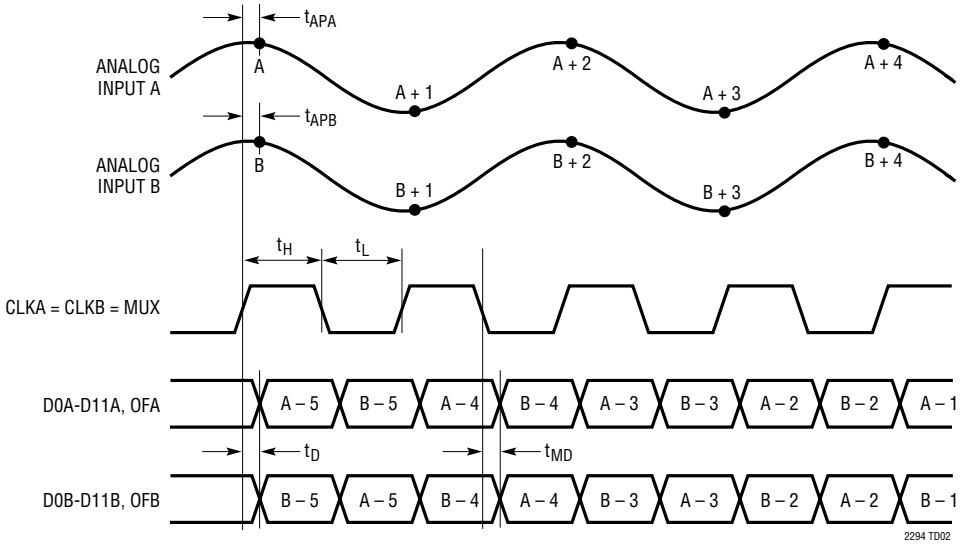
Figure 1. Functional Block Diagram (Only One Channel is Shown)

TIMING DIAGRAMS

Dual Digital Output Bus Timing
(Only One Channel is Shown)



Multiplexed Digital Output Bus Timing



APPLICATIONS INFORMATION

DYNAMIC PERFORMANCE

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20Log\left(\sqrt{(V2^2 + V3^2 + V4^2 + \ldots Vn^2)}/V1\right)$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. The THD calculated in this data sheet uses all the harmonics up to the fifth.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. The 3rd order intermodulation products are 2fa + fb, 2fb + fa, 2fa – fb and 2fb – fa. The intermodulation distortion is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order intermodulation product.

Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is the peak harmonic or spurious noise that is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Input Bandwidth

The input bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

Aperture Delay Time

The time from when CLK reaches midsupply to the instant that the input signal is held by the sample and hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20log\ (2\pi \bullet f_{IN} \bullet t_{JITTER})$$

Crosstalk

Crosstalk is the coupling from one channel (being driven by a full-scale signal) onto the other channel (being driven by a –1dBFS signal).

CONVERTER OPERATION

As shown in Figure 1, the LTC2294 is a dual CMOS pipelined multistep converter. The converter has six pipelined ADC stages; a sampled analog input will result in a digitized value five cycles later (see the Timing Diagram section). For optimal AC performance the analog inputs should be driven differentially. For cost sensitive

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applications, the analog inputs can be driven single-ended with slightly worse harmonic distortion. The CLK input is single-ended. The LTC2294 has two phases of operation, determined by the state of the CLK input pin.

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage residue amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when the odd stages are outputting their residue, the even stages are acquiring that residue and vice versa.

When CLK is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the "Input S/H" shown in the block diagram. At the instant that CLK transitions from low to high, the sampled input is held. While CLK is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H during this high phase of CLK. When CLK goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When CLK goes back high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third, fourth and fifth stages, resulting in a fifth stage residue that is sent to the sixth stage ADC for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally synchronized such that the results can be properly combined in the correction logic before being sent to the output buffer.

SAMPLE/HOLD OPERATION AND INPUT DRIVE

Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC2294 CMOS differential sample-and-hold. The analog inputs are connected to the sampling capacitors (C_{SAMPLE}) through NMOS transistors. The capacitors shown attached to each input ($C_{PARASITIC}$) are the summation of all other capacitance associated with each input.

During the sample phase when CLK is low, the transistors connect the analog inputs to the sampling capacitors and they charge to and track the differential input voltage. When CLK transitions from low to high, the sampled input voltage is held on the sampling capacitors. During the hold phase when CLK is high, the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As CLK transitions from high to low, the inputs are reconnected to the sampling

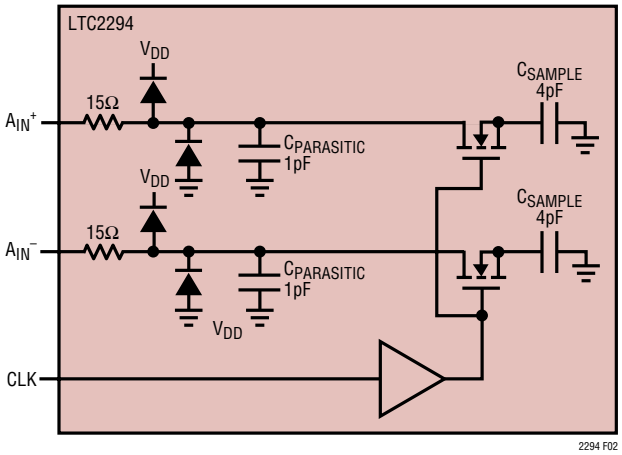

Figure 2. Equivalent Input Circuit

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capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time. If the change between the last sample and the new sample is small, the charging glitch seen at the input will be small. If the input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

Single-Ended Input

For cost sensitive applications, the analog inputs can be driven single-ended. With a single-ended input the harmonic distortion and INL will degrade, but the SNR and DNL will remain unchanged. For a single-ended input, A_{IN}^+ should be driven with the input signal and A_{IN}^- should be connected to 1.5V or V_{CM}.

Common Mode Bias

For optimal performance the analog inputs should be driven differentially. Each input should swing ±0.5V for the 2V range or ±0.25V for the 1V range, around a common mode voltage of 1.5V. The V_{CM} output pin may be used to provide the common mode bias level. V_{CM} can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp differential driver circuit. The V_{CM} pin must be bypassed to ground close to the ADC with a 2.2µF or greater capacitor.

Input Drive Impedance

As with all high performance, high speed ADCs, the dynamic performance of the LTC2294 can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and reactance can influence SFDR. At the falling edge of CLK, the sample-and-hold circuit will connect the 4pF sampling capacitor to the input pin and start the sampling period. The sampling period ends when CLK rises, holding the sampled input on the sampling capacitor. Ideally the input circuitry should be fast enough to fully charge the sampling capacitor during the sampling period $1/(2F_{ENCODE})$; however, this is not always possible and the incomplete settling may degrade the SFDR. The sampling glitch has been designed to be as linear as possible to minimize the effects of incomplete settling.

For the best performance, it is recommended to have a source impedance of 100Ω or less for each input. The source impedance should be matched for the differential inputs. Poor matching will result in higher even order harmonics, especially the second.

Input Drive Circuits

Figure 3 shows the LTC2294 being driven by an RF transformer with a center tapped secondary. The secondary center tap is DC biased with V_{CM}, setting the ADC input signal at its optimum DC level. Terminating on the transformer secondary is desirable, as this provides a common mode path for charging glitches caused by the sample and hold. Figure 3 shows a 1:1 turns ratio transformer. Other turns ratios can be used if the source impedance seen by the ADC does not exceed 100Ω for each ADC input. A disadvantage of using a transformer is the loss of low frequency response. Most small RF transformers have poor performance at frequencies below 1MHz.

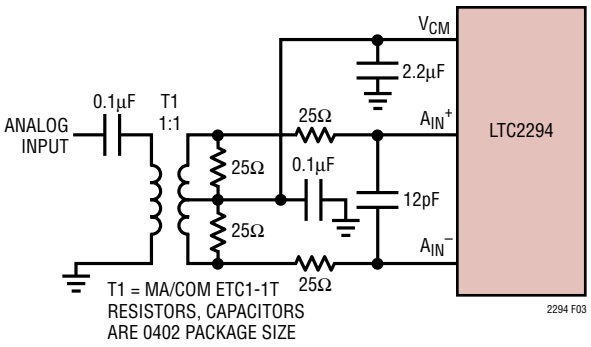

Figure 3. Single-Ended to Differential Conversion Using a Transformer

Figure 4 demonstrates the use of a differential amplifier to convert a single ended input signal into a differential input signal. The advantage of this method is that it provides low frequency input response; however, the limited gain bandwidth of most op amps will limit the SFDR at high input frequencies.

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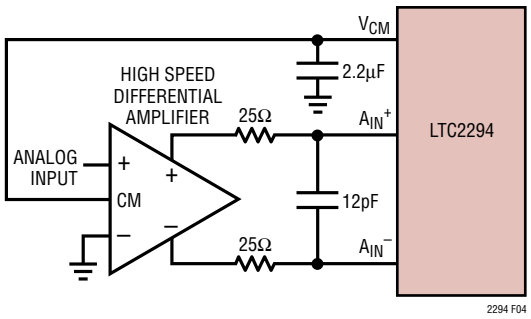

Figure 4. Differential Drive with an Amplifier

Figure 5 shows a single-ended input circuit. The impedance seen by the analog inputs should be matched. This circuit is not recommended if low distortion is required.

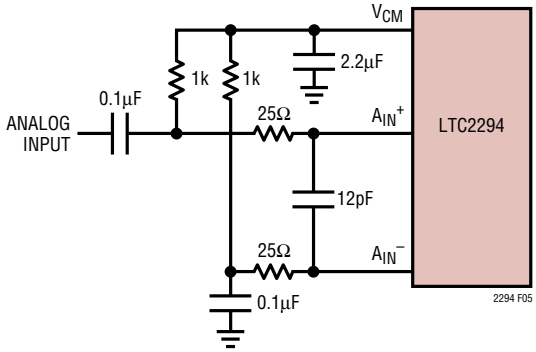

Figure 5. Single-Ended Drive

The 25Ω resistors and 12pF capacitor on the analog inputs serve two purposes: isolating the drive circuitry from the sample-and-hold charging glitches and limiting the wideband noise at the converter input.

For input frequencies above 70MHz, the input circuits of Figure 6, 7 and 8 are recommended. The balun transformer gives better high frequency response than a flux coupled center tapped transformer. The coupling capacitors allow the analog inputs to be DC biased at 1.5V. In Figure 8, the series inductors are impedance matching elements that maximize the ADC bandwidth.

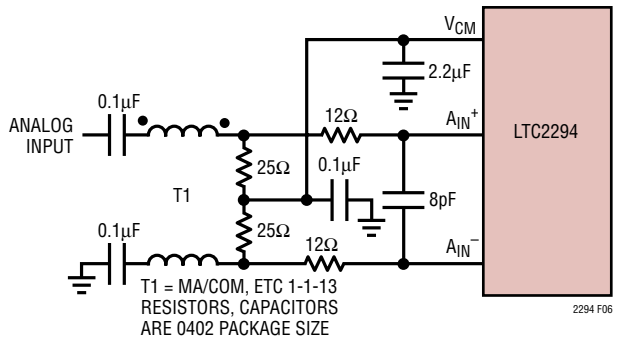

Figure 6. Recommended Front End Circuit for Input Frequencies Between 70MHz and 170MHz

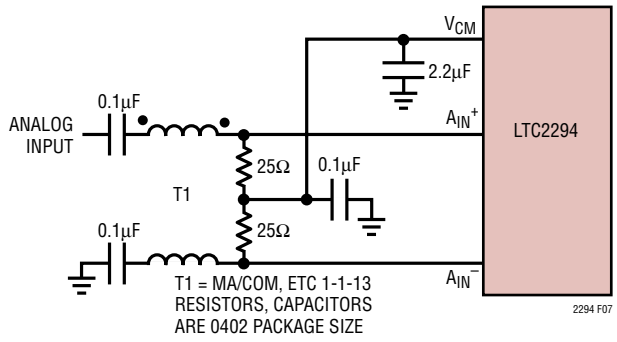

Figure 7. Recommended Front End Circuit for Input Frequencies Between 170MHz and 300MHz

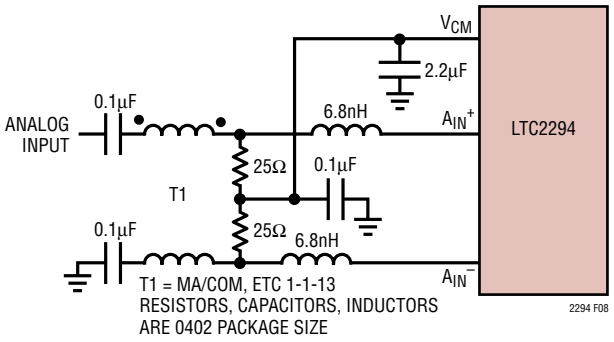

Figure 8. Recommended Front End Circuit for Input Frequencies Above 300MHz

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Reference Operation

Figure 9 shows the LTC2294 reference circuitry consisting of a 1.5V bandgap reference, a difference amplifier and switching and control circuit. The internal voltage reference can be configured for two pin selectable input ranges of 2V (±1V differential) or 1V (±0.5V differential). Tying the SENSE pin to V_{DD} selects the 2V range; tying the SENSE pin to V_{CM} selects the 1V range.

The 1.5V bandgap reference serves two functions: its output provides a DC bias point for setting the common mode voltage of any external input circuitry; additionally, the reference is used with a difference amplifier to generate the differential reference levels needed by the internal ADC circuitry. An external bypass capacitor is required for the 1.5V reference output, V_{CM}. This provides a high frequency low impedance path to ground for internal and external circuitry.

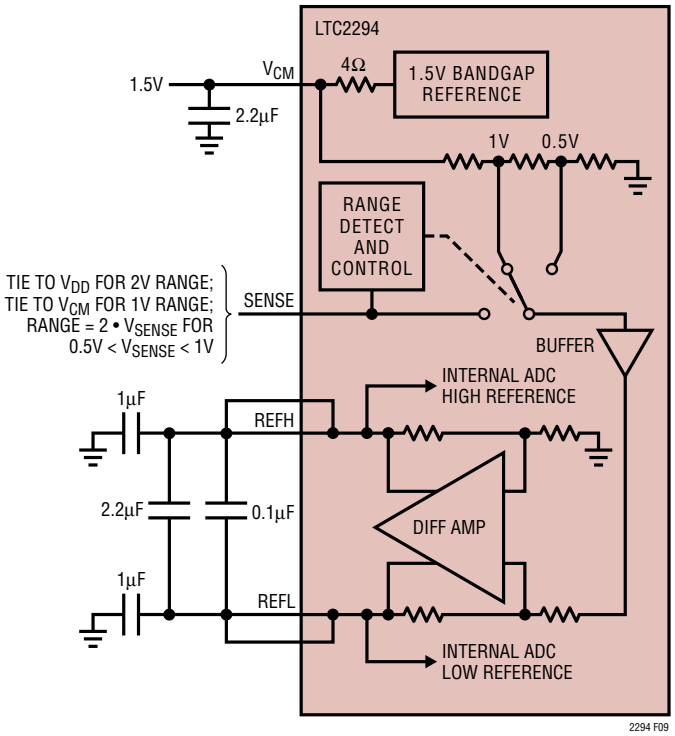

Figure 9. Equivalent Reference Circuit

The difference amplifier generates the high and low reference for the ADC. High speed switching circuits are connected to these outputs and they must be externally bypassed. Each output has two pins. The multiple output pins are needed to reduce package inductance. Bypass capacitors must be connected as shown in Figure 9. Each ADC channel has an independent reference with its own bypass capacitors. The two channels can be used with the same or different input ranges.

Other voltage ranges between the pin selectable ranges can be programmed with two external resistors as shown in Figure 10. An external reference can be used by applying its output directly or through a resistor divider to SENSE. It is not recommended to drive the SENSE pin with a logic device. The SENSE pin should be tied to the appropriate level as close to the converter as possible. If the SENSE pin is driven externally, it should be bypassed to ground as close to the device as possible with a 1µF ceramic capacitor. For the best channel matching, connect an external reference to SENSEA and SENSEB.

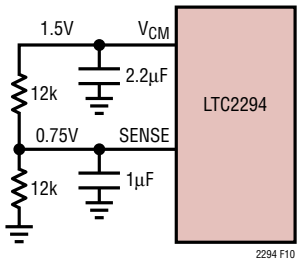

Figure 10. 1.5V Range ADC

Input Range

The input range can be set based on the application. The 2V input range will provide the best signal-to-noise performance while maintaining excellent SFDR. The 1V input range will have better SFDR performance, but the SNR will degrade by 4dB. See the Typical Performance Characteristics section.

Driving the Clock Input

The CLK inputs can be driven directly with a CMOS or TTL level signal. A sinusoidal clock can also be used along with a low jitter squaring circuit before the CLK pin (Figure 11).

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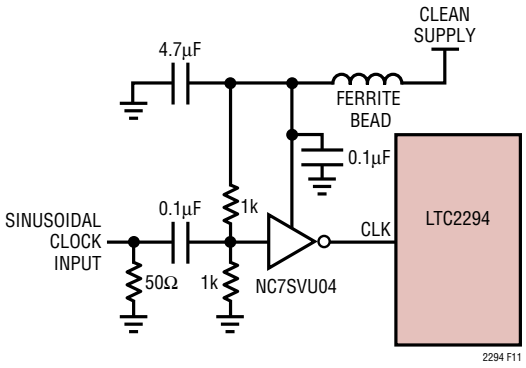
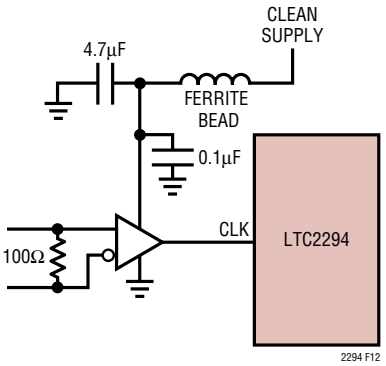


Figure 11. Sinusoidal Single-Ended CLK Drive



IF LVDS USE FIN1002 OR FIN1018.
FOR PECL, USE AZ1000ELT21 OR SIMILAR

Figure 12. CLK Drive Using an LVDS or PECL to CMOS Converter

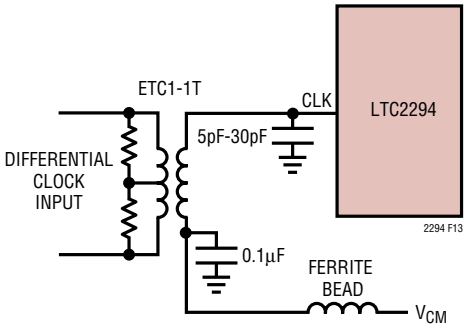


Figure 13. LVDS or PECL CLK Drive Using a Transformer

The noise performance of the LTC2294 can depend on the clock signal quality as much as on the analog input. Any noise present on the clock signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical, such as when digitizing high input frequencies, use as large an amplitude as possible. Also, if the ADC is clocked with a sinusoidal signal, filter the CLK signal to reduce wideband noise and distortion products generated by the source.

It is recommended that CLKA and CLKB are shorted together and driven by the same clock source. If a small time delay is desired between when the two channels sample the analog inputs, CLKA and CLKB can be driven by two different signals. If this delay exceeds 1ns, the performance of the part may degrade. CLKA and CLKB should not be driven by asynchronous signals.

Figures 12 and 13 show alternatives for converting a differential clock to the single-ended CLK input. The use of a transformer provides no incremental contribution to phase noise. The LVDS or PECL to CMOS translators provide little degradation below 70MHz, but at 140MHz will degrade the SNR compared to the transformer solution. The nature of the received signals also has a large bearing on how much SNR degradation will be experienced. For high crest factor signals such as WCDMA or OFDM, where the nominal power level must be at least 6dB to 8dB below full scale, the use of these translators will have a lesser impact.

The transformer in the example may be terminated with the appropriate termination for the signaling in use. The use of a transformer with a 1:4 impedance ratio may be desirable in cases where lower voltage differential signals are considered. The center tap may be bypassed to ground through a capacitor close to the ADC if the differential signals originate on a different plane. The use of a capacitor at the input may result in peaking, and depending on transmission line length may require a 10Ω to 20Ω ohm series resistor to act as both a low pass filter for high frequency noise that may be induced into the clock line by neighboring digital signals, as well as a damping mechanism for reflections.

Maximum and Minimum Conversion Rates

The maximum conversion rate for the LTC2294 is 80Msps. For the ADC to operate properly, the CLK signal should have a 50% (±5%) duty cycle. Each half cycle must have

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at least 5.9ns for the ADC internal circuitry to have enough settling time for proper operation.

An optional clock duty cycle stabilizer circuit can be used if the input clock has a non 50% duty cycle. This circuit uses the rising edge of the CLK pin to sample the analog input. The falling edge of CLK is ignored and the internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 40% to 60% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require a hundred clock cycles for the PLL to lock onto the input clock. To use the clock duty cycle stabilizer, the MODE pin should be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors. The MODE pin controls both Channel A and Channel B—the duty cycle stabilizer is either on or off for both channels.

The lower limit of the LTC2294 sample rate is determined by droop of the sample-and-hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTC2294 is 1Msps.

DIGITAL OUTPUTS

Table 1 shows the relationship between the analog input voltage, the digital data bits, and the overflow bit.

Table 1. Output Codes vs Input Voltage

$A_{IN}^+ - A_{IN}^-$ (2V RANGE)	OF	D11 – D0 (OFFSET BINARY)	D11 – D0 (2's COMPLEMENT)
>+1.000000V	1	1111 1111 1111	0111 1111 1111
+0.999512V	0	1111 1111 1111	0111 1111 1111
+0.999024V	0	1111 1111 1110	0111 1111 1110
+0.000488V	0	1000 0000 0001	0000 0000 0001
0.000000V	0	1000 0000 0000	0000 0000 0000
–0.000488V	0	0111 1111 1111	1111 1111 1111
–0.000976V	0	0111 1111 1110	1111 1111 1110
–0.999512V	0	0000 0000 0001	1000 0000 0001
–1.000000V	0	0000 0000 0000	1000 0000 0000
<–1.000000V	1	0000 0000 0000	1000 0000 0000

Digital Output Buffers

Figure 14 shows an equivalent circuit for a single output buffer. Each buffer is powered by OV_{DD} and OGND, isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and may eliminate the need for external damping resistors.

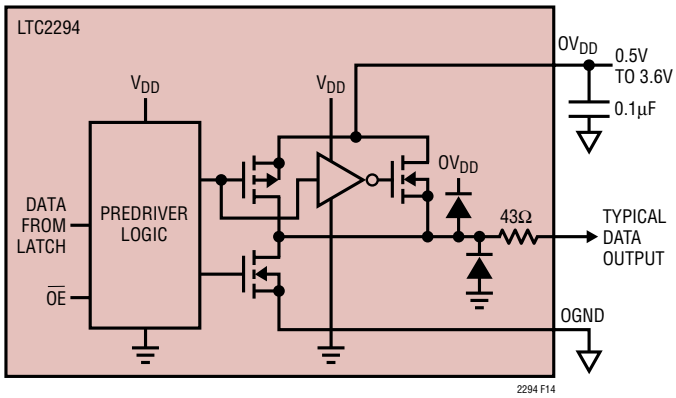

Figure 14. Digital Output Buffer

As with all high speed/high resolution converters, the digital output loading can affect the performance. The digital outputs of the LTC2294 should drive a minimal capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. The output should be buffered with a device such as an ALVCH16373 CMOS latch. For full speed operation the capacitive load should be kept under 10pF.

Lower OV_{DD} voltages will also help reduce interference from the digital outputs.

Data Format

Using the MODE pin, the LTC2294 parallel digital output can be selected for offset binary or 2's complement format. Note that MODE controls both Channel A and Channel B. Connecting MODE to GND or $1/3V_{DD}$ selects

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offset binary output format. Connecting MODE to $2/3V_{DD}$ or V_{DD} selects 2's complement output format. An external resistor divider can be used to set the $1/3V_{DD}$ or $2/3V_{DD}$ logic values. Table 2 shows the logic states for the MODE pin.

Table 2. MODE Pin Function

MODE PIN	OUTPUT FORMAN	CLOCK DUTY CYCLE STABILIZER
0	Offset Binary	Off
$1/3V_{DD}$	Offset Binary	On
$2/3V_{DD}$	2's Complement	On
V_{DD}	2's Complement	Off

Overflow Bit

When OF outputs a logic high the converter is either overranged or underranged.

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD}, should be tied to the same power supply as for the logic being driven. For example, if the converter is driving a DSP powered by a 1.8V supply, then OV_{DD} should be tied to that same 1.8V supply.

OV_{DD} can be powered with any voltage from 500mV up to 3.6V. OGND can be powered with any voltage from GND up to 1V and must be less than OV_{DD}. The logic outputs will swing between OGND and OV_{DD}.

Output Enable

The outputs may be disabled with the output enable pin, $\overline{OE}$. $\overline{OE}$ high disables all data outputs including OF. The data access and bus relinquish times are too slow to allow the outputs to be enabled and disabled during full speed operation. The output Hi-Z state is intended for use during long periods of inactivity. Channels A and B have independent output enable pins ($\overline{OEA}$, $\overline{OEB}$).

Sleep and Nap Modes

The converter may be placed in shutdown or nap modes to conserve power. Connecting SHDN to GND results in normal operation. Connecting SHDN to V_{DD} and $\overline{OE}$ to V_{DD} results in sleep mode, which powers down all circuitry including the reference and typically dissipates 1mW. When exiting sleep mode it will take milliseconds for the output data to become valid because the reference capacitors have to recharge and stabilize. Connecting SHDN to V_{DD} and $\overline{OE}$ to GND results in nap mode, which typically dissipates 30mW. In nap mode, the on-chip reference circuit is kept on, so that recovery from nap mode is faster than that from sleep mode, typically taking 100 clock cycles. In both sleep and nap modes, all digital outputs are disabled and enter the Hi-Z state.

Channels A and B have independent SHDN pins (SHDNA, SHDNB). Channel A is controlled by SHDNA and $\overline{OEA}$, and Channel B is controlled by SHDNB and $\overline{OEB}$. The nap, sleep and output enable modes of the two channels are completely independent, so it is possible to have one channel operating while the other channel is in nap or sleep mode.

Digital Output Multiplexer

The digital outputs of the LTC2294 can be multiplexed onto a single data bus. The MUX pin is a digital input that swaps the two data busses. If MUX is High, Channel A comes out on DA0-DA11, OFA; Channel B comes out on DB0-DB11, OFB. If MUX is Low, the output busses are swapped and Channel A comes out on DB0-DB11, OFB; Channel B comes out on DA0-DA11, OFA. To multiplex both channels onto a single output bus, connect MUX, CLKA and CLKB together (see the Timing Diagram for the multiplexed mode). The multiplexed data is available on either data bus—the unused data bus can be disabled with its $\overline{OE}$ pin.

Grounding and Bypassing

The LTC2294 requires a printed circuit board with a clean, unbroken ground plane. A multilayer board with an internal ground plane is recommended. Layout for the printed

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circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, OV_{DD}, V_{CM}, REFH, and REFL pins. Bypass capacitors must be located as close to the pins as possible. Of particular importance is the 0.1µF capacitor between REFH and REFL. This capacitor should be placed as close to the device as possible (1.5mm or less). A size 0402 ceramic capacitor is recommended. The large 2.2µF capacitor between REFH and REFL can be somewhat further away. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC2294 differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

Heat Transfer

Most of the heat generated by the LTC2294 is transferred from the die through the bottom-side exposed pad and package leads onto the printed circuit board. For good electrical and thermal performance, the exposed pad should be soldered to a large grounded pad on the PC board. It is critical that all ground pins are connected to a ground plane of sufficient area.

Clock Sources for Undersampling

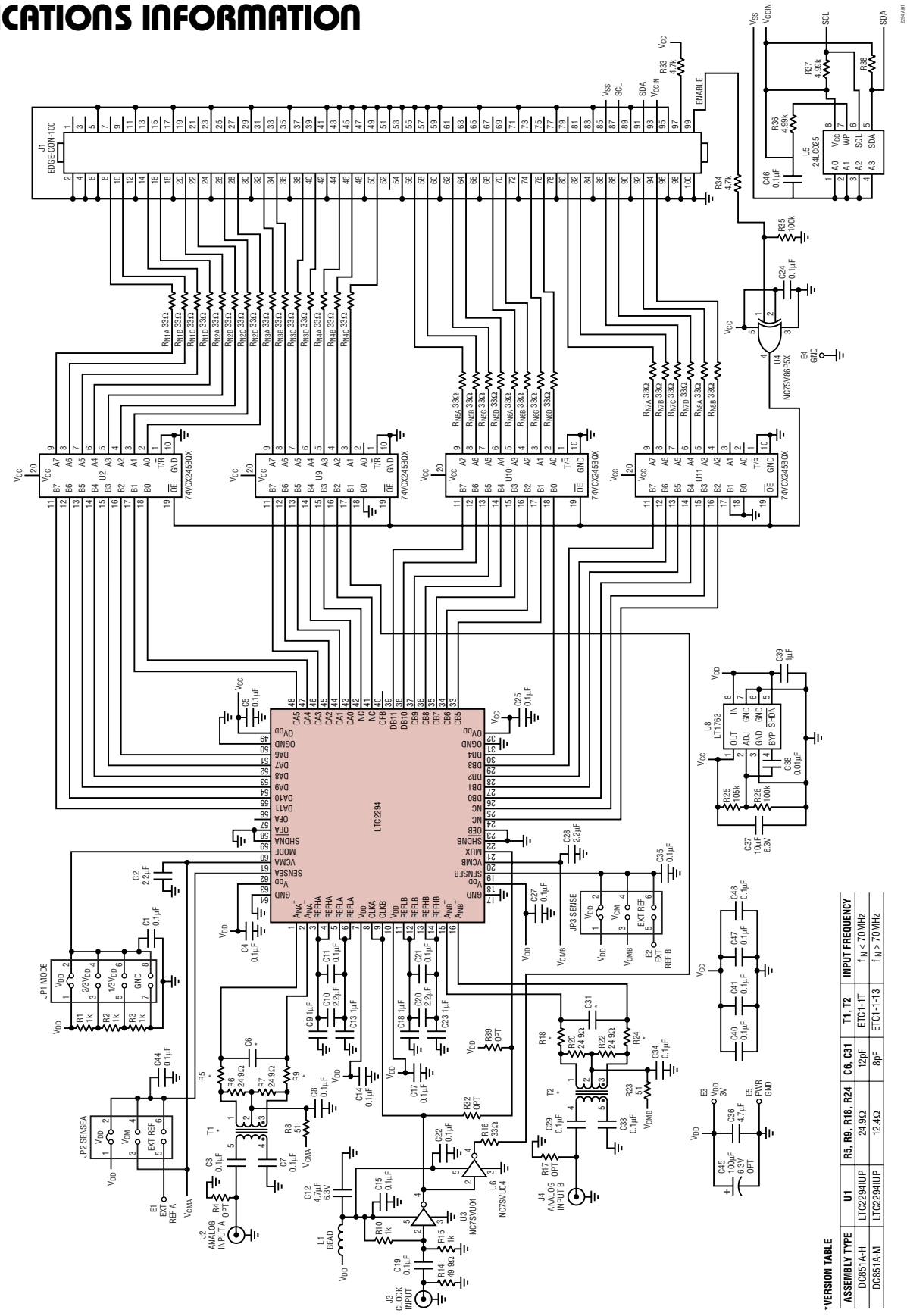
Undersampling raises the bar on the clock source and the higher the input frequency, the greater the sensitivity to clock jitter or phase noise. A clock source that degrades SNR of a full-scale signal by 1dB at 70MHz will degrade SNR by 3dB at 140MHz, and 4.5dB at 190MHz.

In cases where absolute clock frequency accuracy is relatively unimportant and only a single ADC is required, a 3V canned oscillator from vendors such as Saronix or Vectron can be placed close to the ADC and simply connected directly to the ADC. If there is any distance to the ADC, some source termination to reduce ringing that may occur even over a fraction of an inch is advisable. You must not allow the clock to overshoot the supplies or performance will suffer. Do not filter the clock signal with a narrow band filter unless you have a sinusoidal clock source, as the rise and fall time artifacts present in typical digital clock signals will be translated into phase noise.

The lowest phase noise oscillators have single-ended sinusoidal outputs, and for these devices the use of a filter close to the ADC may be beneficial. This filter should be close to the ADC to both reduce roundtrip reflection times, as well as reduce the susceptibility of the traces between the filter and the ADC. If you are sensitive to close-in phase noise, the power supply for oscillators and any buffers must be very stable, or propagation delay variation with supply will translate into phase noise. Even though these clock sources may be regarded as digital devices, do not operate them on a digital supply. If your clock is also used to drive digital devices such as an FPGA, you should locate the oscillator, and any clock fan-out devices close to the ADC, and give the routing to the ADC precedence. The clock signals to the FPGA should have series termination at the source to prevent high frequency noise from the FPGA disturbing the substrate of the clock fan-out device. If you use an FPGA as a programmable divider, you must re-time the signal using the original oscillator, and the re-timing flip-flop as well as the oscillator should be close to the ADC, and powered with a very quiet supply.

For cases where there are multiple ADCs, or where the clock source originates some distance away, differential clock distribution is advisable. This is advisable both from the perspective of EMI, but also to avoid receiving noise from digital sources both radiated, as well as propagated in the waveguides that exist between the layers of multi-layer PCBs. The differential pairs must be close together, and distanced from other signals. The differential pair should be guarded on both sides with copper distanced at least 3x the distance between the traces, and grounded with vias no more than 1/4 inch apart.

APPLICATIONS INFORMATION

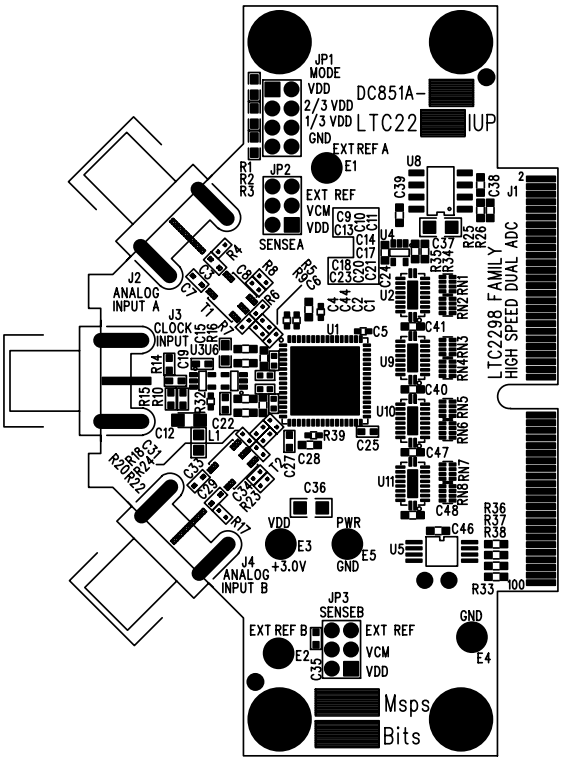


*VERSION TABLE

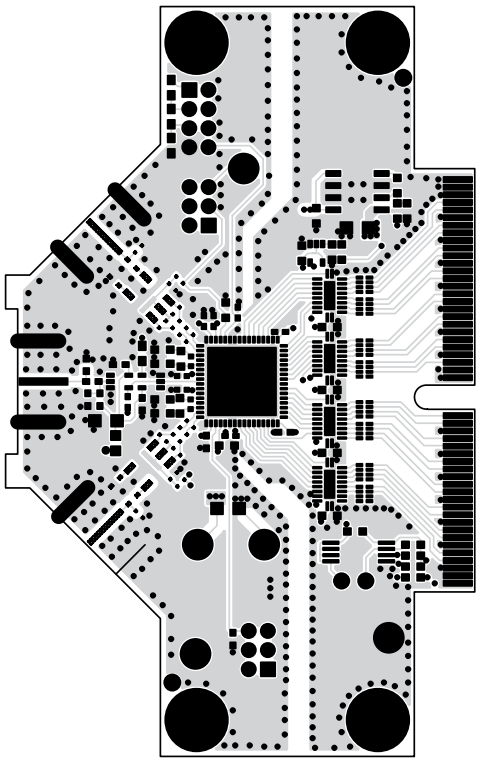
ASSEMBLY TYPE	U1	R5, R9, R18, R24	C6, C31	T1, T2	INPUT FREQUENCY
DC851A-H	LTC2294IUP	24.9Ω	12pF	ETC1-1T	f_{IN} < 70MHz
DC851A-M	LTC2294IUP	12.4Ω	8pF	ETC1-1-13	f_{IN} > 70MHz

APPLICATIONS INFORMATION

Silkscreen Top

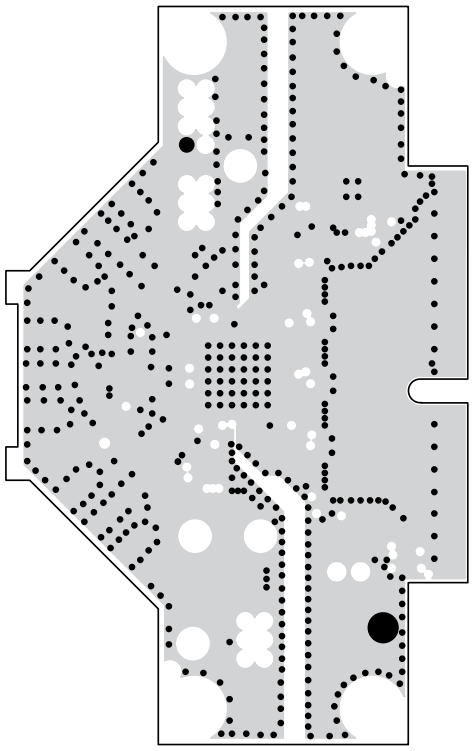


Top Side

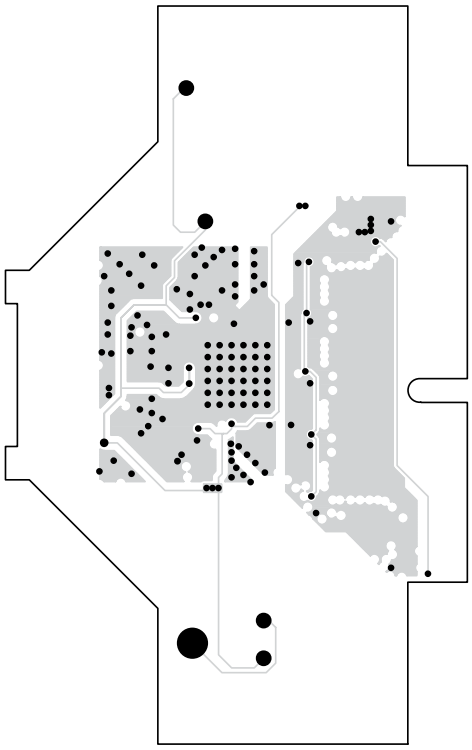


APPLICATIONS INFORMATION

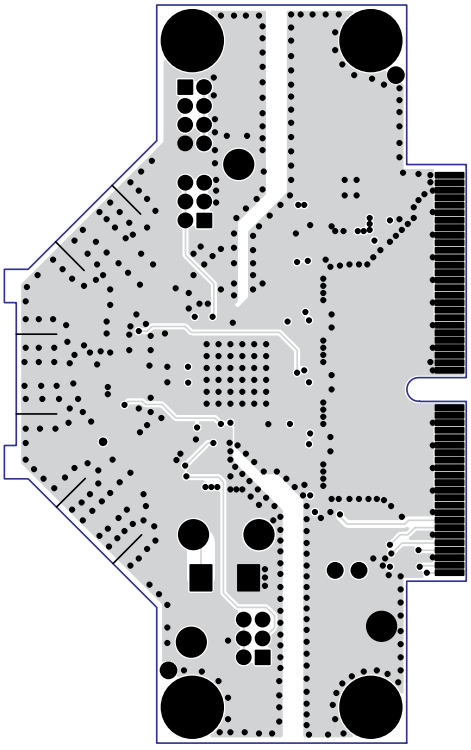
Inner Layer 2 GND



Inner Layer 3 Power

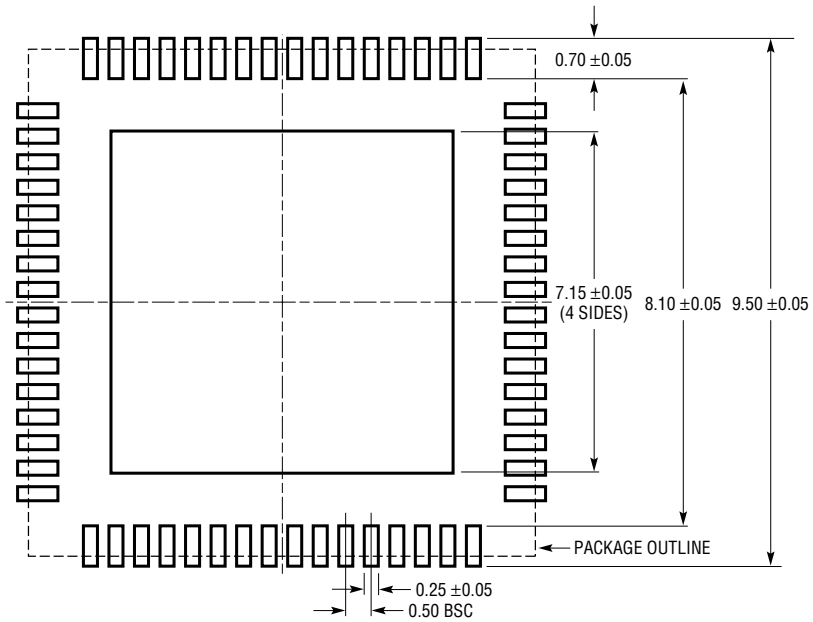


Bottom Side

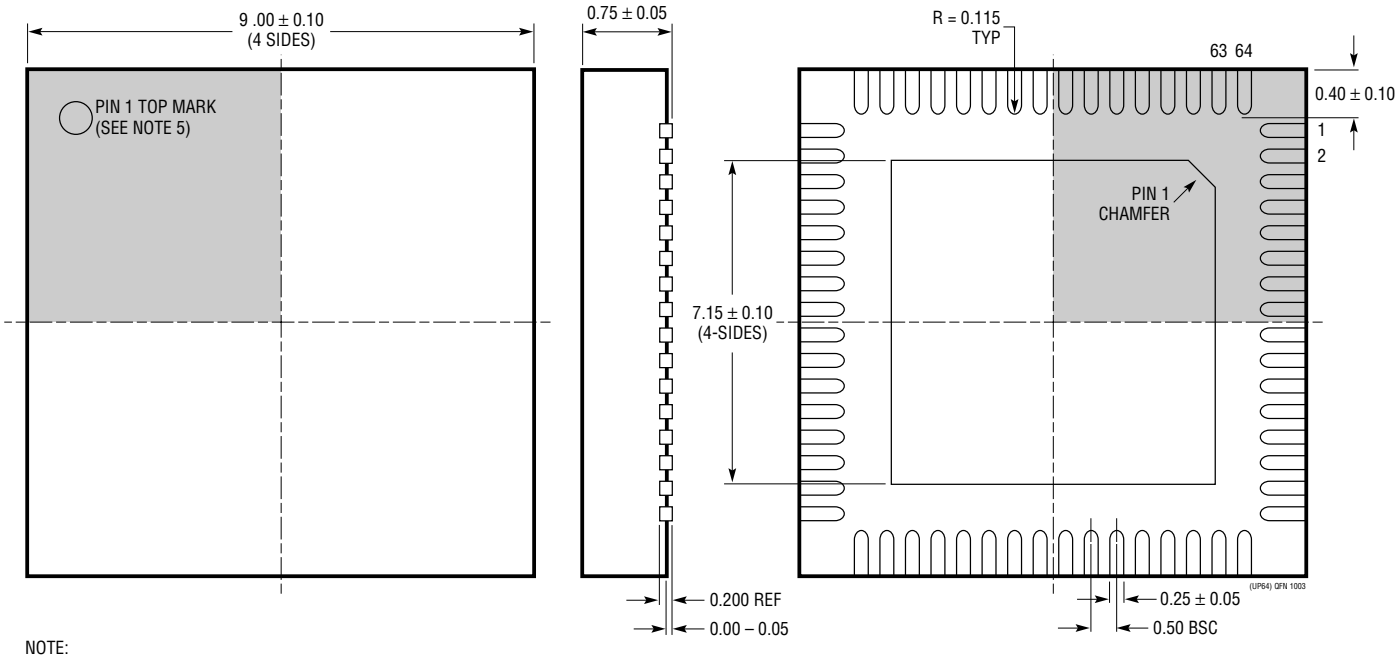


PACKAGE DESCRIPTION

UP Package
64-Lead Plastic QFN (9mm × 9mm)
(Reference LTC DWG # 05-08-1705)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION WNJR-5
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
6. DRAWING NOT TO SCALE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2220	12-Bit, 170Msps ADC	890mW, 67.5dB SNR, 9mm × 9mm QFN Package
LTC2221	12-Bit, 135Msps ADC	630mW, 67.5dB SNR, 9mm × 9mm QFN Package
LTC2222	12-Bit, 105Msps ADC	475mW, 67.9dB SNR, 7mm × 7mm QFN Package
LTC2223	12-Bit, 80Msps ADC	366mW, 68dB SNR, 7mm × 7mm QFN Package
LTC2224	12-Bit, 135Msps ADC	630mW, 67.5dB SNR, 7mm × 7mm QFN Package
LTC2225	12-Bit, 10Msps ADC	60mW, 71.4dB SNR, 5mm × 5mm QFN Package
LTC2226	12-Bit, 25Msps ADC	75mW, 71.4dB SNR, 5mm × 5mm QFN Package
LTC2227	12-Bit, 40Msps ADC	120mW, 71.4dB SNR, 5mm × 5mm QFN Package
LTC2228	12-Bit, 65Msps ADC	205mW, 71.3dB SNR, 5mm × 5mm QFN Package
LTC2230	10-Bit, 170Msps ADC	890mW, 67.5dB SNR, 9mm × 9mm QFN Package
LTC2231	10-Bit, 135Msps ADC	630mW, 67.5dB SNR, 9mm × 9mm QFN Package
LTC2232	10-Bit, 105Msps ADC	475mW, 61.3dB SNR, 7mm × 7mm QFN Package
LTC2233	10-Bit, 80Msps ADC	366mW, 61.3dB SNR, 7mm × 7mm QFN Package
LTC2245	14-Bit, 10Msps ADC	60mW, 74.4dB SNR, 5mm × 5mm QFN Package
LTC2246	14-Bit, 25Msps ADC	75mW, 74.5dB SNR, 5mm × 5mm QFN Package
LTC2247	14-Bit, 40Msps ADC	120mW, 74.4dB SNR, 5mm × 5mm QFN Package
LTC2248	14-Bit, 65Msps ADC	205mW, 74.3dB SNR, 5mm × 5mm QFN Package
LTC2249	14-Bit, 80Msps ADC	222mW, 73dB SNR, 5mm × 5mm QFN Package
LTC2286	10-Bit, Dual, 25Msps ADC	150mW, 61.8dB SNR, 9mm × 9mm QFN Package
LTC2287	10-Bit, Dual, 40Msps ADC	235mW, 61.8dB SNR, 9mm × 9mm QFN Package
LTC2288	10-Bit, Dual, 65Msps ADC	400mW, 61.8dB SNR, 9mm × 9mm QFN Package
LTC2289	10-Bit, Dual, 80Msps ADC	422mW, 61dB SNR, 9mm × 9mm QFN Package
LTC2290	12-Bit, Dual, 10Msps ADC	120mW, 71.3dB SNR, 9mm × 9mm QFN Package
LTC2291	12-Bit, Dual, 25Msps ADC	150mW, 74.5dB SNR, 9mm × 9mm QFN Package
LTC2292	12-Bit, Dual, 40Msps ADC	235mW, 74.4dB SNR, 9mm × 9mm QFN Package
LTC2293	12-Bit, Dual, 65Msps ADC	400mW, 74.3dB SNR, 9mm × 9mm QFN Package
LTC2295	14-Bit, Dual, 10Msps ADC	120mW, 74.4dB SNR, 9mm × 9mm QFN Package
LTC2296	14-Bit, Dual, 25Msps ADC	150mW, 74.5dB SNR, 9mm × 9mm QFN Package
LTC2297	14-Bit, Dual, 40Msps ADC	235mW, 74.4dB SNR, 9mm × 9mm QFN Package
LTC2298	14-Bit, Dual, 65Msps ADC	400mW, 74.3dB SNR, 9mm × 9mm QFN Package
LTC2299	14-Bit, Dual, 80Msps ADC	444mW, 73dB SNR, 9mm × 9mm QFN Package

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