LM26003-xx 3-A Switching Regulator With High Efficiency Sleep Mode

1 Features

- LM26003-Q1 is an Automotive-Grade Product That is AEC-Q100 Grade 1 Qualified (–40°C to +125°C Operating Junction Temperature)
- High-Efficiency Sleep Mode
- 40-µA Typical Iq in Sleep Mode
- 10.8-µA Typical Iq in Shutdown Mode
- 3.0-V Minimum Input Voltage
- 4.0-V to 38-V Continuous Input Range
- 1.5% Reference Accuracy
- Cycle-by-Cycle Current Limit
- Adjustable Frequency (150 kHz to 500 kHz)
- Synchronizable to an External Clock
- Power Good Flag
- Forced PWM Function
- Adjustable Soft-Start
- 20-Pin HTSSOP Package
- Thermal Shut Down

2 Applications

- Automotive Telematics
- Navigation Systems
- In-Dash Instrumentation
- Battery-Powered Applications
- Standby Power for Home Gateways and Set-Top Boxes

3 Description

The LM26003 is a switching regulator designed for the high-efficiency requirements of applications with standby modes. The device features a low-current sleep mode to maintain efficiency under light-load conditions and current-mode control for accurate regulation over a wide input voltage range. Quiescent current is reduced to 10.8 µA typically in shutdown mode and less than 40 µA in sleep mode. Forced PWM mode is also available to disable sleep mode.

The LM26003 device can deliver up to 3 A of continuous load current with a fixed current limit, through the internal N-channel switch. The part has a wide input voltage range of 4.0 V to 38 V and can operate with input voltages as low as 3 V during line transients.

Operating frequency is adjustable from 150 kHz to 500 kHz with a single resistor and can be synchronized to an external clock.

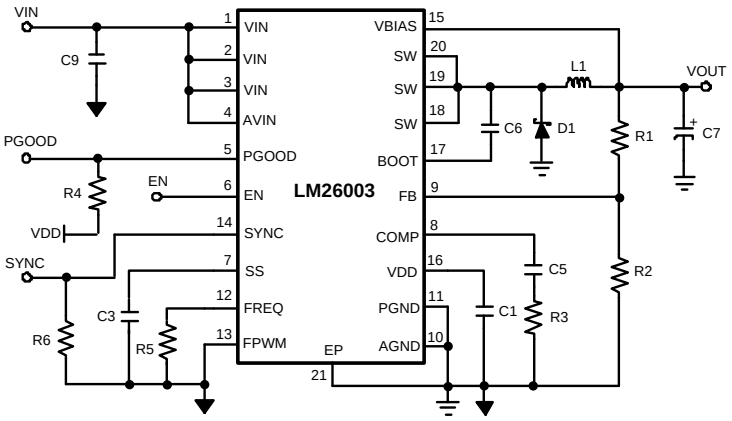
Other features include Power Good, adjustable soft-start, enable pin, input undervoltage protection, and an internal bootstrap diode for reduced component count.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM26003	HTSSOP (20)	6.50 mm x 4.40 mm
LM26003-Q1		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2014) to Revision F — **Page**

- Changed from 0.575V ... 6
- Changed 1.365V ... 6

Changes from Revision D (March 2013) to Revision E — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (March 2013) to Revision D — **Page**

- Changed layout of National Data Sheet to TI format ... 25

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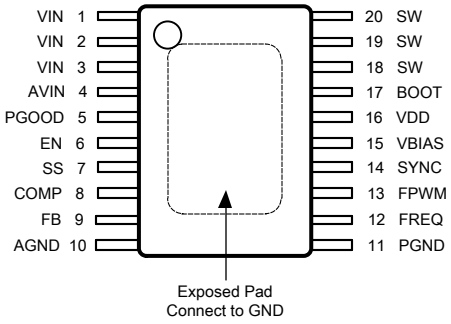
6 Pin Configuration and Functions

20-Pin
TSSOP Package
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	I	Power supply input for high side FET
VIN	2	I	Power supply input for high side FET
VIN	3	I	Power supply input for high side FET
AVIN	4	I	Power supply input for IC supply
PGOOD	5	O	Power Good pin. An open-drain output which goes high when the output voltage is greater than 92% of nominal.
EN	6	I	Enable is an analog level input pin. When pulled below 0.8 V, the device enters shutdown mode.
SS	7	I	Soft-start pin. Connect a capacitor from this pin to GND to set the soft-start time.
COMP	8	I	Compensation pin. Connect to a resistor capacitor pair to compensate the control loop.
FB	9	I	Feedback pin. Connect to a resistor divider between VOUT and GND to set output voltage.
AGND	10	GND	Analog GND as IC reference
PGND	11	GND	Power GND is GND for the switching stage of the regulator
FREQ	12	O	Frequency adjust pin. Connect a resistor from this pin to GND to set the operating frequency.
FPWM	13	I	FPWM is a logic level input pin. For normal operation, connect to GND. When pulled high, sleep mode operation is disabled.
SYNC	14	I	Frequency synchronization pin. Connect to an external clock signal for synchronized operation. SYNC must be pulled low for non-synchronized operation.
VBIAS	15	I	Connect to an external 3-V or greater supply to bypass the internal regulator for improved efficiency. If not used, VBIAS should be tied to GND.
VDD	16	O	The output of the internal regulator. Bypass with a minimum 1.0-µF capacitor.
BOOT	17	I	Bootstrap capacitor pin. Connect a 0.1-µF minimum ceramic capacitor from this pin to SW to generate the gate drive bootstrap voltage.
SW	18	O	Switch pin. The source of the internal N-channel switch.
SW	19	O	Switch pin. The source of the internal N-channel switch.
SW	20	O	Switch pin. The source of the internal N-channel switch.
EP	EP	GND	Exposed Pad thermal connection. Connect to GND.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
Voltages from the indicated pins to GND	VIN	–0.3	40	V
	SW	–1	40	V
	VDD	–0.3	7	V
	VBIAS	–0.3	10	V
	FB	-0.3	7	V
	BOOT	V_{SW}-0.3	V_{SW}+7	V
	PGOOD	–0.3	7	V
	FREQ	–0.3	7	V
	SYNC	–0.3	7	V
	EN	–0.3	40	V
	FPWM	–0.3	7	V
Power Dissipation			3.1	W
Recommended Lead Temperature	Vapor Phase (70s)		215	°C
	Infrared (15s)		220	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

7.2 ESD Ratings: LM26003

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	
		Charged machine model	±200000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings: LM26003-Q1

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 10, 11, and 20)	±1000	
			Other pins	±1000	
		Charged machine model		±200	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.4 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Operating Junction Temperature	−40		125	°C
Supply Voltage	3.0		38	V

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7.5 Thermal Information

THERMAL METRIC[1]		LM26003, LM26003-Q1	UNIT
		PWP	
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	16.5	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	16.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.6 Electrical Characteristics

Unless otherwise stated, Vin = 12 V, T_J = 25°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation.

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
SYSTEM						
I_{SD}[2]	Shutdown Current	EN = 0 V		10.8		µA
		EN = 0 V, –40°C ≤ T_J ≤ 125°C			20	
Iq_{Sleep_VB}[2]	Quiescent Current	Sleep mode, VBIAS = 5 V		40		µA
		Sleep mode, VBIAS = 5 V, –40°C ≤ T_J ≤ 125°C			70	
Iq_{Sleep_VDD}	Quiescent Current	Sleep mode, VBIAS = GND		76		µA
		Sleep mode, VBIAS = GND, –40°C ≤ T_J ≤ 125°C			125	
Iq_{PWM_VB}	Quiescent Current	PWM mode, VBIAS = 5 V FPWM = 2 V		0.16	0.23	mA
Iq_{PWM_VDD}	Quiescent Current	PWM mode, VBIAS = GND FPWM = 2 V		0.65	0.85	mA
I_{BIAS_Sleep}[2]	Bias Current	Sleep mode, VBIAS = 5 V		33		µA
		Sleep mode, VBIAS = 5 V, –40°C ≤ T_J ≤ 125°C			60	
I_{BIAS_PWM}	Bias Current	PWM mode, VBIAS = 5 V		0.5	0.7	mA
V_{FB}	Feedback Voltage	5 V < Vin < 38 V		1.236		V
		5 V < Vin < 38 V, –40°C ≤ T_J ≤ 125°C	1.217		1.255	
I_{FB}	FB Bias Current	VFB = 1.20 V			±200	nA
$\Delta V_{OUT}/\Delta V_{IN}$	Output Voltage Line Regulation	5 V < Vin < 38 V		0.00025		%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output Voltage Load Regulation	0.8 V < V_{COMP} < 1.15 V		0.08		%/A
VDD	VDD Pin Output Voltage	7 V < Vin < 35 V, I_{VDD}= 0 mA to 5 mA		5.99		V
		7 V < Vin < 35 V, I_{VDD}= 0 mA to 5 mA, –40°C ≤ T_J ≤ 125°C	5.50		6.50	
I_{SS_Source}	Soft-start Source Current			2.5		µA
		–40°C ≤ T_J ≤ 125°C	1.5		4.6	
V_{bias_th}	VBIAS On Voltage	Specified at IBIAS = 92.5% of full value	2.64	2.9	3.07	V

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Iq and ISD specify the current into the VIN and AVIN pins. IBIAS is the current into the VBIAS pin when the VBIAS voltage is greater than 3 V. All quiescent current specifications apply to non-switching operation.

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Electrical Characteristics (continued)

Unless otherwise stated, Vin = 12 V, T_J = 25°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
PROTECTION						
I_{LIMPK}	Peak Current Limit			4.7		A
		–40°C ≤ T_J ≤ 125°C	3.15		6.05	
V_{FB_SC}	Short Circuit Frequency Foldback Threshold	Measured at FB falling		0.87		V
F_min_sc	Min Frequency in Foldback	VFB < 0.3 V		45		kHz
V_{TH_PGOOD}	Power Good Threshold	Measured at FB, PGOOD rising		92%		
		Measured at FB, PGOOD rising, –40°C ≤ T_J ≤ 125°C	89%		95%	
	PGOOD Hysteresis		2%	6%	8%	
I_{PGOOD_HI}	PGOOD Leakage Current	PGOOD = 5 V		1.25		nA
R_{DS_PGOOD}	PGOOD On Resistance	PGOOD sink current = 500 µA		150		Ω
V_{UVLO}	Under-voltage Lock-Out Threshold	Vin falling , shutdown, VDD = VIN		2.96		V
		Vin falling , shutdown, VDD = VIN, –40°C ≤ T_J ≤ 125°C	2.70		3.30	
		Vin rising, soft-start, VDD = VIN		3.99		
		Vin rising, soft-start, VDD = VIN, –40°C ≤ T_J ≤ 125°C	3.70		4.30	
TSD	Thermal Shutdown Threshold			160		°C
θ_{JA}	Thermal Resistance	Power dissipation = 1W, 0 lfpm air flow		32		°C/W
LOGIC						
Vth_{EN}	Enable Threshold Voltage	Enable rising		1.18		V
		Enable rising, –40°C ≤ T_J ≤ 125°C	0.8		1.4	
	Enable Hysteresis			180		mV
I_{EN_Source}	EN Source Current	EN = 0 V		4.85		µA
V_{TH_FPWM}	FPWM Threshold			1.24		V
		–40°C ≤ T_J ≤ 125°C	0.8		1.6	
I_{FPWM}	FPWM Leakage Current	FPWM = 5 V		3		nA
EA						
gm	Error Amp Trans-conductance			675		µmho
		–40°C ≤ T_J ≤ 125°C	400		1000	
I_{COMP}	COMP Source Current	VCOMP = 0.9 V		57		µA
	COMP Sink Current	VCOMP = 0.9 V		57		µA
V_{COMP}	COMP Pin Voltage Range		0.64		1.27	V

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7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(ON)}$	Switch On Resistance	Isw = 2A		0.095		Ω
		Isw = 2A, –40°C ≤ T_J ≤ 125°C	0.040		0.200	
I_{sw_off}	Switch Off State Leakage Current	Vin = 38 V, VSW = 0 V		0.002		µA
		Vin = 38 V, VSW = 0 V, –40°C ≤ T_J ≤ 125°C			5.0	
f_{sw}	Switching Frequency	RFREQ = 62k, 124k, 240k, –40°C ≤ T_J ≤ 125°C			±10%	
V_{FREQ}	FREQ Voltage			1.0		V
f_{SW} range	Switching Frequency Range	–40°C ≤ T_J ≤ 125°C	150		500	kHz
V_{SYNC}	Sync Pin Threshold	SYNC rising		1.23		V
		SYNC rising, –40°C ≤ T_J ≤ 125°C			1.6	
		SYNC falling		1.10		
		SYNC falling, –40°C ≤ T_J ≤ 125°C	0.8			
	Sync Pin Hysteresis			135		mV
I_{SYNC}	SYNC Leakage Current			2		nA
F_{SYNC_UP}	Upper Frequency Synchronization Range	As compared to nominal f_{SW}, –40°C ≤ T_J ≤ 125°C			+30%	
F_{SYNC_DN}	Lower Frequency Synchronization Range	As compared to nominal f_{SW}, –40°C ≤ T_J ≤ 125°C			–20%	
T_{OFFMIN}	Minimum Off-time			300		ns
T_{ONMIN}	Minimum On-time			190		ns
TH_{SLEEP_HYS}	Sleep Mode Threshold Hysteresis	VFB rising, % of TH_{WAKE}		101.3%		
TH_{WAKE}	Wake Up Threshold	Measured at falling FB, COMP = 0.6 V		1.236		V
I_{BOOT}	BOOT Pin Leakage Current	BOOT = 6 V, SW = GND		0.001		µA
		BOOT = 6 V, SW = GND, –40°C ≤ T_J ≤ 125°C			5.0	

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7.8 Typical Characteristics

Unless otherwise specified the following conditions apply: Vin = 12 V, T_J = 25°C.

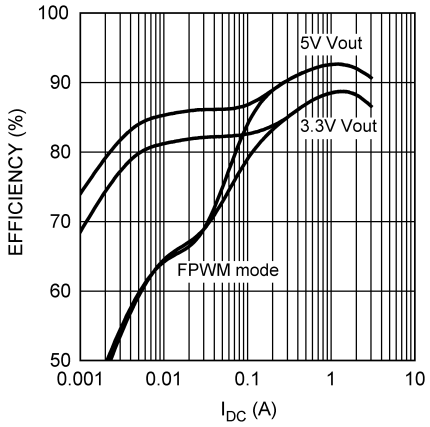

Figure 1. Efficiency vs Load Current (300 kHz)

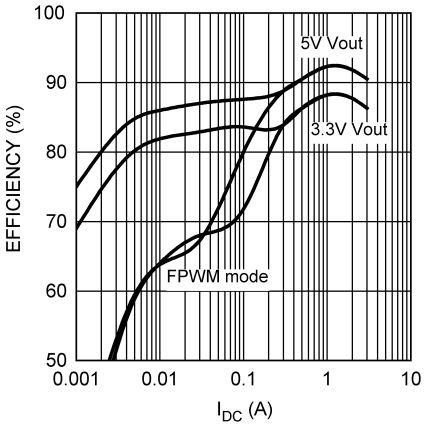

Figure 2. Efficiency vs Load Current (500 kHz)

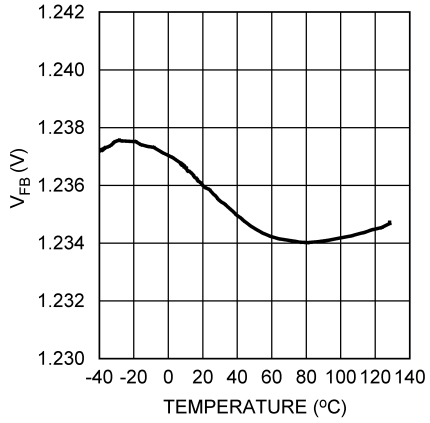

Figure 3. VFB vs Temperature

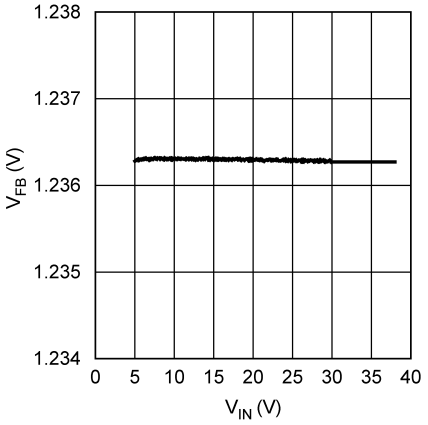

Figure 4. VFB vs Vin (IDC = 300 mA)

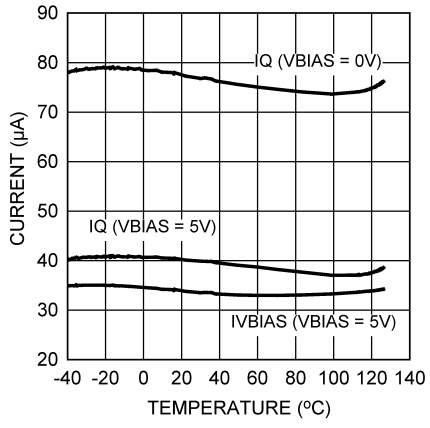

Figure 5. IQ and IVBIAS vs Temperature (Sleep Mode)

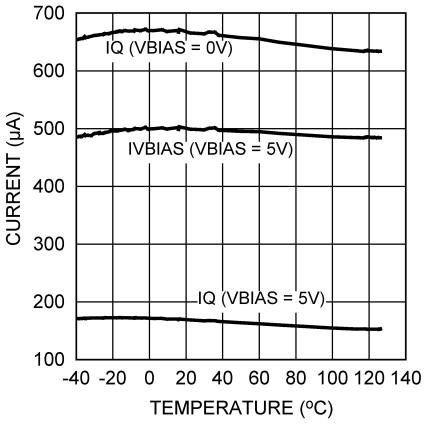

Figure 6. IQ and IVBIAS vs Temperature (PWM Mode)

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Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: Vin = 12 V, T_J = 25°C.

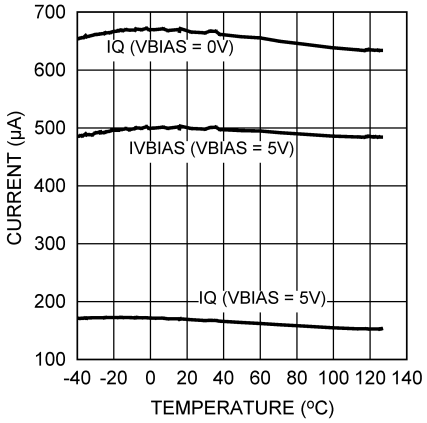


Figure 0. UNDEFINED

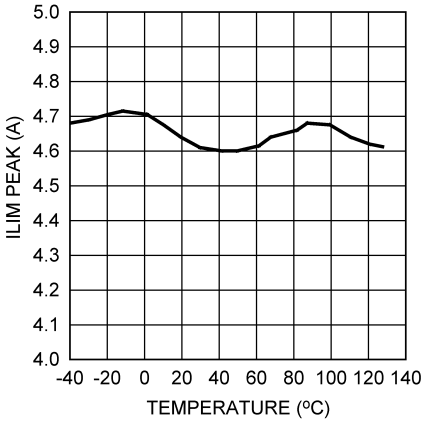


Figure 7. Peak Current Limit vs Temperature

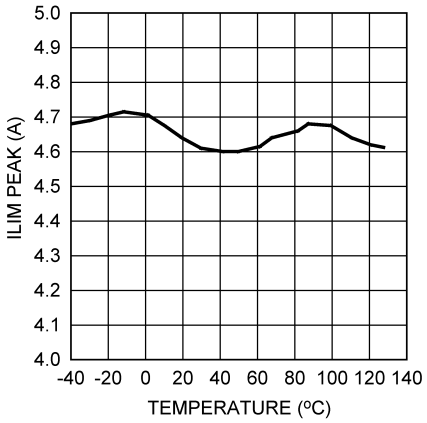


Figure 0. UNDEFINED

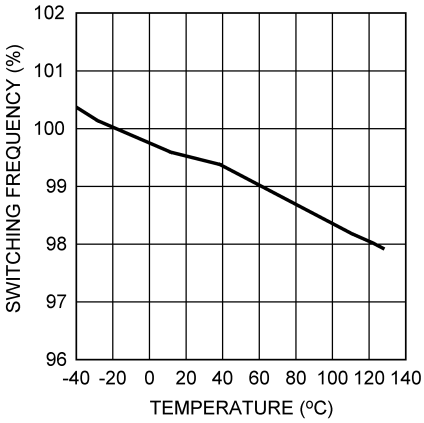


Figure 8. Normalized Switching Frequency vs Temperature (300 kHz)

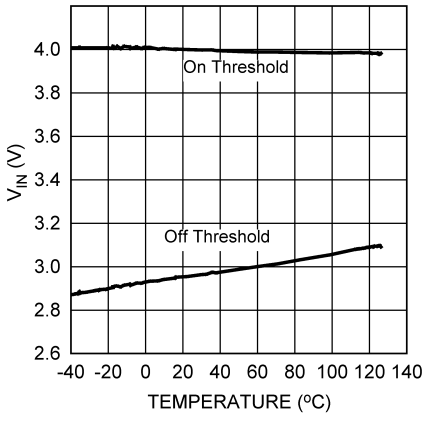


Figure 9. UVLO Threshold vs Temperature (VDD = VIN)

8 Detailed Description

8.1 Overview

The LM26003 device is a current mode PWM buck regulator. At the beginning of each clock cycle, the internal high-side switch turns on, allowing current to ramp-up in the inductor. The inductor current is internally monitored during each switching cycle. A control signal derived from the inductor current is compared to the voltage control signal at the COMP pin, derived from the feedback voltage. When the inductor current reaches its threshold, the high-side switch is turned off and inductor current ramps-down. While the switch is off, inductor current is supplied through the catch diode. This cycle repeats at the next clock cycle. In this way, duty-cycle and output voltage are controlled by regulating inductor current. Current mode control provides superior line and load regulation. Other benefits include cycle-by-cycle current limiting and a simplified compensation scheme. Typical PWM waveforms are shown in Figure 10.

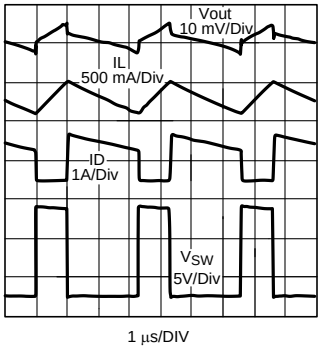
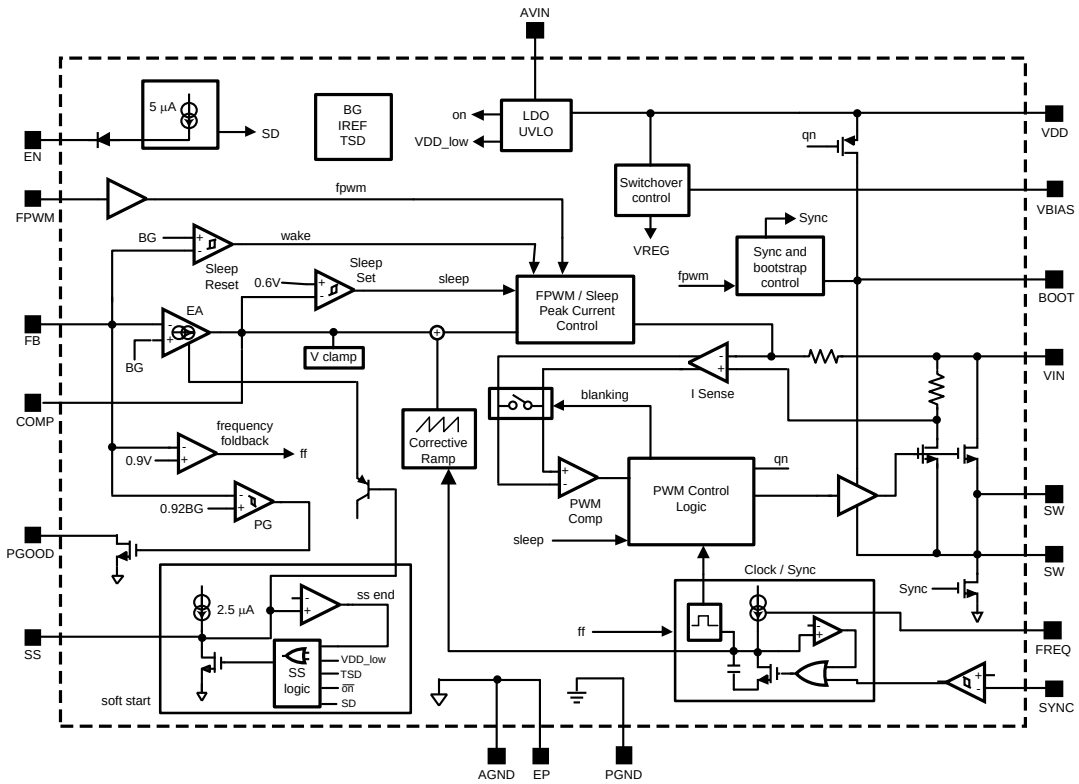


Figure 10. PWM Waveforms 1A-Load, Vin = 12 V

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 FPWM

Pulling the FPWM pin high disables sleep mode and forces the LM26003 device to always operate in PWM mode. Light load efficiency is reduced in PWM mode, but switching frequency remains stable. The FPWM pin can be connected to the VDD pin to pull it high. In FPWM mode, under light load conditions, the regulator operates in discontinuous conduction mode (DCM). In discontinuous conduction mode, current through the inductor starts at zero and ramps-up to its peak, then ramps-down to zero again. Until the next cycle, the inductor current remains at zero. At nominal load currents, in FPWM mode, the device operates in continuous conduction mode, where positive current always flows in the inductor. Typical discontinuous operation waveforms are shown in Figure 11.

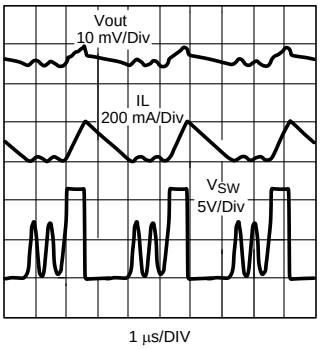

Figure 11. Discontinuous Mode Waveforms 75-mA Load, Vin = 12 V

At very light load, in FPWM mode, the LM26003 device may enter sleep mode. This is to prevent an overvoltage condition from occurring. However, the FPWM sleep threshold is much lower than in normal operation.

8.3.2 Soft-Start

The soft-start feature provides a controlled output voltage ramp-up at startup. This reduces inrush current and eliminates output overshoot at turn-on. The soft-start pin, SS, must be connected to GND through a capacitor. At power-on, enable, or UVLO recovery, an internal 2.5-µA (typical) current charges the soft-start capacitor. During soft-start, the error amplifier output voltage is controlled by both the soft-start voltage and the feedback loop. As the SS pin voltage ramps-up, the duty-cycle increases proportional to the soft-start ramp, causing the output voltage to ramp-up. The rate at which the duty-cycle increases depends on the capacitance of the soft-start capacitor. The higher the capacitance, the slower the output voltage ramps-up. The soft-start capacitor value can be calculated with the following equation:

$$Css = \frac{Iss \times tss}{1.236V} \quad (1)$$

where

- tss is the desired soft-start time
- Iss is the soft-start source current.

During soft-start, current limit and synchronization remain in effect, while sleep mode and frequency foldback are disabled. Soft-start mode ends when the SS pin voltage reaches 1.23 V typical. At this point, output voltage control is transferred to the FB pin and the SS pin is discharged.

8.3.3 Current Limit

The peak current limit is set internally by directly measuring peak inductor current through the internal switch. To ensure accurate current sensing, AVIN should be bypassed with a minimum 100-nF ceramic capacitor as close as possible to AVIN and GND pins. Also the PVIN pin should be bypassed with at least 2.2 µF to ensure low jitter operation.

When the inductor current reaches the current limit threshold, the internal FET turns off immediately allowing inductor current to ramp-down until the next cycle. This reduction in duty-cycle corresponds to a reduction in output voltage.

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Feature Description (continued)

The current limit comparator is disabled for less than 150 ns at the leading edge for increased immunity to switching noise.

Because the current limit monitors peak inductor current, the DC load current limit threshold varies with inductance and frequency. Assuming a minimum current limit of 3.15 A, maximum load current can be calculated as follows:

$$Iload_{max} = 3.15A - \frac{Iripple}{2} \quad (2)$$

Where Iripple is the peak-to-peak inductor ripple current, calculated as shown below:

$$Iripple = \frac{(Vin - Vout) \times Vout}{fsw \times L \times Vin} \quad (3)$$

To find the worst case (lowest) current limit threshold, use the maximum input voltage and minimum current limit specification.

During high overcurrent conditions, such as output short circuit, the LM26003 device employs frequency foldback as a second level of protection. If the feedback voltage falls below the short circuit threshold of 0.9 V, operating frequency is reduced, thereby reducing average switch current. This is especially helpful in short circuit conditions, when inductor current can rise very high during the minimum on-time. Frequency reduction begins at 20% below the nominal frequency setting. The minimum operating frequency in foldback mode is 45 kHz (typical).

If the FB voltage falls below the frequency foldback threshold during frequency synchronized operation, the SYNC function is disabled. Operating frequency versus FB voltage in short circuit conditions is shown in the *Typical Characteristics* section.

Under conditions where the on-time is close to minimum (less than 200 ns typically), such as high input voltage and high switching frequency, the current limit may not function properly. This is because the current limit circuit cannot reduce the on-time below minimum which prevents entry into frequency foldback mode. There are two ways to ensure proper current limit and foldback operation under high input voltage conditions. First, the operating frequency can be reduced to increase the nominal on-time. Second, the inductor value can be increased to slow the current ramp and reduce the peak overcurrent.

8.3.4 Frequency Adjustment and Synchronization

The switching frequency of the LM26003 device can be adjusted between 150 kHz and 500 kHz using a single external resistor. This resistor is connected from the FREQ pin to ground as shown in the typical application. The resistor value can be calculated with the following empirically derived equation:

$$R_{FREQ} = (6.25 \times 10^{10}) \times f_{SW}^{-1.042} \quad (4)$$

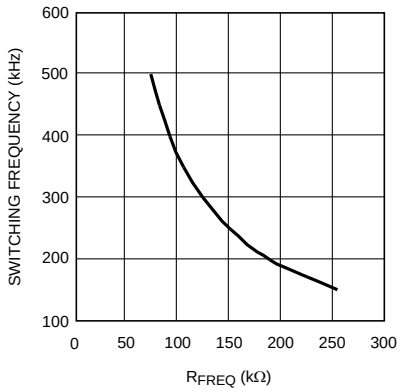

Figure 12. Switching Frequency vs R_{FREQ}

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Feature Description (continued)

The switching frequency can also be synchronized to an external clock signal using the SYNC pin. The SYNC pin allows the operating frequency to be varied above and below the nominal frequency setting. The adjustment range is from 30% above nominal to 20% below nominal. External synchronization requires a 1.23-V minimum (typical) peak signal level at the SYNC pin. The FREQ resistor must always be connected to initialize the nominal operating frequency. The operating frequency is synchronized to the falling edge of the SYNC input. When SYNC goes low, the high-side switch turns on. This allows any duty-cycle to be used for the sync signal when synchronizing to a frequency higher than nominal. When synchronizing to a lower frequency, however, there is a minimum duty-cycle requirement for the SYNC signal, given in the equation below:

$$Sync_Dmin \geq 1 - \frac{f_{sync}}{fnom} \quad (5)$$

where

- fnom is the nominal switching frequency set by the FREQ resistor
- fsync is a square wave.

If the SYNC pin is not used, it must be pulled low for normal operation. A 10 kΩ pulldown resistor is recommended to protect against a missing sync signal. Although the LM26003 device is designed to operate at up to 500 kHz, maximum load current may be limited at higher frequencies due to increased temperature rise. See the *Thermal Considerations and TSD* section.

8.3.5 VBIAS

The VBIAS pin is used to bypass the internal regulator which provides the bias voltage to the LM26003 device. When the VBIAS pin is connected to a voltage greater than 3 V, the internal regulator automatically switches over to the VBIAS input. This reduces the current into VIN (Iq) and increases system efficiency. Using the VBIAS pin has the added benefit of reducing power dissipation within the device.

For most applications where 3 V < Vout < 10 V, VBIAS can be connected to VOUT. If not used, VBIAS should be tied to GND.

If VBIAS drops below 2.9 V (typical), the device automatically switches over to supply the internal bias voltage from Vin.

When the LM26003 device is powered with the circuit's output voltage through VBIAS, especially at low output voltages such as 3.3 V, output ripple noise can couple in through the Vbias pin causing some falling edge jitter on the switch node. To avoid this, additional bypassing close to the VBIAS pin with a low ESR capacitor can be implemented. The circuit diagram in Figure 16 shows this bypass capacitor C8.

8.3.6 Low VIN Operation and UVLO

The LM26003 device is designed to remain operational during short line transients when the input voltage may drop as low as 3.0 V. Minimum nominal operating input voltage is 4.0 V. Below this voltage, switch $R_{DS(ON)}$ increases, due to the lower gate drive voltage from VDD. The minimum voltage required at VDD is approximately 3.5 V for normal operation within specification.

VDD can also be used as a pullup voltage for functions such as PGOOD and FPWM. Note that if VDD is used externally, the pin is not recommended for loads greater than 1 mA.

If the input voltage approaches the nominal output voltage, the duty-cycle is maximized to hold up the output voltage. In this mode of operation, once the duty-cycle reaches its maximum, the LM26003 device can skip a maximum of seven off pulses, effectively increasing the duty-cycle and thus minimizing the dropout from input to output. Typical off-pulse skipping waveforms are shown in Figure 13.

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Feature Description (continued)

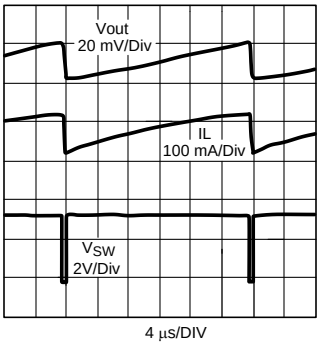

Figure 13. Off-Pulse Skipping Waveforms Vin = 3.5 V, Vnom = 3.3 V, fnom = 305 kHz

UVLO is sensed at both VIN and VDD, and is activated when either voltage falls below 2.96 V (typical). Although VDD is typically less than 200 mV below VIN, it will not discharge through VIN. Therefore when the VIN voltage drops rapidly, VDD may remain high, especially in sleep mode. For fast line voltage transients, using a larger capacitor at the VDD pin can help to hold off a UVLO shutdown by extending the VDD discharge time. By holding up VDD, a larger cap can also reduce the $R_{DS(ON)}$ (and dropout voltage) in low VIN conditions. Alternately, under heavy loading the VDD voltage can fall several hundred mV below VIN. In this case, UVLO may be triggered by VDD even though the VIN voltage is above the UVLO threshold.

When UVLO is activated the LM26003 device enters a standby state in which VDD remains charged. As input voltage and VDD voltage rise above 3.99 V (typical) the device will restart from soft-start mode.

8.3.7 PGOOD

A Power Good pin, PGOOD, is available to monitor the output voltage status. The pin is internally connected to an open-drain MOSFET, which remains open while the output voltage is within operating range. PGOOD goes low (low impedance to ground) when the output falls below 89% of nominal or EN is pulled low. When the output voltage returns to within 95% of nominal, as measured at the FB pin, PGOOD returns to a high state. For improved noise immunity, there is a 5-µs delay between the PGOOD threshold and the PGOOD pin going low.

8.4 Device Functional Modes

The LM26003 device has three basic operation modes: shutdown, sleep or light load operation and full operation. The part enters shutdown mode when the EN pin is pulled low. In this mode, the converter is disabled and the quiescent current is minimized. See the *Enable* section for more details.

The part enters sleep mode when the converter is active (EN high) and the output current is low. Sleep mode is activated as the COMP voltage naturally falls below a typical 0.6 V threshold in light load operation. When operating in sleep mode, the switching events of the converter are reduced in order to lower the current consumption of the system. Forcing the FPWM pin high will prevent sleep mode operation. Refer to *Sleep Mode* for details about operating in Sleep mode as well as entering and exiting sleep mode.

When the part in enabled and the output load is higher, the part will be in full PWM operation. In addition to these normal functioning modes, the LM26003 device has a frequency foldback operating mode which reduces the operating frequency to protect from short circuits. See *Current Limit* for more details.

8.4.1 Enable

The LM26003 device provides a shutdown function via the EN pin to disable the device when the output voltage does not need to be maintained. EN is an analog level input with typically 180 mV of hysteresis. The device is active when the EN pin is above 1.18 V (typical) and in shutdown mode when EN is below this threshold. When EN goes high, the internal VDD regulator turns on and charges the VDD capacitor. When VDD reaches 3.9 V (typical), the soft-start pin begins to source current. In shutdown mode, the VDD regulator shuts down and total quiescent current is reduced to 10.8 µA (typical). Because the EN pin sources 4.85 µA (typical) of pullup current, this pin can be left open for always-on operation. When open, EN will be pulled up to VIN.

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Device Functional Modes (continued)

If EN is connected to VIN, it must be connected through a 10 kΩ resistor to limit noise spikes. EN can also be driven externally with a maximum voltage of 38 V or VIN + 15 V, whichever is lower.

8.4.2 Sleep Mode

In light load conditions, the LM26003 device automatically switches into sleep mode for improved efficiency. As loading decreases, the voltage at FB increases and the COMP voltage decreases. When the COMP voltage reaches the 0.6-V (typical) clamp threshold and the FB voltage rises 1% above nominal, sleep mode is enabled and switching stops. The regulator remains in sleep mode until the FB voltage falls to the reset threshold, at which point switching resumes. This 1% FB window limits the corresponding output ripple requirement to approximately 1% of nominal output voltage. The sleep cycle will repeat until load current is increased. Figure 14 shows typical switching and output voltage waveforms in sleep mode.

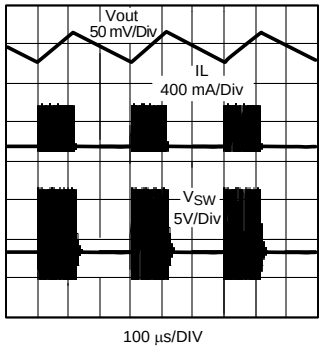

Figure 14. Sleep Mode Waveforms 25-mA Load, Vin = 12 V

In sleep mode, quiescent current is reduced to less than 40 µA (typical) when not switching. The DC sleep mode threshold can roughly be calculated according to the equation below:

$$I_{Sleep} = \left[I_{min} + 0.23\,\mu \left[\frac{Vin - Vout}{L} \right] \right]^2 x \left[\frac{fsw \times L}{D \times 2 \times (Vin - Vout)} \right] \quad (6)$$

where

- Imin = Ilim/16 (4.7A/16 typically)
- D = duty-cycle, defined as (Vout + Vdiode)/Vin.

When load current increases above this limit, the LM26003 device is forced back into PWM operation. The sleep mode threshold varies with frequency, inductance, and duty-cycle as shown in Figure 15.

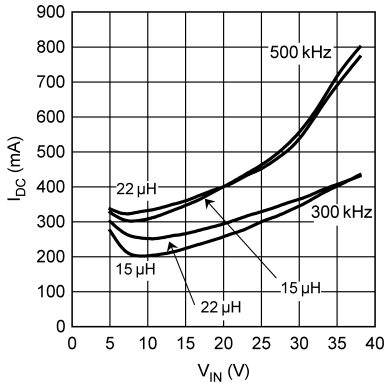

Figure 15. Sleep Mode Threshold vs Vin Vout = 3.3 V

Below the sleep threshold, decreasing load current results in longer sleep cycles, which can be quantified as shown below:

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Device Functional Modes (continued)

Dwake = Iload/Isleep

where

- Dwake is the percentage of time awake when the load current is below the sleep threshold. (7)

Sleep mode combined with low IQ operation minimizes the input supply current. Input supply current in sleep mode can be calculated based on the wake duty cycle, as shown below:

$$Iin = Iq + (I_{QG} \times Dwake) + (Io \times D) \quad (8)$$

Where I_{QG} is the gate drive current, calculated as:

$$I_{QG} = (9.2 \times 10^{-9}) \times f_{SW}$$

And Io is the sum of Iload, Ibias, and current through the feedback resistors.

Because this calculation applies only to sleep mode, use the $I_{q_Sleep_VB}$ and I_{BIAS_SLEEP} values from the *Electrical Characteristics*. If VBIAS is connected to ground, use the same equation with Ibias equal to zero and $I_{q_Sleep_VDD}$.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM26003 is a switching regulator designed for the high-efficiency requirements of applications with standby modes.

9.2 Typical Application

The following sections detail the design of a typical buck converter with sleep mode operation enabled (FPWM low). Figure 16 shows a complete typical application schematic. The components have been selected based on the design criteria given in the following sections.

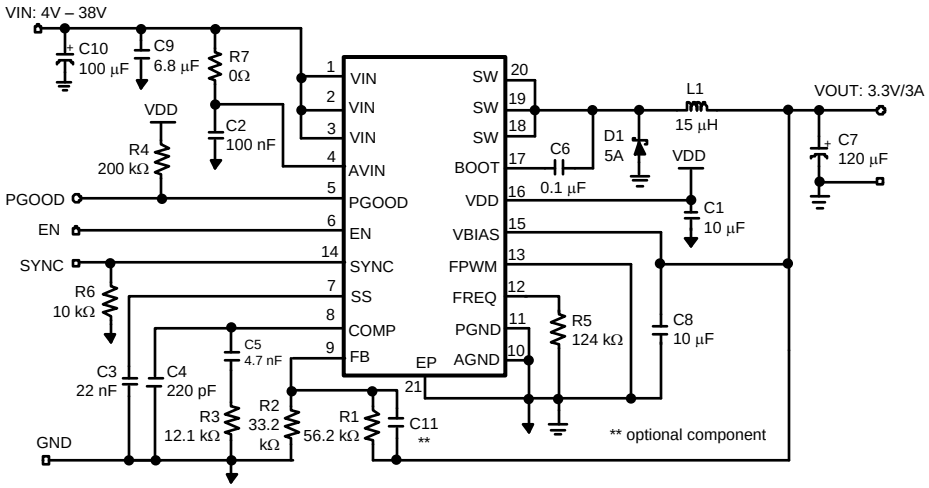

Figure 16. Example Circuit 3A, 300 kHz

9.2.1 Design Requirements

The following parameters are needed to properly design the application and size the components:

Table 1. Design Parameters

PARAMETERS	VALUES
Vout	Output voltage
Vin min	Maximum input voltage
Vin max	Minimum input voltage
Iout max	Maximum output current
Fsw	Switching Frequency
Fbw	Bandwidth of the converter

9.2.2 Detailed Design Procedure

Table 2. Bill of Materials

REFERENCE NUMBER	MANUFACTURER	PART NUMBER
C7	Nippon Chemi-Con	APXE6R3ARA121ME61G
C9	TDK	C4532X7R1H685M
C10	Panasonic	EEE-FK1J101P
D1	Central Semiconductor	CMSH 5-40
L1	Wurth	744770115

9.2.2.1 Setting Output Voltage

The output voltage is set by the ratio of a voltage divider at the FB pin as shown in the typical application. The resistor values can be determined by the following equation:

$$R2 = \frac{R1}{\left(\frac{Vout}{Vfb} - 1\right)} \tag{9}$$

where

- Vfb = 1.236 V typically.

A maximum value of 150 kΩ is recommended for the sum of R1 and R2.

As input voltage decreases towards the nominal output voltage, the LM26003 device can skip up to seven off-pulses as described in the *Low VIN Operation and UVLO* section. In low output voltage applications, if the on-time reaches Ton_{MIN}, the device will skip on-pulses to maintain regulation. There is no limit to the number of pulses that are skipped. In this mode of operation, however, output ripple voltage may increase slightly.

9.2.2.2 Inductor

The output inductor should be selected based on inductor ripple current. The amount of inductor ripple current compared to load current, or ripple content, is defined as Iripple/Iload. Ripple content should be less than 40%. Inductor ripple current, Iripple, can be calculated as shown below:

$$Iripple = \frac{(Vin - Vout) \times Vout}{fsw \times L \times Vin} \tag{10}$$

Larger ripple content increases losses in the inductor and reduces the effective current limit.

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current limit threshold.

Remember that inductor value also affects the sleep mode threshold as shown in Figure 15.

When choosing the inductor, the saturation current rating must be higher than the maximum peak inductor current and the RMS current rating should be higher than the maximum load current. Peak inductor current, Ipeak, is calculated as:

$$Ipeak = Iload + \frac{Iripple}{2} \tag{11}$$

For example, at a maximum load of 3 A and a ripple content of 10%, peak inductor current is equal to 3.15 A which is safely at the minimum current limit of 3.15 A. By increasing the inductor size, ripple content and peak inductor current are lowered, which increases the current limit margin.

The size of the output inductor can also be determined using the desired output ripple voltage, Vrip. The equation to determine the minimum inductance value based on Vrip is as follows:

$$L_{MIN} = \frac{(Vin - Vout) \times Vout \times Re}{Vin \times fsw \times Vrip} \tag{12}$$

Where Re is the ESR of the output capacitors, and Vrip is a peak-to-peak value. This equation assumes that the output capacitors have some amount of ESR. It does not apply to ceramic output capacitors.

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If this method is used, ripple content should still be verified to be less than 40% and that the peak currents do not exceed the minimum current threshold.

9.2.2.3 Output Capacitor

The primary criterion for selecting an output capacitor is equivalent series resistance, or ESR.

ESR (Re) can be selected based on the requirements for output ripple voltage and transient response. Once an inductor value has been selected, ripple voltage can be calculated for a given Re using the equation above for LMIN. Lower ESR values result in lower output ripple.

Re can also be calculated from the following equation:

$$Re_{MAX} = \frac{\Delta Vt}{\Delta It} \tag{13}$$

where

- ΔVt is the allowed voltage excursion during a load transient
- ΔIt is the maximum expected load transient.

If the total ESR is too high, the load transient requirement cannot be met, no matter how large the output capacitance.

If the ESR criteria for ripple voltage and transient excursion cannot be met, more capacitors should be used in parallel.

For non-ceramic capacitors, the minimum output capacitance is of secondary importance, and is determined only by the load transient requirement.

If there is not enough capacitance, the output voltage excursion will exceed the maximum allowed value even if the maximum ESR requirement is met. The minimum capacitance is calculated as follows:

$$C_{MIN} = \frac{L \times \left(\Delta Vt - \sqrt{(\Delta Vt)^2 - (\Delta It \times R_e)^2}\right)}{V_{out} \times R_e^2} \tag{14}$$

It is assumed the total ESR, Re, is no greater than Re_{MAX}. Also, it is assumed that L has already been selected.

Generally speaking, the output capacitance requirement decreases with Re, ΔIt, and L. A typical value greater than 120 µF works well for most applications.

9.2.2.4 Input Capacitor

In a switching converter, very fast switching pulse currents are drawn from the input rail. Therefore, input capacitors are required to reduce noise, EMI, and ripple at the input to the LM26003 device. Capacitors must be selected that can handle both the maximum ripple RMS current at highest ambient temperature as well as the maximum input voltage. The equation for calculating the RMS input ripple current is shown below:

$$Irms = \frac{Iload \times \sqrt{Vout \times (Vin - Vout)}}{Vin} \tag{15}$$

For noise suppression, a ceramic capacitor in the range of 1.0 µF to 10 µF should be placed as close as possible to the PVIN pin. For the AVIN pin also some decoupling is necessary. It is very important that the pin is decoupled with such a capacitor close to the AGND pin and the GND pin of the IC to avoid switching noise to couple into the IC. Also some RC input filtering can be implemented using a small resistor between PVIN and AVIN. In Figure 16 the resistor value of R7 is selected to be 0Ω but can be increased to filter with different time constants depending on the capacitor value used. When using a R7 resistor, keep in mind that the resistance will increase the minimum input voltage threshold due to the voltage drop across the resistor.

The PVIN decoupling should be implemented in a way to minimize the trace length between the Cin capacitor gnd and the Schottky diode gnd. A larger, high ESR input capacitor should also be used. This capacitor is recommended for damping input voltage spikes during power-on and for holding up the input voltage during transients. In low input voltage applications, line transients may fall below the UVLO threshold if there is not enough input capacitance. Both tantalum and electrolytic type capacitors are suitable for the bulk capacitor. However, large tantalums may not be available for high input voltages and their working voltage must be derated by at least 2X.

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9.2.2.5 Bootstrap

The drive voltage for the internal switch is supplied via the BOOT pin. This pin must be connected to a ceramic capacitor, Cboot, from the switch node, shown as C6 in the typical application. The LM26003 device provides the VDD voltage internally, so no external diode is needed. A maximum value of 0.1 µF is recommended for Cboot. Values smaller than 0.022 µF may result in insufficient hold up time for the drive voltage and increased power dissipation.

During low Vin operation, when the on-time is extended, the bootstrap capacitor is at risk of discharging. If the Cboot capacitor is discharged below approximately 2.5 V, the LM26003 device enters a high frequency re-charge mode. The Cboot cap is re-charged via the synchronous FET shown in the block diagram. Switching returns to normal when the Cboot cap has been recharged.

9.2.2.6 Catch Diode

When the internal switch is off, output current flows through the catch diode. Alternately, when the switch is on, the diode sees a reverse voltage equal to Vin. Therefore, the important parameters for selecting the catch diode are peak current and peak inverse voltage. The average current through the diode is given by:

I_{DAVE} = Iload x (1-D)

where

- D is the duty-cycle, defined as Vout/Vin. (16)

The catch diode conducts the largest currents during the lowest duty-cycle. Therefore ID_{AVE} should be calculated assuming maximum input voltage. The diode should be rated to handle this current continuously. For overcurrent or short-circuit conditions, the catch diode should be rated to handle peak currents equal to the peak current limit.

The peak inverse voltage rating of the diode must be greater than maximum input voltage.

A Schottky diode must be used. It's low forward voltage maximizes efficiency and BOOT voltage, while also protecting the SW pin against large negative voltage spikes.

When selecting the catch diode for high efficiency low output load applications, select a Schottky diode with low reverse leakage current. Also keep in mind that the reverse leakage current of a Schottky diode increases with temperature and with reverse voltage. Reverse voltage equals roughly the input voltage in a buck converter. At hot, the diode reverse leakage current may be larger than the current consumption of the LM26003 device.

9.2.2.7 Compensation

The purpose of loop compensation is to ensure stable operation while maximizing dynamic performance. Stability can be analyzed with loop gain measurements, while dynamic performance is analyzed with both loop gain and load transient response. Loop gain is equal to the product of control-output transfer function (power stage) and the feedback transfer function (the compensation network).

For stability purposes, our target is to have a loop gain slope that is –20dB/decade from a very low frequency to beyond the crossover frequency. Also, the crossover frequency should not exceed one-fifth of the switching frequency, that is, 60 kHz in the case of 300 kHz switching frequency.

For dynamic purposes, the higher the bandwidth, the faster the load transient response. The downside to high bandwidth is that it increases the regulators susceptibility to board noise which ultimately leads to excessive falling edge jitter of the switch node voltage.

A large DC gain means high DC regulation accuracy (that is, DC voltage changes little with load or line variations).

To achieve this loop gain, the compensation components should be set according to the shape of the control-output bode plot. A typical plot is shown in Figure 17.

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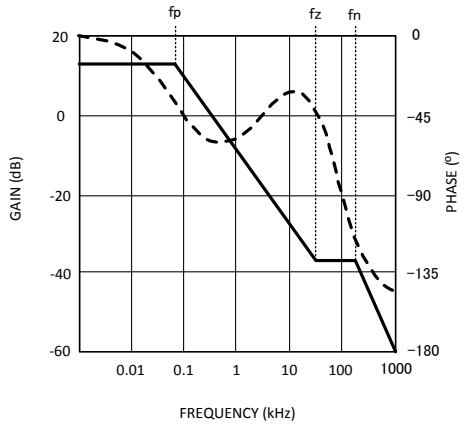

Figure 17. Control-Output Transfer Function

The control-output transfer function consists of one pole (fp), one zero (fz), and a double pole at fn (half the switching frequency).

Referring to Figure 17, the following should be done to create a –20dB/decade roll-off of the loop gain:

1. Place a pole at 0Hz (fpc)
2. Place a zero at fp (fzc)
3. Place a second pole at fz (fpc1)

The resulting feedback (compensation) bode plot is shown below in Figure 18. Adding the control-output response to the feedback response will then result in a nearly continuous -20db/decade slope.

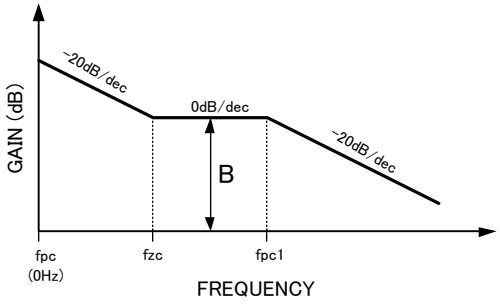

Figure 18. Feedback Transfer Function

The control-output corner frequencies can be determined approximately by the following equations:

$$fz = \frac{1}{2\pi \times Re \times Co} \quad (17)$$

$$fp = \frac{1}{20 \times \pi \times Ro \times Co} + \frac{0.5}{2 \times \pi \times L \times fsw \times Co} \quad (17)$$

$$fn = \frac{fsw}{2} \quad (17)$$

where

- Co is the output capacitance
- Ro is the load resistance
- Re is the output capacitor ESR
- fsw is the switching frequency.

The effects of slope compensation and current sense gain are included in this equation. However, the equation is an approximation intended to simplify loop compensation calculations.

Since fp is determined by the output network, it shifts with loading. Determine the range of frequencies (fpmin/max) across the expected load range. Then determine the compensation values as described below and shown in Figure 19.

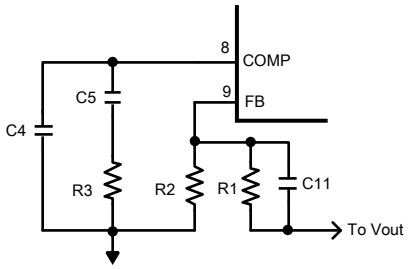

Figure 19. Compensation Network

1. The compensation network automatically introduces a low frequency pole (fpc), which is close to 0 Hz.
2. Once the fp range is determined, R5 should be calculated using:

$$R3 = \frac{B}{gm} \times \left(\frac{R1 + R2}{R2}\right) \quad (18)$$

   Where B is the desired feedback gain in v/v between fp and fz, and gm is the transconductance of the error amplifier. A gain value around 10 dB (3.3 V/V) is generally a good starting point. Bandwidth increases with increasing values of R3.
3. Next, place a zero (fzc) near fp using C5. C5 can be determined with the following equation:

$$C5 = \frac{1}{2 \times \pi \times fp_{MAX} \times R3} \quad (19)$$

   The selected value of C5 should place fzc within a decade above or below fpmax and not less than fpmin. A higher C5 value (closer to fpmin) generally provides a more stable loop, but too high a value will slow the transient response time. Conversely, a smaller C5 value will result in a faster transient response, but lower phase margin.
4. A second pole (fpc1) can also be placed at fz. This pole can be created with a single capacitor, C4. The minimum value for this capacitor can be calculated by:

$$C4 = \frac{1}{2 \times \pi \times fz \times R3} \quad (20)$$

   C4 may not be necessary in all applications. However if the operating frequency is being synchronized below the nominal frequency, C4 is recommended. Although it is not required for stability, C4 is very helpful in suppressing noise.

   A phase lead capacitor can also be added to increase the phase and gain margins. The phase lead capacitor is most helpful for high input voltage applications or when synchronizing to a frequency greater than nominal. This capacitor, shown as C11 in Figure 19, should be placed in parallel with the top feedback resistor, R1.

   C11 introduces an additional zero and pole to the compensation network. These frequencies can be calculated as shown below:

$$fzff = \frac{1}{2 \times \pi \times R1 \times C11}$$

$$fpff = \frac{fzff \times Vout}{Vfb} \quad (21)$$

   A phase lead capacitor will boost loop phase around the region of the zero frequency, fzff. fzff should be placed somewhat below the fpz1 frequency set by C4. However, if C11 is too large, it will have no effect.

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9.2.3 Application Curves

Refer to *Typical Characteristics*.

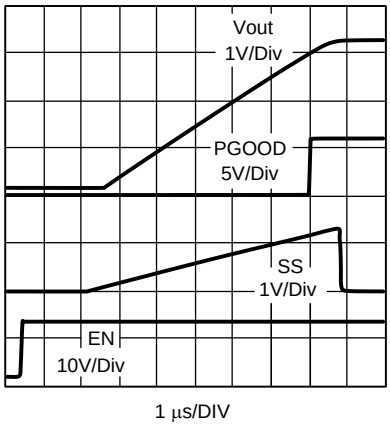

Figure 20. Startup Waveforms

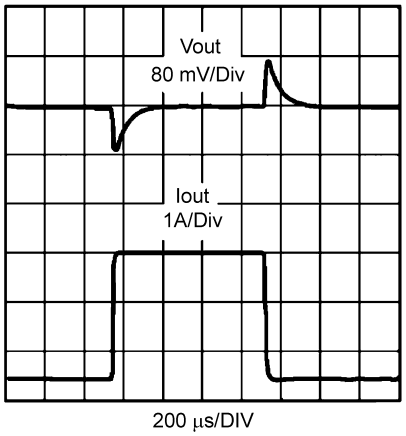

Figure 21. Load Transient Response

10 Power Supply Recommendations

The LM26003 device is designed to operate from various DC power supplies including a car battery. If so, VIN input should be protected from reversal voltage and voltage dump over 48 V. The impedance of the input supply rail should be low enough that the input current transient does not cause a drop below VIN UVLO level. If the input supply is connected by using long wires, additional bulk capacitance may be required in addition to normal input capacitor.

11 Layout

11.1 Layout Guidelines

Good board layout is critical for switching regulators such as the LM26003 device. First, the ground plane area must be sufficient for thermal dissipation purposes, and second, appropriate guidelines must be followed to reduce the effects of switching noise.

Switch mode converters are very fast switching devices. In such devices, the rapid increase of input current combined with parasitic trace inductance generates unwanted Ldi/dt noise spikes at the SW node and also at the VIN node. The magnitude of this noise tends to increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI) and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise.

The current sensing circuit in current mode devices can be easily affected by switching noise. This noise can cause duty-cycle jitter which leads to increased spectrum noise. Although the LM26003 device has 150 ns blanking time at the beginning of every cycle to ignore this noise, some noise may remain after the blanking time. Following the important guidelines below will help minimize switching noise and its effect on current sensing.

The switch node area should be as small as possible. The catch diode, input capacitors, and output capacitors should be grounded to the same local ground, with the bulk input capacitor grounded as close as possible to the catch diode anode. Additionally, the ground area between the catch diode and bulk input capacitor is very noisy and should be somewhat isolated from the rest of the ground plane.

A ceramic input capacitor must be connected as close as possible to the AVIN pin as well as PVIN pin. The capacitor between AVIN and ground should be grounded close to the GND pins of the LM26003 device and the PVIN capacitor should be grounded close to the Schottky diode ground. Often, the AVIN bypass capacitor is most easily located on the bottom side of the PCB. It increases trace inductance due to the vias, it reduces trace length however.

The above layout recommendations are illustrated in Figure 22.

It is a good practice to connect the EP, GND pin, and small signal components (COMP, FB, FREQ) to a separate ground plane, shown in Figure 22 as EP GND, and in the schematics as a signal ground symbol. Both the exposed pad and the GND pin must be connected to ground. This quieter plane should be connected to the high current ground plane at a quiet location, preferably near the Vout ground as shown by the dashed line in Figure 22.

The EP GND plane should be made as large as possible, since it is also used for thermal dissipation. Several vias can be placed directly below the EP to increase heat flow to other layers when they are available. The recommended via hole diameter is 0.3mm.

The trace from the FB pin to the resistor divider should be short and the entire feedback trace must be kept away from the inductor and switch node. See *AN-1229 SIMPLE SWITCHER ® PCB Layout Guidelines*, SNVA054, for more information regarding PCB layout for switching regulators.

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11.2 Layout Example

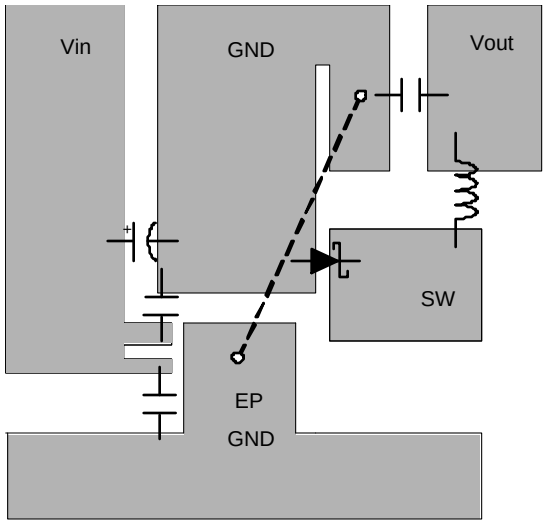

Figure 22. Example PCB Layout

11.3 Thermal Considerations and TSD

Although the LM26003 device has a built in current limit, at ambient temperatures above 80°C, device temperature rise may limit the actual maximum load current. Therefore, temperature rise must be taken into consideration to determine the maximum allowable load current.

Temperature rise is a function of the power dissipation within the device. The following equations can be used to calculate power dissipation (PD) and temperature rise, where total PD is the sum of FET switching losses, FET DC losses, drive losses, Iq, and VBIAS losses:

$$PD_{TOTAL} = Psw_{AC} + Psw_{DC} + PQG + P_{Iq} + P_{VBIAS} \quad (22)$$

$$Psw_{AC} = Vin \times Iload \times fsw \times \left(\frac{Vin \times 10^{-9}}{1.33}\right) \quad (23)$$

$$Psw_{DC} = D \times Iload^2 \times (0.095 + 0.00065 \times (T_j - 25)) \quad (24)$$

$$P_{QG} = Vin \times 9.2 \times 10^{-9} \times fsw \quad (25)$$

$$P_{Iq} = Vin \times Iq \quad (26)$$

$$P_{VBIAS} = Vbias \times I_{VBIAS} \quad (27)$$

Given this total power dissipation, junction temperature can be calculated as follows:

$$Tj = Ta + (PD_{TOTAL} \times \theta_{JA}) \quad (28)$$

Where θ_{JA}= 32°C/W (typically) when using a multi-layer board with a large copper plane area. θ_{JA} varies with board type and metallization area.

To calculate the maximum allowable power dissipation, assume Tj = 125°C. To ensure that junction temperature does not exceed the maximum operating rating of 125°C, power dissipation should be verified at the maximum expected operating frequency, maximum ambient temperature, and minimum and maximum input voltage. The calculated maximum load current is based on continuous operation and may be exceeded during transient conditions.

If the power dissipation remains above the maximum allowable level, device temperature will continue to rise. When the junction temperature exceeds its maximum, the LM26003 device engages Thermal Shut Down (TSD). In TSD, the part remains in a shutdown state until the junction temperature falls to within normal operating limits. At this point, the device restarts in soft-start mode.

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines, SNVA054

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM26003	Click here	Click here	Click here	Click here	Click here
LM26003-Q1	Click here	Click here	Click here	Click here	Click here

12.4 Trademarks

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All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM26003MH/NOPB	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM26003 MH
LM26003MH/NOPB.A	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM26003 MH
LM26003MH/NOPB.B	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM26003 MH
LM26003MHX/NOPB	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM26003 MH
LM26003MHX/NOPB.A	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM26003 MH
LM26003MHX/NOPB.B	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM26003 MH
LM26003QMH/NOPB	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM26003 QMH
LM26003QMH/NOPB.A	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM26003 QMH
LM26003QMH/NOPB.B	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM26003 QMH
LM26003QMHX/NOPB	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM26003 QMH
LM26003QMHX/NOPB.A	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM26003 QMH
LM26003QMHX/NOPB.B	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM26003 QMH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LM26003, LM26003-Q1 :

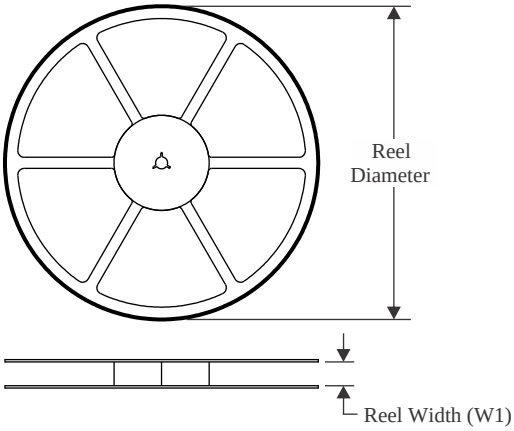
- Catalog : LM26003
- Automotive : LM26003-Q1

NOTE: Qualified Version Definitions:

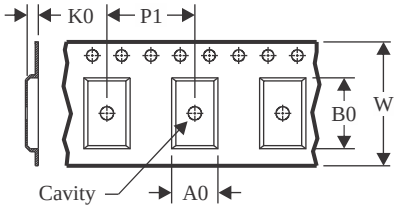
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

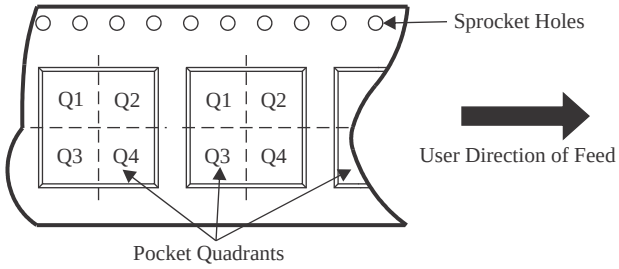


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

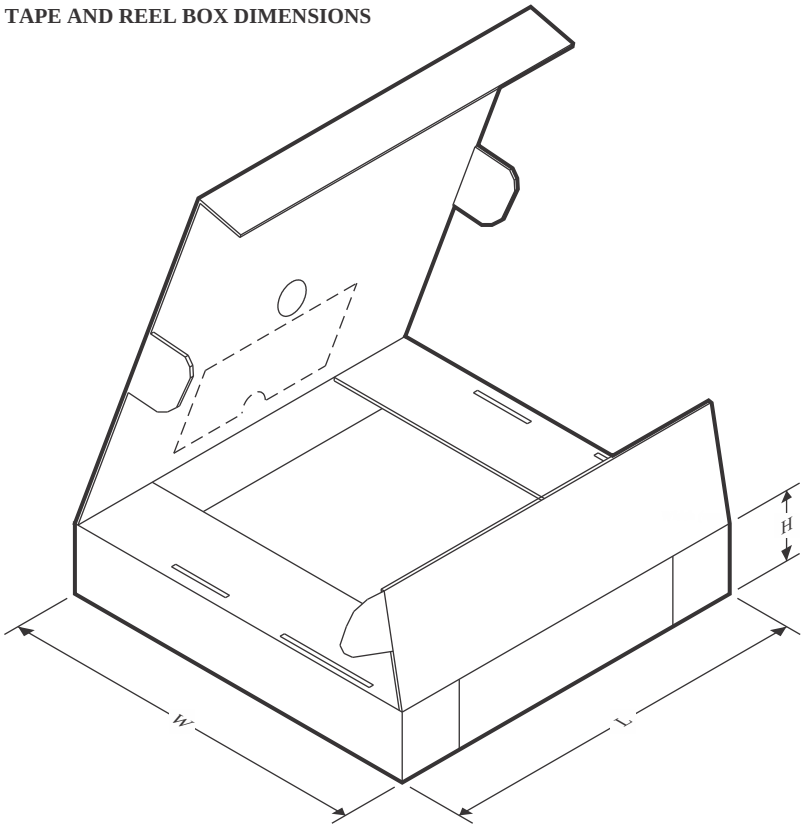
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM26003MHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
LM26003QMHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

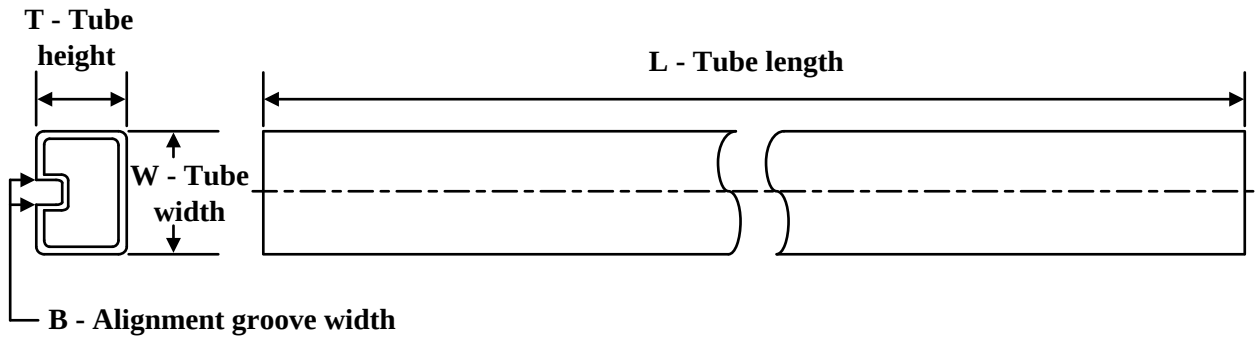
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM26003MHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0
LM26003QMHX/NOPB	HTSSOP	PWP	20	2500	356.0	356.0	35.0

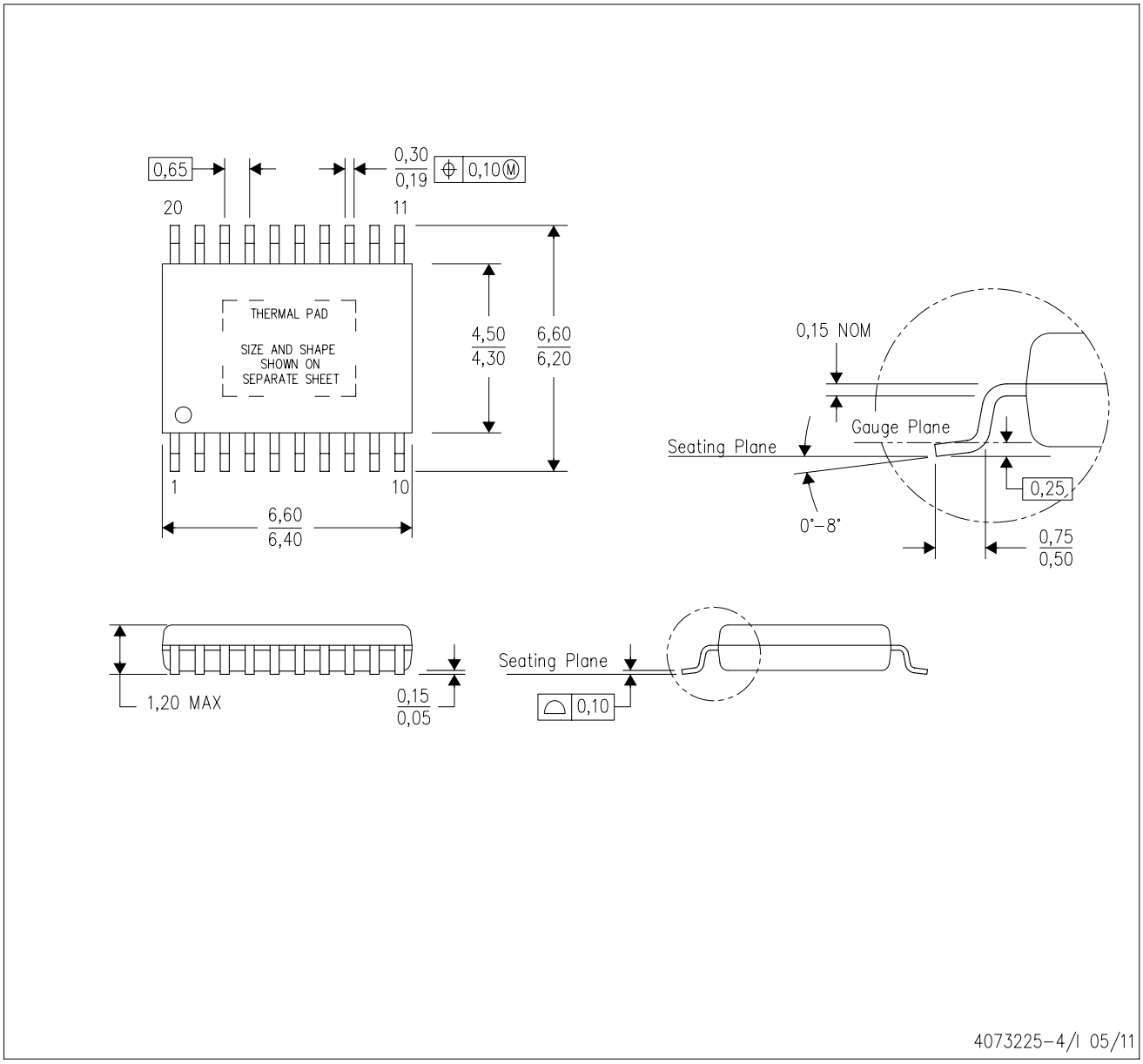
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM26003MH/NOPB	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM26003MH/NOPB.A	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM26003MH/NOPB.B	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM26003QMH/NOPB	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM26003QMH/NOPB.A	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM26003QMH/NOPB.B	PWP	HTSSOP	20	73	495	8	2514.6	4.06

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

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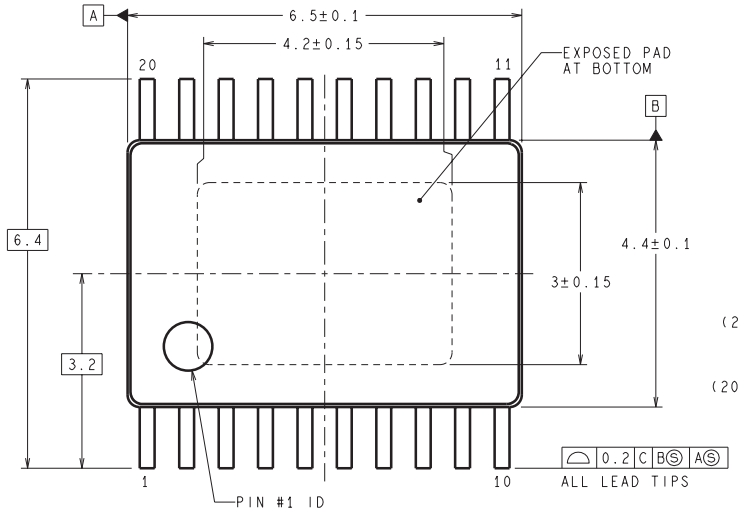
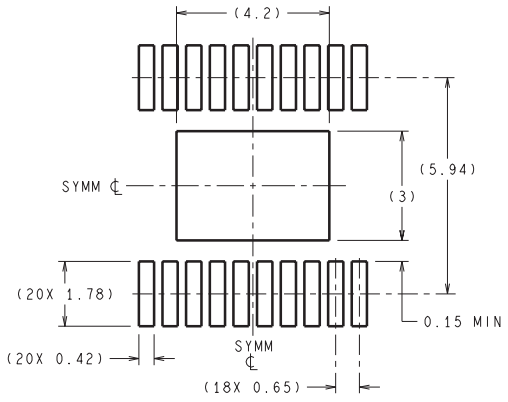
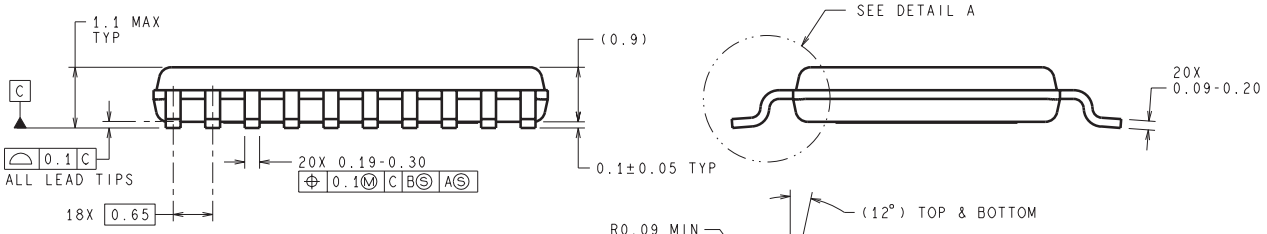
PWP0020A

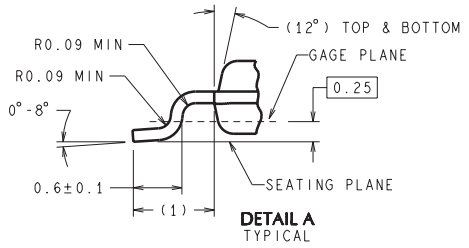




RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



DETAIL A
TYPICAL

MXA20A (Rev C)

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