



Intel® 80321 I/O Processor

Datasheet

Product Features

- Core Features
 - Integrated Intel® XScale™ Core
 - ARM® V5T Instruction Set
 - ARM V5E DSP Extensions
 - 400 MHz and 600 MHz
 - Write Buffer, Write-back Cache
- PCI Bus Interface
 - *PCI Local Bus Specification*, Rev. 2.2 compliant
 - *PCI-X Addendum to the PCI Local Bus Specification*, Rev. 1.0a
 - 64-bit/66 MHz Operation in PCI Mode
 - 64-bit/133 MHz Operation in PCI-X Mode
 - Support 32-bit PCI Initiators and Targets
 - Four Split Read Requests as Initiator
 - Eight Split Read Requests as Target
 - 64-bit Addressing Support
- Memory Controller
 - PC200 Double Data Rate (DDR) SDRAM
 - Up to 1 Gbyte of 64-bit DDR SDRAM
 - Up to 512 Mbytes of 32-bit DDR SDRAM
 - Single-bit Error Correction, Multi-bit Support (ECC)
 - 1024-byte Posted Memory Write Queue
 - 40- and 72-bit wide Memory Interface
- Address Translation Unit
 - 2 Kbyte or 4 Kbyte Outbound Read Queue
 - 4 Kbyte Outbound Write Queue
 - 4 Kbyte Inbound Read and Write Queue
 - Connects Internal Bus to PCI/PCI-X Bus
- DMA Controller
 - Two Independent Channels Connected to Internal Bus
 - Up to 1064 Mbytes/s Burst Support in PCI-X Mode
 - Up to 1600 Mbytes/s Burst Support for Internal Bus
 - Two 1-Kbyte Queues in Ch-0 and Ch-1
 - 2^{32} Addressing Range on Internal Bus Interface
 - 2^{64} Addressing Range on PCI Interface
- Application Accelerator Unit
 - Performs XOR on Read Data
 - Compute Parity Across Local Memory Blocks
 - 1 Kbyte/512-byte Store Queue
- I²C Bus Interface Units
 - Two Separate I²C Units
 - Serial Bus
 - Master/Slave Capabilities
 - System Management Functions
- SSP Serial Port
 - Full-duplex Synchronous Serial Interface
 - Supports 7.2 KHz to 1.84 MHz Bit Rates
- Peripheral Performance Monitoring Unit
 - One Dedicated Global Time Stamp Counter
 - Fourteen Programmable Event Counters
 - Three Control/Status Registers
- Timers
 - Two Dual-programmable 32-bit Timers
 - Watchdog Timer
- 544-Ball, Plastic Ball Grid Array (PBGA)
- Eight General Purpose I/O Pins

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Revision History

Date	Revision #	Description
January 2005	005	Updated case temperature range and other text in first paragraph of Section 3.2, "Package Thermal Specifications" on page 39. Added Section 3.2.1, "Thermal Characteristics" on page 39. Added Table 11 "544-Lead PBGA Package Thermal Characteristics" on page 39. Updated Table 13 "Absolute Maximum Ratings" on page 41: - Updated ratings for "Case temperature under bias." Updated Table 14 "Operating Conditions" on page 41: - Updated maximum value for "Case temperature under bias."
January 2003	004	In Table 7 "Miscellaneous Signals": - For signal GPIO[4]/SDA1, added sentence "2.7K pull-up is required." - For signal GPIO[5]/SCL1, added sentence "2.7K pull-up is required." - For signal GPIO[6]/SDA0, added sentence "2.7K pull-up is required." - For signal GPIO[7]/SCL0, added sentence "2.7K pull-up is required." - Added signal P_BMI with count and type values, and description. In Table 8 "Pin Mode Behavior": - Changed R DYRCV# signal from VI to VO for Reset. - Added signal P_BMI with reset and norm values. In Table 9 "544-Lead PBGA Package - Alphabetical Ball Listing": Changed AE23 from NC2 to P_BMI. In Table 10 "544-Lead PBGA Package - Alphabetical Signal Listing": Changed NC2 to P_BMI. In Section 4.3, "Targeted DC Specifications": Revised notice to state "The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design." Revised Table 16 "I_{CC} Characteristics". In Table 19 "DDR SDRAM Signal Timings": Added TVA6 with description, and minimum signal timing value. In Figure 13 "DDR SDRAM Read Timings": - Revised signal timing relationships for TVA5 and TVA6 to CK and rcveno#. - Added TVA6 signal timing relationship to reveni# and DQS. Added Figure 18 "PCI_RST# vs. PWRDELAY Timings During Power-Up". Added Figure 19 "PCI_RST# vs. PWRDELAY Timings During Power-Down".
June 2002	003	Formatting Changes.
June 2002	002	Removed Advance Information designation.
February 2002	001	Initial release.



1.0 Introduction

1.1 About This Document

This is the *Intel® 80321 I/O Processor Datasheet*. This datasheet contains a functional overview, package signal locations, targeted electrical specifications, and bus functional waveforms. Detailed functional descriptions other than parametric performance is published in the *Intel® 80321 I/O Processor Developer's Manual*.

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1.1.1 Terminology

To aid the discussion of the Intel® 80321 I/O processor (80321) architecture, the following terminology is used:

Downstream	At or toward a PCI bus with a higher number (after configuration)
Host processor	Processor located upstream from the 80321
Local processor	Intel XScale® core (ARM* architecture compliant) within the 80321
Local bus	80321 Internal Bus
Local memory	Memory subsystem on the Intel XScale® core PC200 DDR SDRAM or Peripheral Bus Interface busses
Upstream	At or toward a PCI bus with a lower number (after configuration)

1.1.2 Other Relevant Documents

Table 1. Related Documentation

Document Title	Document# / Contact
<i>Intel® 80312 I/O Companion Chip Developer's Manual</i>	273410
<i>Intel® 80312 I/O Companion Chip Specification Update</i>	273416
<i>Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Developer's Manual</i>	273411
<i>Intel® 80310 I/O Processor Chipset with Intel® XScale™ Microarchitecture Design Guide</i>	273354
<i>Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Datasheet</i>	273414
<i>Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Specification Update</i>	273415
<i>PCI Local Bus Specification, Revision 2.2</i>	PCI Special Interest Group 1-800-433-5177 http://www.pcisig.com/home
<i>PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a</i>	
<i>PCI-to-PCI Bridge Architecture Specification, Revision 1.1</i>	
<i>PCI System Design Guide, Revision 1.0</i>	
<i>PCI Hot-Plug Specification, Revision 1.0</i>	
<i>PCI Bus Power Management Interface Specification, Revision 1.1</i>	
<i>I²C Peripherals for Microcontrollers</i>	Philips Semiconductor*
<i>Advanced Configuration and Power Interface Specification, Revision 1.0 (ACPI)</i>	http://www.teleport.com/~acpi/

NOTE: Also see our product website at: <http://developer.intel.com/design/io/>.

1.2 About the Intel® 80321 I/O Processor

The 80321 is a single-function device that integrates the Intel XScale® core with intelligent peripherals, including a PCI bus application bridge. The 80321 consolidates into a single system:

- Intel XScale® core
- PCI - Local Memory Bus Address Translation Unit
- Messaging Unit
- Direct Memory Access (DMA) Controller
- Peripheral Bus Interface Unit
- Integrated Memory Controller
- Performance Monitor
- Application Accelerator
- Two I²C Bus Interface Units
- Synchronous Serial Port Unit
- Eight General Purpose Input Output (GPIO) ports

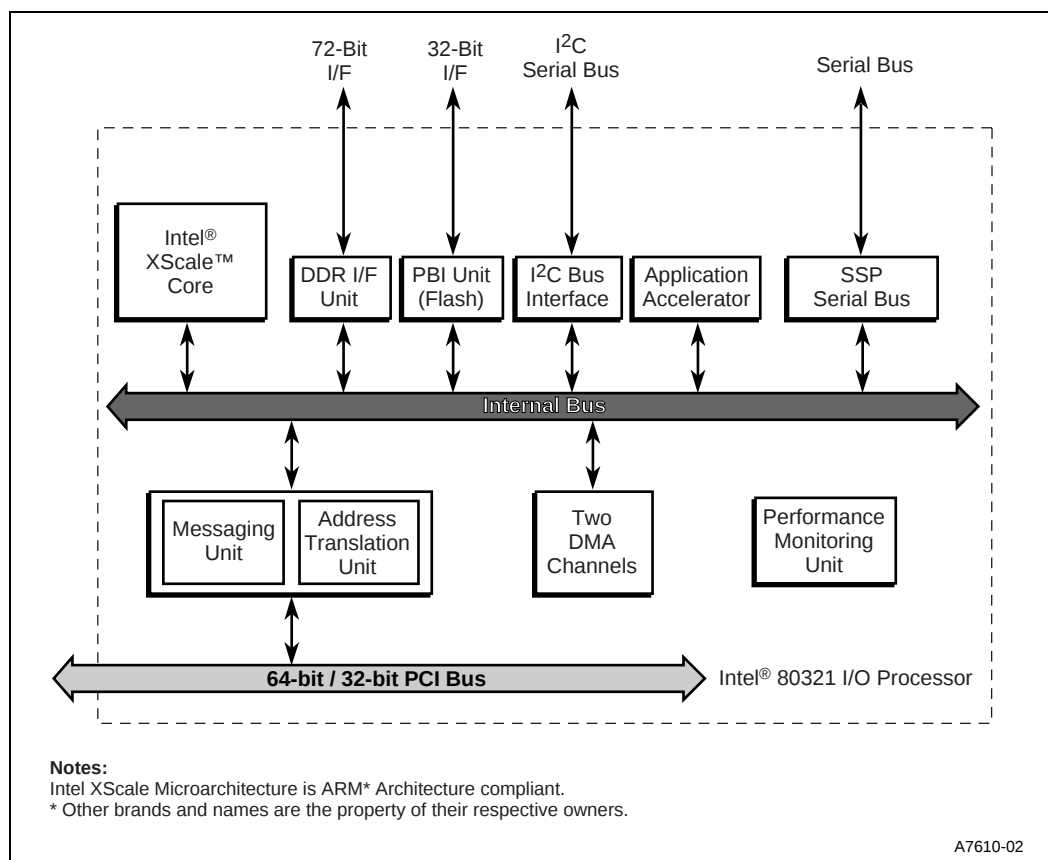
It is an integrated processor that addresses the needs of intelligent I/O applications and helps reduce intelligent I/O system costs.

The PCI Bus is an industry standard, high performance, low latency system bus. The 80321 PCI Bus is capable of 133 MHz operation in PCI-X mode as defined by the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a. Also, the processor supports a 66 MHz conventional PCI mode as defined by the *PCI Local Bus Specification*, Revision 2.2. The addition of the Intel XScale® core brings intelligence to the PCI bus application bridge.

The 80321 is a single-function PCI device. This function represents the address translation unit. The address translation unit is an ‘application bridge’ as defined by the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a. The 80321 contains PCI configuration space accessible through the PCI bus.

Figure 1 is a block diagram of the 80321.

Figure 1. Intel® 80321 I/O Processor Functional Block Diagram



2.0 Features

The 80321 combines the Intel XScale® core with powerful new features to create an intelligent I/O processor. This single-function PCI device is fully compliant with the *PCI Local Bus Specification*, Revision 2.2. 80321-specific features include:

- Address Translation Unit
- Memory Controller
- Peripheral Bus Interface
- Application Accelerator Unit
- I²C Bus Interface Units
- DMA Controller
- Performance Monitoring Unit
- Synchronous Serial Port Unit
- Messaging Unit
- I₂O* Compatibility

The subsections that follow briefly overview each feature. Refer to the appropriate chapter in the *Intel® 80321 I/O Processor Developer's Manual* for full technical descriptions.

The 80321 core is based upon the Intel XScale® core. The core processor operates at a maximum frequency of 600 MHz. The instruction cache is 32 Kbytes in size and is 32-way set associative. Also, the core processor includes a data cache that is 32 Kbytes and is 32-way set associative and a mini data cache that is 2 Kbytes and is 2-way set associative.

The 80321 includes 8 General Purpose I/O (GPIO) pins.

2.1 Internal Bus

The Internal Bus is a high-speed interconnect between all internal units and controllers. The Internal Bus operates at 200 MHz and is 64 bits wide.

2.2 DMA Controller

The DMA Controller allows low-latency, high-throughput data transfers between PCI bus agents and the local memory. Two separate DMA channels accommodate data transfers on the PCI bus. The DMA Controller supports chaining and unaligned data transfers. It is programmable through the Intel XScale® core only.

2.3 Address Translation Unit

The Address Translation Unit (ATU) allows PCI transactions direct access to the 80321 local memory. The ATU supports transactions between PCI address space and the 80321 address space. Address translation is controlled through programmable registers accessible from both the PCI interface and the Intel XScale® core. Dual access to registers allows flexibility in mapping the two address spaces. The ATU also supports the following extended capability configuration headers:

1. Power Management header as defined by *PCI Bus Power Management Interface Specification*, Revision 1.1.
2. Message Signaled Interrupt capability structure specified in *PCI Local Bus Specification*, Revision 2.2.
3. PCI-X Capabilities List Item specified in the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a.

2.4 Messaging Unit

The Messaging Unit (MU) provides data transfer between the PCI system and the 80321. It uses interrupts to notify each system when new data arrives. The MU has four messaging mechanisms:

- Message Registers
- Doorbell Registers
- Circular Queues
- Index Registers

Each allows a host processor or external PCI device and the 80321 to communicate through message passing and interrupt generation.

2.5 Memory Controller

The Memory Controller allows direct control of a PC200 DDR SDRAM memory subsystem. It features programmable chip selects and support for error correction codes (ECC). External memory may be configured as PCI addressable memory or private 80321 memory.

2.6 Peripheral Bus Interface

The Peripheral Bus Interface Unit (PBI) is a data communication path to certain components of a 80321 hardware system that do not have PCI bus interfaces and/or do not optimally reside on the PCI Bus. Examples of such components include Flash Memory and DSP host interface ports. The PBI allows the processor to manipulate data and interact with these components in the I/O environment. To perform these tasks at high bandwidth, the bus features a burst transfer capability which allows successive 32-bit data transfers. The bus has a 33 MHz, 66 MHz and a 100 MHz operating mode.

2.7 Application Accelerator Unit

The Application Accelerator Unit transfers blocks of data to and from the local memory and performs boolean operations, such as XOR, on the data.

2.8 Performance Monitoring Unit

The Performance Monitoring Unit (PMON) allows various events on the 80321 to be monitored. The 14 Event Counters may be programmed to observe events selected from a pre-defined set of events.

2.9 I²C Bus Interface Units

There are two I²C (Inter-Integrated Circuit) Bus Interface Units that allow the Intel XScale® core to serve as a master and slave device residing on the I²C bus. The I²C unit uses a serial bus developed by Philips Semiconductor* consisting of a two-pin interface. The bus allows the 80321 to interface to other I²C peripherals and microcontrollers for system management functions. It requires a minimum of hardware for an economical system to relay status and reliability information on the I/O subsystem to an external device. Also refer to *I²C Peripherals for Microcontrollers* (Philips Semiconductor*).

2.10 Synchronous Serial Port Unit

The Synchronous Serial Port (SSP) Unit is a full-duplex synchronous serial interface. It may connect to a variety of external analog-to-digital (A/D) converters, audio and telecom codecs, and many other devices which use serial protocols for transferring data. It supports the National Microwire*, Texas Instrument* synchronous serial protocol, and the Motorola* serial peripheral interface (SPI) protocol.

3.0 Package Information

3.1 Package Introduction

The 80321 is offered in a Plastic Ball Grid Array (PBGA) package. This is a perimeter array package with 508 ball connections in the outer area of the package and a square 6x6 grid of rows of ball connections in the middle area of the package. See [Figure 3 “544-Lead PBGA Package \(Bottom View\)”](#) on page 26.

3.1.1 Functional Signal Definitions

This section defines the pins and signals.

Table 2. Pin Description Nomenclature

Symbol	Description
I	Input pin only
O	Output pin only
I/O	Pin may be either an input or output.
OD	Open Drain pin
-	Pin must be connected as described.
Sync(...)	Synchronous. Signal meets timings relative to an input clock. Sync(P) Synchronous to P_CLK Sync(M) Synchronous to M_CK[2:0] Sync(PB) Synchronous to PB_CLK Sync(SS) Synchronous to SSCKO Sync(T) Synchronous to TCK
Async	Asynchronous. Inputs may be asynchronous relative to all clocks. All asynchronous signals are level-sensitive.
Rst(P)	The pin is reset with P_RST# .
Rst(M)	The pin is reset with M_RST# . Note that M_RST# is asserted when P_RST# is asserted or PCSR[5] is set with software.
Rst(T)	The pin is reset with TRST# .
(Configuration Pin)	These pins are used during reset to configure the processor. These pins have internal pullup resistors which are turned on when P_RST# is low. To configure the pin low connect a 4.7K Ω resistor from the pin to ground. By default the pin is configured high.

Table 3. DDR SDRAM Signals

Name	Count	Type	Description
RCVENI#	1	I	RECEIVE ENABLE IN provides delay information for enabling the input receivers and must be connected to RCVENO# of the 80321.
RCVENO#	1	O	RECEIVE ENABLE OUT must be connected to RCVENI# of the 80321 and be trace length matched to Clock Trace plus average DQ Traces.
M_CK[2:0]	3	O	MEMORY CLOCKS are used to provide the positive differential clocks to the external SDRAM memory subsystem.
M_CK[2:0]#	3	O	MEMORY CLOCKS are used to provide the negative differential clocks to the external SDRAM memory subsystem.
M_RST#	1	O Async	MEMORY RESET indicates when the memory subsystem has been reset with P_RST# or a software reset.
SA[12:0]	13	O Sync(M) Rst(M)	MEMORY ADDRESS BUS carries the multiplexed row and column addresses to the SDRAM memory banks. For SA[10] , See Note 1.
SBA[1:0]	2	O Sync(M) Rst(M)	SDRAM BANK ADDRESS indicates which of the SDRAM internal banks are read or written during the current transaction. See Note 1.
SRAS#	1	O Sync(M) Rst(M)	SDRAM ROW ADDRESS STROBE indicates the presence of a valid row address on the Multiplexed Address Bus SA[12:0] . See Note 1.
SCAS#	1	O Sync(M) Rst(M)	SDRAM COLUMN ADDRESS STROBE indicates the presence of a valid column address on the Multiplexed Address Bus SA[12:0] . See Note 1.
SWE#	1	O Sync(M) Rst(M)	SDRAM WRITE ENABLE indicates that the current memory transaction is a write operation. See Note 1.
SCE[1:0]#	2	O Sync(M) Rst(M)	SDRAM CHIP SELECT enables the SDRAM devices for a memory access (Physical banks 0 and 1). See Note 1.
SCKE[1:0]	2	O Sync(M) Rst(M)	SDRAM CLOCK ENABLE enables the clocks for the SDRAM memory. Deasserting places the SDRAM in self-refresh mode. See Note 1.
DQ[63:0]	64	I/O Sync(M) Rst(M)	SDRAM DATA BUS carries 64-bit data to and from memory. During a data cycle, read or write data is present on one or more contiguous bytes. During write operations, unused pins are driven to determinate values. See Note 1.
SCB[7:0]	8	I/O Sync(M) Rst(M)	SDRAM ECC CHECK BITS carry the 8-bit ECC code to and from memory during data cycles. See Note 1.
DQS[8:0]	9	I/O Sync(M) Rst(M)	SDRAM DATA STROBES carry the strobe signals which are used to capture data on the data bus. See Note 1.
SDQM[8:0]	9	O Sync(M) Rst(M)	SDRAM DATA MASK controls which bytes on the data bus should be written. When SDQM[8:0] is asserted, the SDRAM devices do not accept valid data from the byte lanes. See Note 1.
V _{REF}	1	I	SDRAM VOLTAGE REFERENCE is used to supply the reference voltage to the differential inputs of the memory controller pins.

NOTE:

1. These pins remain functional for 20 **M_CK[2:0]** periods after **M_RST#** is asserted for a warm boot. The designated Rst(M) state applies after 20 **M_CK[2:0]** periods after **M_RST#** is asserted. For more details, refer to the MCU Chapter of the *Intel® 80321 I/O Processor Developer's Manual*.

Table 4. Peripheral Bus Interface Signals (Sheet 1 of 3)

Name	Count	Type	Description
AD[31:0]	32	I/O Sync(PB) Rst(M)	ADDRESS / DATA BUS During an address cycle bits 31-2 contain the physical word address and bits 1-0 specify the number of data transfers during the bus transaction. 00= 1 Transfer 01= 2 Transfers 10= 3 Transfers 11= 4 Transfers. During a data cycle bits 31-0, 15-0 or 7-0 contain valid data, depending on the corresponding 32-, 16- or 8-bit bus width. During 16- and 8-bit bus write operations the unused bus pins are driven to determinate values.
A[3:2]	2	O Sync(PB) Rst(M)	ADDRESS [3:2] carries a demultiplexed version of bits 3 and 2 of the address bus. During an address cycle A[3:2] matches AD[3:2] . During a burst read or write data cycle A[3:2] represents the current DWORD address in the burst transaction.
BE[3:0]#	4	O Sync(PB) Rst(M)	BYTE ENABLES select which of up to four data bytes on the bus participate in the current bus access. The byte enables are asserted during the address cycle. These signals do not toggle during a burst and they remain active through the last data cycle. Byte enable encoding is dependent on the bus width: 32-bit bus: BE[3]# enables data on AD[31:24] BE[2]# enables data on AD[23:16] BE[1]# enables data on AD[15:8] BE[0]# enables data on AD[7:0] 16-bit bus: BE[3]# enables data on AD[15:8] BE[2]# is not used (state is high) BE[1]# becomes Address Bit 1 (A[1]) BE[0]# enables data on AD[7:0] 8-bit bus: BE[3]# is not used (state is high) BE[2]# is not used (state is high) BE[1]# becomes Address Bit 1 (A[1]) BE[0]# becomes Address Bit 0 (A[0]) For 16- and 8-bit bus accesses these address bits are asserted in conjunction with A[3:2] .
ALE	1	O Sync(PB) Rst(M)	ADDRESS LATCH ENABLE indicates the transfer of a physical address. The pin is asserted during the first address cycle and deasserted during the second address cycle. The pin floats whenever the bus is relinquished to an external device
ADS#	1	O Sync(PB) Rst(M)	ADDRESS STROBE indicates a valid address and the start of a new bus access. The pin is asserted during the second address cycle and deasserted during the first data cycle. The pin floats whenever the bus is relinquished to an external device
PB_CLK	1	O	PERIPHERAL BUS CLOCK is the reference clock for all signals on the peripheral bus.
WR#	1	O Sync(PB) Rst(M)	WRITE / READ indicates whether the bus access is a write or a read with respect to the 80321 and is valid during the entire bus access. This pin may be used to control the OE# input on the flash ROM. The pin floats whenever the bus is relinquished to an external device 0 = Read 1 = Write

Table 4. Peripheral Bus Interface Signals (Sheet 2 of 3)

Name	Count	Type	Description
FWE#	1	O Sync(PB) Rst(M)	FLASH WRITE ENABLE indicates whether the bus access is a write or a read with respect to the 80321 and is valid during the entire bus access. This pin is used for flash memory accesses and controls the SWE# input on the ROM. The pin floats whenever the bus is relinquished to an external device. 0 = Write 1 = Read
DEN#	1	O Sync(PB) Rst(M)	DATA ENABLE indicates data transfer cycles during a bus access. DEN# is asserted at the start of the first data cycle and deasserted at the end of the last data cycle. The pin is used to provide control for data transceivers connected to the bus. The pin floats whenever the bus is relinquished to an external device
BLAST#	1	O Sync(PB) Rst(M)	BURST LAST indicates the last data transfer of a bus access. BLAST# remains active when wait states are inserted and becomes inactive after the final data transfer is complete. The pin floats whenever the bus is relinquished to an external device
RDYRCV#	1	I/O Sync(PB) Rst(M)	READY / RECOVER During a data cycle the pin indicates that data may be sampled or removed. 0 = Sample data 1 = Insert wait state During a recover state the pin indicates that the recover state is repeated. This function allows slow external devices longer to float their pins before the next address is driven. 0 = Insert recovery state 1 = Recovery complete NOTE: PBI Base Address Register 0 bit 9 (Flash Window Enable) is enabled for flash by default to support the boot process. See PBBAR0 description in the 80321 I/O Processor Developer's Manual.
HOLD	1	I Sync(PB)	HOLD is used by an external device to request access to the bus.
HOLDA	1	O Sync(PB) Rst(M)	HOLD ACKNOWLEDGE indicates to an external device that it has been granted access to the bus.
PB_RST#	1	O Async	PERIPHERAL BUS RESET indicates when the peripheral bus has been reset with P_RST# or a software reset.
PCE[5]# / PBI100MHZ# (Configuration Pin)	1	I/O Sync(PB) Rst(M)	PERIPHERAL CHIP ENABLES specify which of the six memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access. PERIPHERAL BUS 100 MHz ENABLE is latched at the deasserting edge of P_RST# and it indicates the speed at which the PBI bus operates. [PBI100MHZ# , PBI66MHZ#] 11 = 33 MHz (Default Mode) 10 = 66 MHz 01 = 100 MHz 00 = Undefined (Reserved - Do Not Use)
PCE[4]# / PBI66MHZ# (Configuration Pin)	1	I/O Sync(PB) Rst(M)	PERIPHERAL CHIP ENABLES specify which of the six memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access. PERIPHERAL BUS 66MHz ENABLE is latched at the deasserting edge of P_RST# and it indicates the speed at which the PBI bus operates. [PBI100MHZ# , PBI66MHZ#] 11 = 33 MHz (Default Mode) 10 = 66 MHz 01 = 100 MHz 00 = Undefined (Reserved - Do Not Use)

Table 4. Peripheral Bus Interface Signals (Sheet 3 of 3)

Name	Count	Type	Description
PCE[3]# / P_BOOT16# (Configuration Pin)	1	O Sync(PB) Rst(M)	PERIPHERAL CHIP ENABLES specify which of the six memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access. PERIPHERAL BUS BOOT WIDTH 16 ENABLE specifies the width of the peripheral bus for flash accesses during boot up. 0 = 16-bit bus width (Requires Pull-Down Resistor) 1 = 8-bit bus width (Default Mode)
PCE[2]# / 32BITPCI# (Configuration Pin)	1	I/O Sync(PB) Rst(M)	PERIPHERAL CHIP ENABLES specify which of the six memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access. 32 BIT PCI is latched at the deasserting edge of P_RST# and it indicates the width of the PCI-X bus to the PCI-X Status Register (bit 16 of the PCI-X Status Register). 0 = 32-Bit PCI-X Bus (Requires pull-down resistor) 1 = 64-Bit PCI-X Bus (Default mode)
PCE[1]# / RETRY (Configuration Pin)	1	I/O Sync(PB) Rst(M)	PERIPHERAL CHIP ENABLES specify which of the six memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access. RETRY is latched at the deasserting edge of P_RST# and it determines when the Primary PCI interface disables PCI configuration cycles by signaling a Retry until the Configuration Cycle Retry bit is cleared in the PCI Configuration and Status Register. 0 = Configuration Cycles enabled (Requires pull-down resistor) 1 = Retry enabled (Default mode)
PCE[0]# / RST_MODE# (Configuration Pin)	1	I/O Sync(PB) Rst(M)	PERIPHERAL CHIP ENABLES specify which of the six memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access. RESET MODE is latched at the deasserting edge of P_RST# and it determines when the 80321 is held in reset until the Intel XScale® microprocessor Reset bit is cleared in the PCI Configuration and Status Register. 0 = Hold in reset (Requires pull-down resistor) 1 = Don't hold in reset (Default mode)
WIDTH[1:0]	2	O Sync(PB) Rst(M)	WIDTH denotes the physical memory attributes for a bus transaction. The pins float whenever the bus is relinquished to an external device. 00 = 8 Bits Wide 01 = 16 Bits Wide 10 = 32 Bits Wide 11 = Reserved

Table 5. PCI Bus Signals (Sheet 1 of 2)

Name	Count	Type	Description
P_AD[31:0]	32	I/O Sync(P) Rst(P)	PCI ADDRESS/DATA is the multiplexed PCI address and bottom 32 bits of the data bus.
P_AD[63:32]	32	I/O Sync(P) Rst(P)	PCI DATA is the upper 32 bits of the PCI data bus driven during the data phase.
P_PAR	1	I/O Sync(P) Rst(P)	PCI BUS PARITY is even parity across P_AD[31:0] and P_C/BE[3:0]#.
P_PAR64	1	I/O Sync(P) Rst(P)	PCI BUS UPPER DWORD PARITY is even parity across P_AD[63:32] and P_C/BE[7:4]#.
P_C/BE[3:0]#	4	I/O Sync(P) Rst(P)	PCI BUS COMMAND and BYTE ENABLES are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables for P_AD[31:0].
P_C/BE[7:4]#	4	I/O Sync(P) Rst(P)	PCI BUS BYTE ENABLES are as byte enables for P_AD[63:32] during the data phase.
P_REQ#	1	O Rst(P)	PCI BUS REQUEST indicates to the PCI bus arbiter that the 80321 desires use of the PCI bus.
P_REQ64#	1	I/O Sync(P) Rst(P)	PCI BUS REQUEST 64-BIT TRANSFER indicates the attempt of a 64-bit transaction on the PCI bus. When the target is 64-bit capable, the target acknowledges the attempt with the assertion of P_ACK64#.
P_GNT#	1	I Sync(P)	PCI BUS GRANT indicates that access to the PCI bus has been granted.
P_ACK64#	1	I/O Sync(P) Rst(P)	PCI BUS ACKNOWLEDGE 64-BIT TRANSFER indicates that the device has positively decoded its address as the target of the current access and the target transfers data using the full 64-bit data bus.
P_FRAME#	1	I/O Sync(P) Rst(P)	PCI BUS CYCLE FRAME is asserted to indicate the beginning and duration of an access.
P_IRDY#	1	I/O Sync(P) Rst(P)	PCI BUS INITIATOR READY indicates the initiating agent's ability to complete the current data phase of the transaction. During a write, it indicates that valid data is present on the Address/Data bus. During a read, it indicates the processor is ready to accept the data.
P_TRDY#	1	I/O Sync(P) Rst(P)	PCI BUS TARGET READY indicates the target agent's ability to complete the current data phase of the transaction. During a read, it indicates that valid data is present on the Address/Data bus. During a write, it indicates the target is ready to accept the data.
P_STOP#	1	I/O Sync(P) Rst(P)	PCI BUS STOP indicates a request to stop the current transaction on the PCI bus.
P_DEVSEL#	1	I/O Sync(P) Rst(P)	PCI BUS DEVICE SELECT is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
P_SERR#	1	I/O OD Sync(P) Rst(P)	PCI BUS SYSTEM ERROR is driven for address parity errors on the PCI bus.
P_CLK	1	I	PCI BUS INPUT CLOCK provides the timing for all PCI transactions and is the clock source for most internal 80321 units.

Table 5. PCI Bus Signals (Sheet 2 of 2)

Name	Count	Type	Description
P_RST#	1	I Async	RESET brings PCI-specific registers, sequencers, and signals to a consistent state. When P_RST# is asserted: PCI output signals are driven to a known consistent state. PCI bus interface output signals are three-stated. Open drain signals such as P_SERR# are floated. P_RST# may be asynchronous to P_CLK when asserted or deasserted. Although asynchronous, deassertion must be guaranteed to be a clean, bounce-free edge.
P_PERR#	1	I/O Sync(P) Rst(P)	PCI BUS PARITY ERROR is asserted when a data parity error occurs during a PCI bus transaction.
P_IDSEL	1	I Sync(P)	PCI BUS INITIALIZATION DEVICE SELECT is used to select the 80321 during a Configuration Read or Write command on the PCI bus.
P_INT[A:D]#	4	O OD Async Rst(P)	PCI BUS INTERRUPT requests an interrupt. The assertion and deassertion of P_INT[A:D]# is asynchronous to P_CLK . A device asserts its P_INT[A:D]# line when requesting attention from its device driver. Once the P_INT[A:D]# signal is asserted, it remains asserted until the device driver clears the pending request. P_INT[A:D]# Interrupts are level sensitive.
P_M66EN	1	I	PCI BUS 66 MHz ENABLE indicates the speed of the PCI bus. When this signal is sampled high the PCI bus speed is 66 MHz, when low the bus speed is 33 MHz.

Table 6. Serial Port Interface Signals

Name	Count	Type	Description
SSCKO	1	O	SERIAL PORT CLOCK OUT is the output bit-rate clock.
SFRM	1	O Sync(SS) Rst(M)	SERIAL FRAME indicates the beginning and end of a serial data word.
TXD	1	O Sync(SS) Rst(M)	TRANSMIT DATA is the outbound serial data pin.
RXD	1	I Sync(SS)	RECEIVE DATA is the inbound serial data pin.
SSCKI	1	I	SERIAL PORT CLOCK IN is the input bit-rate clock which may be used when a frequency other than the default of 3.7 MHz is needed.

Table 7. Miscellaneous Signals (Sheet 1 of 2)

Name	Count	Type	Description
P_BMI	1	O Async Rst(M)	PCI-X Bus Master Indicator is an output used for hiding an I/O Controller on the same bus segment as the 80321 by controlling the IDSEL line of that I/O Controller. The output state of this signal is controlled by bit 0 of the GPOD register and the default state at Reset is 0. When not being used, this pin will be a NC. Please see the 80321 Specification Update, Specification Clarification section for more details.
XINT[3:0]#	4	I Async	EXTERNAL INTERRUPT REQUESTS are used by external devices to request interrupt service. These pins are level-detect only and are internally synchronized. These interrupts may be directed to either the PCI pins P_INT[A:D]# or to the 80321 interrupt controller pins XINT[3:0]# as shown below. XINT[0]# ⇒ P_INT[A]# or XINT[0]# XINT[1]# ⇒ P_INT[B]# or XINT[1]# XINT[2]# ⇒ P_INT[C]# or XINT[2]# XINT[3]# ⇒ P_INT[D]# or XINT[3]#
HPI#	1	I Async	HIGH PRIORITY INTERRUPT causes a high priority non-maskable interrupt to the 80321. This pin is level-detect only and is internally synchronized.
GPIO[3:0]	4	I/O Async Rst(M)	GENERAL PURPOSE INPUT/OUTPUT. These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input.
GPIO[4] / SDA1	1	I/O Async Rst(P) I/O OD Rst(M)	GENERAL PURPOSE INPUT/OUTPUT. These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. I²C DATA is used for data transfer and arbitration on the I ² C bus. This is one of two I ² C buses that the user may enable. 2.7K pull-up is required.
GPIO[5] / SCL1	1	I/O Async Rst(P) I/O OD Rst(M)	GENERAL PURPOSE INPUT/OUTPUT. These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. I²C CLOCK provides synchronous operation of the I ² C bus. This is one of two I ² C buses that the user may enable. 2.7K pull-up is required.
GPIO[6] / SDA0	1	I/O Async Rst(P) I/O OD Rst(M)	GENERAL PURPOSE INPUT/OUTPUT. These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. I²C DATA is used for data transfer and arbitration on the I ² C bus. This is one of two I ² C buses that the user may enable. 2.7K pull-up is required.
GPIO[7] / SCL0	1	I/O Async Rst(P) I/O OD Rst(M)	GENERAL PURPOSE INPUT/OUTPUT. These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. I²C CLOCK provides synchronous operation of the I ² C bus. This is one of two I ² C buses that the user may enable. 2.7K pull-up is required.
TCK	1	I Rst(T)	TEST CLOCK is an input which provides the clocking function for the IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the component on the rising edge and data is clocked out of the component on the falling edge.
TDI	1	I Sync(T) Rst(T)	TEST DATA INPUT is the serial input pin for the JTAG feature. TDI is sampled on the rising edge of TCK , during the SHIFT-IR and SHIFT-DR states of the Test Access Port. This signal has a weak internal pull-up to ensure proper operation when this signal is unconnected.
TDO	1	O Sync(T) Rst(T)	TEST DATA OUTPUT is the serial output pin for the JTAG feature. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, TDO floats. The behavior of TDO is independent of P_RST# .

Table 7. Miscellaneous Signals (Sheet 2 of 2)

Name	Count	Type	Description
TRST#	1	I Asyn Rst(T)	TEST RESET asynchronously resets the Test Access Port (TAP) controller function of IEEE 1149.1 Boundary Scan Testing (JTAG). This signal has a weak internal pull-up.
TMS	1	I Sync(T) Rst(T)	TEST MODE SELECT is sampled at the rising edge of TCK to select the operation of the test logic for IEEE 1149.1 Boundary Scan testing. This signal has a weak internal pull-up to ensure proper operation when this signal is unconnected.
RCOMP	1	I	RESISTER COMPENSATION is connected through a 30.1 Ω 1% 1/4 W resistor to ground. This is used to minimize the PCI pin variations due to voltage and temperature variations.
PWRDELAY	1	I Asyn	POWER FAIL DELAY is used with external delay circuits to delay the reset of the memory controller in a power-fail condition. This allows the self-refresh command to be sent to the DDR SDRAM array.
POR#	1	I	POWER ON RESET should be tied to the 1.3 V supply. It is used to provide clocks to the core from an internal ring oscillator during power up, which prevents internal contention. It also tristates the other pins to prevent external power sequencing contention.
NC[2:0]	3	I/O	NO CONNECT pins have no usable function. However they are in the boundary scan chain and must not be connected to any signal, power or ground.
V _{CCPLL1}	1	PWR	PLL POWER is a separate V _{CC13} supply ball for the phase lock loop clock generator. It is to be connected to the board V _{CC13} plane. In noisy environments, add a simple bypass filter circuit to reduce noise-induced clock jitter and its effects on timing relationships.
V _{CCPLL2}	1	PWR	PLL POWER is a separate V _{CC13} supply ball for the phase lock loop clock generator. It is to be connected to the board V _{CC13} plane. In noisy environments, add a simple bypass filter circuit to reduce noise-induced clock jitter and its effects on timing relationships.
V _{CC33}	51	PWR	3.3 V POWER balls to be connected to a 3.3 V power board plane.
V _{CC25}	38	PWR	2.5 V POWER balls to be connected to a 2.5 V power board plane.
V _{CC13}	34	PWR	1.3 V POWER balls to be connected to a 1.3 V power board plane.
V _{SS}	118	GND	GROUND balls to be connected to a ground board plane.

Table 8. Pin Mode Behavior (Sheet 1 of 2)

Pin	Reset	Norm	Hold	32-Bit PCI	32-Bit Mem	ECC Off
RCVENI#	VI	VI	-	-	-	-
RCVENO#	1*	VO	-	-	-	-
M_CK[2:0]	VO	VO	-	-	-	-
M_CK[2:0]#	VO	VO	-	-	-	-
M_RST#	0	VO	-	-	-	-
SA[12:0]	0*	VO	-	-	-	-
SBA[1:0]	0*	VO	-	-	-	-
SRAS#	1*	VO	-	-	-	-
SCAS#	1*	VO	-	-	-	-
SWE#	1*	VO	-	-	-	-
SCE[1:0]#	1*	VO	-	-	-	-
SCKE[1:0]	0*	VO	-	-	-	-
DQ[63:32]	Z*	VB	-	-	ID	-
Q[31:0]	Z*	VB	-	-	-	-
SCB[7:0]	Z*	VB	-	-	-	ID
DQS[7:4]	Z*	VB	-	-	ID	-
DQS[3:0]	Z*	VB	-	-	-	-
DQS[8]	Z*	VB	-	-	-	ID
SDQM[7:4]	Z*	VO	-	-	Z	-
SDQM[3:0]	Z*	VO	-	-	-	-
SDQM[8]	Z*	VO	-	-	-	Z
AD[31:16]	0	VB	Z	-	-	-
AD[15:8]	0	VB	Z	-	-	-
AD[7:0]	0	VB	Z	-	-	-
A[3:2]	0	VO	Z	-	-	-
BE[3:0]#	1	VO	Z	-	-	-
ALE	0	VO	Z	-	-	-
ADS#	1	VO	Z	-	-	-
PB_CLK	VO	VO	-	-	-	-
W/R#	0	VO	Z	-	-	-
FWE#	1	VO	Z	-	-	-
DEN#	1	VO	Z	-	-	-
BLAST#	1	VO	Z	-	-	-
RDYRCV#	VO	VI	-	-	-	-
HOLD	VI	VI	-	-	-	-
HOLDA	VO	VO	1	-	-	-
PB_RST#	0	VO	-	-	-	-
PCE[5]# / PBI100MHZ#	H	VO	1	-	-	-
PCE[4]# / PBI66MHZ#	H	VO	1	-	-	-
PCE[3]# / P_BOOT16#	H	VO	1	-	-	-
PCE[2]# / 32BITPCI#	H	VO	1	-	-	-
PCE[1]# / RETRY	H	VO	1	-	-	-
PCE[0]# / RST_MODE#	H	VO	1	-	-	-
WIDTH[1:0]	0	VO	Z	-	-	-

Table 8. Pin Mode Behavior (Sheet 2 of 2)

Pin	Reset	Norm	Hold	32-Bit PCI	32-Bit Mem	ECC Off
P_AD[63:32]	Z	VB	-	H	-	-
P_AD[31:16]	Z	VB	-	-	-	-
P_AD[15:0]	Z	VB	-	-	-	-
P_PAR	Z	VB	-	-	-	-
P_PAR64	Z	VB	-	H	-	-
P_C/BE[3:0]#	Z	VB	-	-	-	-
P_C/BE[7:4]#	Z	VB	-	H	-	-
P_REQ#	Z	VO	-	-	-	-
P_REQ64#	Z	VB	-	-	-	-
P_GNT#	VI	VI	-	-	-	-
P_ACK64#	Z	VB	-	-	-	-
P_FRAME#	VI	VB	-	-	-	-
P_IRDY#	VI	VB	-	-	-	-
P_TRDY#	VI	VB	-	-	-	-
P_STOP#	VI	VB	-	-	-	-
P_DEVSEL#	VI	VB	-	-	-	-
P_SERR#	Z	VB	-	-	-	-
P_CLK	VI	VI	-	-	-	-
P_RST#	VI	VI	-	-	-	-
P_PERR#	Z	VB	-	-	-	-
P_IDSEL	VI	VI	-	-	-	-
P_INT[A:D]#	Z	VO	-	-	-	-
P_M66EN	VI	VI	-	-	-	-
SSCKO	VO	VO	-	-	-	-
SFRM	VO	VO	-	-	-	-
TXD	VO	VO	-	-	-	-
RXD	VI	VI	-	-	-	-
SSCKI	VI	VI	-	-	-	-
P_BMI	0	VO	-	-	-	-
XINT[3:0]#	VI	VI	-	-	-	-
HPI#	VI	VI	-	-	-	-
GPIO[7]	VI	VB	-	-	-	-
GPIO[6]	VI	VB	-	-	-	-
GPIO[5]	VI	VB	-	-	-	-
GPIO[4:0]	VI	VB	-	-	-	-
TCK	VI	VI	-	-	-	-
TDI	H	H	-	-	-	-
TDO	Z	VO	-	-	-	-
TRST#	H	H	-	-	-	-
TMS	H	H	-	-	-	-
PWRDELAY	VI	VI	-	-	-	-
NC[2:0]	H	H	-	-	-	-

NOTES:

1 = driven to V_{CC}
0 = driven to V_{SS}
X = driven to unknown state
ID = The input is disabled
H = pulled up to V_{CC}
PD = pull-up disabled

NOTES:(continued)

L = pulled down to V_{SS}
Z = output disabled (Floats)
VB = acts like a Valid Bidirectional pin.
VO = a Valid Output level is driven.
VI = Need to drive a Valid Input level.
* = After power fail sequence completes.
** = Caused by Hi-Z from mode pins only.

Figure 3. 544-Lead PBGA Package (Bottom View)



Figure 4. Ball Map - Left Side - Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	SA1	DQ35	DQ38	DQ34	DQ33	VREF	SCB3	SDQM ₈	SCB0	SA2	DQ30T	SDQM ₃	DQ28
B	SA0	DQ39	VSS	DQS4	VSS	REV VENO#	VSS	DQS8	VSS	SA3	VSS	DQ29	VSS
C	SA10	VSS	VCC25	SDQM ₄	DQ36	VCC25	SCB7	SCB1	VCC25	SA4	DQ27	VCC25	DQ24
D	SRAS#	SBA0	SBA1	VSS	DQ37	DQ32	REV VENI#	SCB2	SCB5	DQ31	DQ26	DQ25	SA6
E	DQ45	VSS	DQ44	DQ40	VCC25	VSS	SCB6	VSS	SCB4	VSS	DQ53	VSS	SA5
F	SDQM5	DQS5	VCC25	DQ41	VSS	VCC25	VCC25	VCC25	VCC25	VCC25	VCC25	VCC25	VCC25
G	DQ46	VSS	DQ47	DQ43	DQ42	VCC25	VCC13	VCC13	VCC13	VCC13			
H	DQ49	DQ48	SCAS#	SWE#	VSS	VCC25	VCC13						
J	DQS6	VSS	VCC25	DQ53	DQ52	VCC25	VCC13						
K	DQ50	DQ54	SDQM6	DQ55	VSS	VCC25	VCC13						
L	DQ60	VSS	DQ51	SCE1#	SCE0#	VCC25					VSS	VSS	VSS
M	DQ57	DQ61	VCC25	DQ56	VSS	VCC25					VSS	VSS	VSS
N	DQ62	VSS	DQ58	SDQM7	DQS7	VCC25					VSS	VSS	VSS
P	DQ59	M _{CK2} #	M _{CK2}	DQ63	VSS	VCC25					VSS	VSS	VSS
R	M _{CK1}	VSS	VCC13	M _{CK0} #	M _{CK0}	VCC25					VSS	VSS	VSS
T	M _{CK1} #	P _{INTB} #	P _{INTA} #	R _{COMP}	VSS	VCC33					VSS	VSS	VSS
U	P _{INTD} #	VSS	R _{REQ} #	R _{INTC} #	R _{RST} #	VCC33	VCC13						
V	P _{AD31}	P _{GNT} #	VCC33	P _{AD30}	VSS	VCC33	VCC13						
W	P _{AD29}	VSS	P _{AD27}	P _{AD28}	P _{AD26}	VCC33	VCC13						
Y	P _{AD25}	P _{CBE3} #	P _{AD24}	P _{IDSEL}	VSS	VCC33	VCC13	VCC13	VCC13	VCC13			
AA	P _{AD23}	VSS	VCC33	P _{AD22}	P _{AD20}	VCC33	VCC33	VCC33	VCC33	VCC33	VCC33	VCC13	VCC33
AB	P _{AD19}	P _{AD21}	P _{AD18}	P _{AD16}	VSS	P _{AD9}	VSS	P _{AD4}	VSS	P _{CBE7} #	VSS	P _{AD62}	VSS
AC	P _{AD17}	VSS	P _{FRAME} #	P _{TRDY} #	P _{AD13}	P _{CBE0} #	P _{CLK}	P _{AD2}	P _{AD0}	P _{REQ64} #	P _{PAR64}	P _{CBE4} #	P _{AD58}
AD	P _{CBE2} #	P _{STOP} #	VCC33	P _{AD15}	P _{AD11}	VCC33	P _{AD6}	P _{M66EN}	VCC33	P _{AD3}	P _{CBE5} #	VCC33	P _{AD60}
AE	P _{IRDY} #	VSS	P _{PAR}	VSS	P _{AD14}	VSS	VCC _{PLL2}	VSS	P _{AD7}	VSS	P _{ACK64} #	VSS	P _{AD61}
AF	P _{DEVSEL} #	P _{PERR} #	P _{SERR} #	P _{CBE1} #	VCC _{PLL1}	P _{AD12}	P _{AD10}	P _{AD8}	P _{AD5}	P _{AD1}	P _{CBE6} #	P _{AD63}	P _{AD59}
	1	2	3	4	5	6	7	8	9	10	11	12	13

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Figure 5. Ball Map - Right Side - Top View

14	15	16	17	18	19	20	21	22	23	24	25	26	
SA8	DQ18	DQS2	DQ20	SCKE0	DQ14	DQS1	DQS8	DQS6	DQS0	DQ5	DQ0	AD31	A
SA7	VSS	DQ21	VSS	SCKE1	VSS	DQ13	VSS	DQ2	VSS	DQ4	VSS	AD30	B
DQ23	VCC25	DQ17	SA9	VCC25	SDQM1	DQ12	VCC25	SDQM0	DQ1	VCC25	AD29	AD28	C
DQ19	SDQM2	DQ16	SA11	DQ11	DQ15	DQ9	M-RST#	DQ7	AD25	AD27	VSS	AD26	D
VSS	DQ22	VSS	SA12	VSS	DQ10	VSS	DQ3	VSS	BE3#	AD22	AD24	AD23	E
VCC25	VCC25	VCC25	VCC25	VCC25	VCC25	VCC25	VCC25	BE2#	AD21	VCC23	VSS	AD20	F
			VCC13	VCC13	VCC13	VCC13	VCC33	VSS	BE1#	AD17	AD19	AD18	G
						VCC13	VCC33	WIDTH 1	AD14	AD16	VSS	AD15	H
						VCC13	VCC33	VSS	AD11	VCC33	AD13	AD12	J
						VCC13	VCC33	WIDTH 0	AD8	AD10	VSS	AD9	K
VSS	VSS	VSS					VCC33	VSS	BE0#	AD5	AD7	AD8	L
VSS	VSS	VSS					VCC13	A3	AD4	VCC33	VSS	AD3	M
VSS	VSS	VSS					VCC33	VSS	A2	AD0	AD2	AD1	N
VSS	VSS	VSS					VCC13	FWE#	WIR#	ADS#	VSS	ALE	P
VSS	VSS	VSS					VCC33	VSS	RDY RCV#	VCC33	BLAST #	DEN#	R
VSS	VSS	VSS						PB_RST#	HOLDA	HOLD	VSS	PB_CLK	T
						VCC13	VCC33	VSS	PCE5#	PCE4#	PCE3#	PCE2#	U
						VCC13	VCC33	PCE0#	NC0	VCC33	VSS	PCE1#	V
						VCC13	VCC33	VSS	GPIO7	GPIO6	GPIO5	GPIO4	W
			VCC13	VCC13	VCC13	VCC13	VCC33	GPIO3	GPIO2	GPIO1	VSS	GPIO0	Y
VCC13	VCC33	VCC13	VCC33	VCC33	VCC33	VCC33	VCC33	VSS	SFRM	VCC33	RXD	TXD	AA
P_AD54	VSS	P_AD48	VSS	P_AD40	VSS	P_AD32	VSS	VCC33	HPI#	SSCKI	VSS	SSCKO	AB
P_AD56	P_AD52	P_AD50	P_AD44	P_AD42	P_AD36	P_AD34	TDO	TRST#	VSS	XINT 3#	XINT 2#	XINT 1#	AC
P_AD57	VCC33	P_AD49	P_AD46	VCC33	P_AD38	P_AD35	VCC33	TCK	NC1	VCC33	VSS	XINT 0#	AD
VSS	P_AD53	VSS	P_AD45	VSS	P_AD39	VSS	TDI	VSS	P_BMI	VSS	VCC33	VCC33	AE
P_AD55	P_AD51	P_AD47	P_AD43	P_AD41	P_AD37	P_AD33	POR#	TMS	PWR DELAY	VCC33	VCC33	VCC33	AF
14	15	16	17	18	19	20	21	22	23	24	25	26	

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Table 9. 544-Lead PBGA Package - Alphabetical Ball Listing (Sheet 1 of 5)

Ball	Signal	Ball	Signal	Ball	Signal
A1	SA1	B13	V _{SS}	C25	AD29
A2	DQ35	B14	SA7	C26	AD28
A3	DQ38	B15	V _{SS}	D1	SRAS#
A4	DQ34	B16	DQ21	D2	SBA0
A5	DQ33	B17	V _{SS}	D3	SBA1
A6	V _{REF}	B18	SCKE1	D4	V _{SS}
A7	SCB3	B19	V _{SS}	D5	DQ37
A8	SDQM8	B20	DQ13	D6	DQ32
A9	SCB0	B21	V _{SS}	D7	RCVENI#
A10	SA2	B22	DQ2	D8	SCB2
A11	DQ30	B23	V _{SS}	D9	SCB5
A12	SDQM3	B24	DQ4	D10	DQ31
A13	DQ28	B25	V _{SS}	D11	DQ26
A14	SA8	B26	AD30	D12	DQ25
A15	DQ18	C1	SA10	D13	SA6
A16	DQS2	C2	V _{SS}	D14	DQ19
A17	DQ20	C3	V _{CC25}	D15	SDQM2
A18	SCKE0	C4	SDQM4	D16	DQ16
A19	DQ14	C5	DQ36	D17	SA11
A20	DQS1	C6	V _{CC25}	D18	DQ11
A21	DQ8	C7	SCB7	D19	DQ15
A22	DQ6	C8	SCB1	D20	DQ9
A23	DQS0	C9	V _{CC25}	D21	M_RST#
A24	DQ5	C10	SA4	D22	DQ7
A25	DQ0	C11	DQ27	D23	AD25
A26	AD31	C12	V _{CC25}	D24	AD27
B1	SA0	C13	DQ24	D25	V _{SS}
B2	DQ39	C14	DQ23	D26	AD26
B3	V _{SS}	C15	V _{CC25}	E1	DQ45
B4	DQS4	C16	DQ17	E2	V _{SS}
B5	V _{SS}	C17	SA9	E3	DQ44
B6	RCVENO#	C18	V _{CC25}	E4	DQ40
B7	V _{SS}	C19	SDQM1	E5	V _{CC25}
B8	DQS8	C20	DQ12	E6	V _{SS}
B9	V _{SS}	C21	V _{CC25}	E7	SCB6
B10	SA3	C22	SDQM0	E8	V _{SS}
B11	V _{SS}	C23	DQ1	E9	SCB4
B12	DQ29	C24	V _{CC25}	E10	V _{SS}

Table 9. 544-Lead PBGA Package - Alphabetical Ball Listing (Sheet 2 of 5)

Ball	Signal	Ball	Signal	Ball	Signal
E11	DQS3	F23	AD21	J1	DQS6
E12	V _{SS}	F24	V _{CC33}	J2	V _{SS}
E13	SA5	F25	V _{SS}	J3	V _{CC25}
E14	V _{SS}	F26	AD20	J4	DQ53
E15	DQ22	G1	DQ46	J5	DQ52
E16	V _{SS}	G2	V _{SS}	J6	V _{CC25}
E17	SA12	G3	DQ47	J7	V _{CC13}
E18	V _{SS}	G4	DQ43	J20	V _{CC13}
E19	DQ10	G5	DQ42	J21	V _{CC33}
E20	V _{SS}	G6	V _{CC25}	J22	V _{SS}
E21	DQ3	G7	V _{CC13}	J23	AD11
E22	V _{SS}	G8	V _{CC13}	J24	V _{CC33}
E23	BE3#	G9	V _{CC13}	J25	AD13
E24	AD22	G10	V _{CC13}	J26	AD12
E25	AD24	G17	V _{CC13}	K1	DQ50
E26	AD23	G18	V _{CC13}	K2	DQ54
F1	SDQM5	G19	V _{CC13}	K3	SDQM6
F2	DQS5	G20	V _{CC13}	K4	DQ55
F3	V _{CC25}	G21	V _{CC33}	K5	V _{SS}
F4	DQ41	G22	V _{SS}	K6	V _{CC25}
F5	V _{SS}	G23	BE1#	K7	V _{CC13}
F6	V _{CC25}	G24	AD17	K20	V _{CC13}
F7	V _{CC25}	G25	AD19	K21	V _{CC33}
F8	V _{CC25}	G26	AD18	K22	WIDTH0
F9	V _{CC25}	H1	DQ49	K23	AD8
F10	V _{CC25}	H2	DQ48	K24	AD10
F11	V _{CC25}	H3	SCAS#	K25	V _{SS}
F12	V _{CC25}	H4	SWE#	K26	AD9
F13	V _{CC25}	H5	V _{SS}	L1	DQ60
F14	V _{CC25}	H6	V _{CC25}	L2	V _{SS}
F15	V _{CC25}	H7	V _{CC13}	L3	DQ51
F16	V _{CC25}	H20	V _{CC13}	L4	SCE1#
F17	V _{CC25}	H21	V _{CC33}	L5	SCE0#
F18	V _{CC25}	H22	WIDTH1	L6	V _{CC25}
F19	V _{CC25}	H23	AD14	L11	V _{SS}
F20	V _{CC25}	H24	AD16	L12	V _{SS}
F21	V _{CC25}	H25	V _{SS}	L13	V _{SS}
F22	BE2#	H26	AD15	L14	V _{SS}

Table 9. 544-Lead PBGA Package - Alphabetical Ball Listing (Sheet 3 of 5)

Ball	Signal	Ball	Signal	Ball	Signal
L15	V _{SS}	N21	V _{CC33}	R23	RDYRCV#
L16	V _{SS}	N22	V _{SS}	R24	V _{CC33}
L21	V _{CC33}	N23	A2	R25	BLAST#
L22	V _{SS}	N24	AD0	R26	DEN#
L23	BE0#	N25	AD2	T1	M_CK1#
L24	AD5	N26	AD1	T2	P_INTB#
L25	AD7	P1	DQ59	T3	P_INTA#
L26	AD6	P2	M_CK2#	T4	RCOMP
M1	DQ57	P3	M_CK2	T5	V _{SS}
M2	DQ61	P4	DQ63	T6	V _{CC33}
M3	V _{CC25}	P5	V _{SS}	T11	V _{SS}
M4	DQ56	P6	V _{CC25}	T12	V _{SS}
M5	V _{SS}	P11	V _{SS}	T13	V _{SS}
M6	V _{CC25}	P12	V _{SS}	T14	V _{SS}
M11	V _{SS}	P13	V _{SS}	T15	V _{SS}
M12	V _{SS}	P14	V _{SS}	T16	V _{SS}
M13	V _{SS}	P15	V _{SS}	T21	V _{CC13}
M14	V _{SS}	P16	V _{SS}	T22	PB_RST#
M15	V _{SS}	P21	V _{CC13}	T23	HOLDA
M16	V _{SS}	P22	FWE#	T24	HOLD
M21	V _{CC13}	P23	W/R#	T25	V _{SS}
M22	A3	P24	ADS#	T26	PB_CLK
M23	AD4	P25	V _{SS}	U1	P_INTD#
M24	V _{CC33}	P26	ALE	U2	V _{SS}
M25	V _{SS}	R1	M_CK1	U3	P_REQ#
M26	AD3	R2	V _{SS}	U4	P_INTC#
N1	DQ62	R3	V _{CC25}	U5	P_RST#
N2	V _{SS}	R4	M_CK0#	U6	V _{CC33}
N3	DQ58	R5	M_CK0	U7	V _{CC13}
N4	SDQM7	R6	V _{CC25}	U20	V _{CC13}
N5	DQS7	R11	V _{SS}	U21	V _{CC33}
N6	V _{CC25}	R12	V _{SS}	U22	V _{SS}
N11	V _{SS}	R13	V _{SS}	U23	PCE5#
N12	V _{SS}	R14	V _{SS}	U24	PCE4#
N13	V _{SS}	R15	V _{SS}	U25	PCE3#
N14	V _{SS}	R16	V _{SS}	U26	PCE2#
N15	V _{SS}	R21	V _{CC33}	V1	P_AD31
N16	V _{SS}	R22	V _{SS}	V2	P_GNT#

Table 9. 544-Lead PBGA Package - Alphabetical Ball Listing (Sheet 4 of 5)

Ball	Signal	Ball	Signal	Ball	Signal
V3	V _{CC33}	Y19	V _{CC13}	AB5	V _{SS}
V4	P_AD30	Y20	V _{CC13}	AB6	P_AD9
V5	V _{SS}	Y21	V _{CC33}	AB7	V _{SS}
V6	V _{CC33}	Y22	GPIO3	AB8	P_AD\$
V7	V _{CC13}	Y23	GPIO2	AB9	V _{SS}
V20	V _{CC13}	Y24	GPIO1	AB10	P_CBE7#
V21	V _{CC33}	Y25	V _{SS}	AB11	V _{SS}
V22	PCE0#	Y26	GPIO0	AB12	P_AD62
V23	NC0	AA1	P_AD23	AB13	V _{SS}
V24	V _{CC33}	AA2	V _{SS}	AB14	P_AD54
V25	V _{SS}	AA3	V _{CC33}	AB15	V _{SS}
V26	PCE1#	AA4	P_AD22	AB16	P_AD48
W1	P_AD29	AA5	P_AD20	AB17	V _{SS}
W2	V _{SS}	AA6	V _{CC33}	AB18	P_AD40
W3	P_AD27	AA7	V _{CC33}	AB19	V _{SS}
W4	P_AD28	AA8	V _{CC33}	AB20	P_AD32
W5	P_AD26	AA9	V _{CC33}	AB21	V _{SS}
W6	V _{CC33}	AA10	V _{CC33}	AB22	V _{CC33}
W7	V _{CC13}	AA11	V _{CC33}	AB23	HPI#
W20	V _{CC13}	AA12	V _{CC13}	AB24	SSCKI
W21	V _{CC33}	AA13	V _{CC33}	AB25	V _{SS}
W22	V _{SS}	AA14	V _{CC13}	AB26	SSCKO
W23	GPIO7	AA15	V _{CC33}	AC1	P_AD17
W24	GPIO6	AA16	V _{CC13}	AC2	V _{SS}
W25	GPIO5	AA17	V _{CC33}	AC3	P_FRAME#
W26	GPIO4	AA18	V _{CC33}	AC4	P_TRDY#
Y1	P_AD25	AA19	V _{CC33}	AC5	P_AD13
Y2	P_CBE3#	AA20	V _{CC33}	AC6	P_CBE0#
Y3	P_AD24	AA21	V _{CC33}	AC7	P_CLK
Y4	P_IDSEL	AA22	V _{SS}	AC8	P_AD2
Y5	V _{SS}	AA23	SFRM	AC9	P_AD0
Y6	V _{CC33}	AA24	V _{CC33}	AC10	P_REQ64#
Y7	V _{CC13}	AA25	RXD	AC11	P_PAR64
Y8	V _{CC13}	AA26	TXD	AC12	P_CBE4#
Y9	V _{CC13}	AB1	P_AD19	AC13	P_AD58
Y10	V _{CC13}	AB2	P_AD21	AC14	P_AD56
Y17	V _{CC13}	AB3	P_AD18	AC15	P_AD52
Y18	V _{CC13}	AB4	P_AD16	AC16	P_AD50

Table 9. 544-Lead PBGA Package - Alphabetical Ball Listing (Sheet 5 of 5)

Ball	Signal	Ball	Signal	Ball	Signal
AC17	P_AD44	AD21	V _{CC33}	AE24	V _{SS}
AC18	P_AD42	AD22	TCK	AE25	V _{CC33}
AC19	P_AD36	AD23	NC1	AE26	V _{CC33}
AC20	P_AD34	AD24	V _{CC33}	AF1	P_DEVSEL#
AC21	TDO	AD25	V _{SS}	AF2	P_PERR#
AC22	TRST#	AD26	XINT0#	AF3	P_SERR#
AC23	V _{SS}	AE1	P_IRDY#	AF4	P_CBE1#
AC24	XINT3#	AE2	V _{SS}	AF5	V _{CCPLL1}
AC25	XINT2#	AE3	P_PAR	AF6	P_AD12
AC26	XINT1#	AE4	V _{SS}	AF7	P_AD10
AD1	P_CBE2#	AE5	P_AD14	AF8	P_AD8
AD2	P_STOP#	AE6	V _{SS}	AF9	P_AD5
AD3	V _{CC33}	AE7	V _{CCPLL2}	AF10	P_AD1
AD4	P_AD15	AE8	V _{SS}	AF11	P_CBE6#
AD5	P_AD11	AE9	P_AD7	AF12	P_AD63
AD6	V _{CC33}	AE10	V _{SS}	AF13	P_AD59
AD7	P_AD6	AE11	P_ACK64#	AF14	P_AD55
AD8	P_M66EN	AE12	V _{SS}	AF15	P_AD51
AD9	V _{CC33}	AE13	P_AD61	AF16	P_AD47
AD10	P_AD3	AE14	V _{SS}	AF17	P_AD43
AD11	P_CBE5#	AE15	P_AD53	AF18	P_AD41
AD12	V _{CC33}	AE16	V _{SS}	AF19	P_AD37
AD13	P_AD60	AE17	P_AD45	AF20	P_AD33
AD14	P_AD57	AE18	V _{SS}	AF21	POR#
AD15	V _{CC33}	AE19	P_AD39	AF22	TMS
AD16	P_AD49	AE20	V _{SS}	AF23	PWRDELAY
AD17	P_AD46	AE21	TDI	AF24	V _{CC33}
AD18	V _{CC33}	AE22	V _{SS}	AF25	V _{CC33}
AD19	P_AD38	AE23	P_BMI	AF26	V _{CC33}
AD20	P_AD35				

Table 10. 544-Lead PBGA Package - Alphabetical Signal Listing (Sheet 1 of 5)

Signal	Ball	Signal	Ball	Signal	Ball
A2	N23	BE2#	F22	DQ34	A4
A3	M22	BE3#	E23	DQ35	A2
AD0	N24	BLAST#	R25	DQ36	C5
AD1	N26	DEN#	R26	DQ37	D5
AD2	N25	DQ0	A25	DQ38	A3
AD3	M26	DQ1	C23	DQ39	B2
AD4	M23	DQ2	B22	DQ40	E4
AD5	L24	DQ3	E21	DQ41	F4
AD6	L26	DQ4	B24	DQ42	G5
AD7	L25	DQ5	A24	DQ43	G4
AD8	K23	DQ6	A22	DQ44	E3
AD9	K26	DQ7	D22	DQ45	E1
AD10	K24	DQ8	A21	DQ46	G1
AD11	J23	DQ9	D20	DQ47	G3
AD12	J26	DQ10	E19	DQ48	H2
AD13	J25	DQ11	D18	DQ49	H1
AD14	H23	DQ12	C20	DQ50	K1
AD15	H26	DQ13	B20	DQ51	L3
AD16	H24	DQ14	A19	DQ52	J5
AD17	G24	DQ15	D19	DQ53	J4
AD18	G26	DQ16	D16	DQ54	K2
AD19	G25	DQ17	C16	DQ55	K4
AD20	F26	DQ18	A15	DQ56	M4
AD21	F23	DQ19	D14	DQ57	M1
AD22	E24	DQ20	A17	DQ58	N3
AD23	E26	DQ21	B16	DQ59	P1
AD24	E25	DQ22	E15	DQ60	L1
AD25	D23	DQ23	C14	DQ61	M2
AD26	D26	DQ24	C13	DQ62	N1
AD27	D24	DQ25	D12	DQ63	P4
AD28	C26	DQ26	D11	DQS0	A23
AD29	C25	DQ27	C11	DQS1	A20
AD30	B26	DQ28	A13	DQS2	A16
AD31	A26	DQ29	B12	DQS3	E11
ADS#	P24	DQ30	A11	DQS4	B4
ALE	P26	DQ31	D10	DQS5	F2
BE0#	L23	DQ32	D6	DQS6	J1
BE1#	G23	DQ33	A5	DQS7	N5

Table 10. 544-Lead PBGA Package - Alphabetical Signal Listing (Sheet 2 of 5)

Signal	Ball	Signal	Ball	Signal	Ball
DQS8	B8	P_AD14	AE5	P_AD52	AC15
FWE#	P22	P_AD15	AD4	P_AD53	AE15
GPIO0	Y26	P_AD16	AB4	P_AD54	AB14
GPIO1	Y24	P_AD17	AC1	P_AD55	AF14
GPIO2	Y23	P_AD18	AB3	P_AD56	AC14
GPIO3	Y22	P_AD19	AB1	P_AD57	AD14
GPIO4	W26	P_AD20	AA5	P_AD58	AC13
GPIO5	W25	P_AD21	AB2	P_AD59	AF13
GPIO6	W24	P_AD22	AA4	P_AD60	AD13
GPIO7	W23	P_AD23	AA1	P_AD61	AE13
HOLD	T24	P_AD24	Y3	P_AD62	AB12
HOLDA	T23	P_AD25	Y1	P_AD63	AF12
HPI#	AB23	P_AD26	W5	P_CBE0#	AC6
M_CK0	R5	P_AD27	W3	P_CBE1#	AF4
M_CK0#	R4	P_AD28	W4	P_CBE2#	AD1
M_CK1	R1	P_AD29	W1	P_CBE3#	Y2
M_CK1#	T1	P_AD30	V4	P_CBE4#	AC12
M_CK2	P3	P_AD31	V1	P_CBE5#	AD11
M_CK2#	P2	P_AD32	AB20	P_CBE6#	AF11
M_RST#	D21	P_AD33	AF20	P_CBE7#	AB10
NC0	V23	P_AD34	AC20	P_CLK	AC7
NC1	AD23	P_AD35	AD20	P_DEVSEL#	AF1
P_BMI	AE23	P_AD36	AC19	P_FRAME#	AC3
P_ACK64#	AE11	P_AD37	AF19	P_GNT#	V2
P_AD0	AC9	P_AD38	AD19	P_IDSEL	Y4
P_AD1	AF10	P_AD39	AE19	P_INTA#	T3
P_AD2	AC8	P_AD40	AB18	P_INTB#	T2
P_AD3	AD10	P_AD41	AF18	P_INTC#	U4
P_AD4	AB8	P_AD42	AC18	P_INTD#	U1
P_AD5	AF9	P_AD43	AF17	P_IRDY#	AE1
P_AD6	AD7	P_AD44	AC17	P_M66EN	AD8
P_AD7	AE9	P_AD45	AE17	P_PAR	AE3
P_AD8	AF8	P_AD46	AD17	P_PAR64	AC11
P_AD9	AB6	P_AD47	AF16	P_PERR#	AF2
P_AD10	AF7	P_AD48	AB16	P_REQ#	U3
P_AD11	AD5	P_AD49	AD16	P_REQ64#	AC10
P_AD12	AF6	P_AD50	AC16	P_RST#	U5
P_AD13	AC5	P_AD51	AF15	P_SERR#	AF3

Table 10. 544-Lead PBGA Package - Alphabetical Signal Listing (Sheet 3 of 5)

Signal	Ball	Signal	Ball	Signal	Ball
P_STOP#	AD2	SCB4	E9	V _{CC13}	J20
P_TRDY#	AC4	SCB5	D9	V _{CC13}	K7
PB_CLK	T26	SCB6	E7	V _{CC13}	K20
PB_RST#	T22	SCB7	C7	V _{CC13}	U7
PCE0#	V22	SCKE0	A18	V _{CC13}	U20
PCE1#	V26	SCKE1	B18	V _{CC13}	V7
PCE2#	U26	SCE0#	L5	V _{CC13}	W7
PCE3#	U25	SCE1#	L4	V _{CC13}	W20
PCE4#	U24	SDQM0	C22	V _{CC13}	Y7
PCE5#	U23	SDQM1	C19	V _{CC13}	Y8
POR#	AF21	SDQM2	D15	V _{CC13}	Y9
PWRDELAY	AF23	SDQM3	A12	V _{CC13}	Y10
SRAS#	D1	SDQM4	C4	V _{CC13}	Y17
RCOMP	T4	SDQM5	F1	V _{CC13}	Y19
RCVENI#	D7	SDQM6	K3	V _{CC13}	Y20
RCVENO#	B6	SDQM7	N4	V _{CC13}	M21
RDYRCV#	R23	SDQM8	A8	V _{CC13}	P21
RXD	AA25	SFRM	AA23	V _{CC13}	T21
SA0	B1	SSCKI	AB24	V _{CC13}	V20
SA1	A1	SSCKO	AB26	V _{CC13}	Y18
SA2	A10	TCK	AD22	V _{CC13}	AA12
SA3	B10	TDI	AE21	V _{CC13}	AA14
SA4	C10	TDO	AC21	V _{CC13}	AA16
SA5	E13	TMS	AF22	V _{CC25}	C3
SA6	D13	TRST#	AC22	V _{CC25}	C6
SA7	B14	TXD	AA26	V _{CC25}	C9
SA8	A14	V _{CC25}	F20	V _{CC25}	C12
SA9	C17	V _{CC13}	G7	V _{CC25}	C15
SA10	C1	V _{CC13}	G8	V _{CC25}	C18
SA11	D17	V _{CC13}	G9	V _{CC25}	C21
SA12	E17	V _{CC13}	G10	V _{CC25}	C24
SBA0	D2	V _{CC13}	G17	V _{CC25}	E5
SBA1	D3	V _{CC13}	G18	V _{CC25}	F3
SCAS#	H3	V _{CC13}	G19	V _{CC25}	F6
SCB0	A9	V _{CC13}	G20	V _{CC25}	F7
SCB1	C8	V _{CC13}	H7	V _{CC25}	F8
SCB2	D8	V _{CC13}	H20	V _{CC25}	F9
SCB3	A7	V _{CC13}	J7	V _{CC25}	F10

Table 10. 544-Lead PBGA Package - Alphabetical Signal Listing (Sheet 4 of 5)

Signal	Ball	Signal	Ball	Signal	Ball
V _{CC25}	F11	V _{CC33}	AA21	V _{SS}	B3
V _{CC25}	F12	V _{CC33}	AA24	V _{SS}	B5
V _{CC25}	F13	V _{CC33}	AB22	V _{SS}	B7
V _{CC25}	F14	V _{CC33}	AD24	V _{SS}	B9
V _{CC25}	F15	V _{CC33}	AA3	V _{SS}	B11
V _{CC25}	F16	V _{CC33}	AA6	V _{SS}	B13
V _{CC25}	F17	V _{CC33}	AA7	V _{SS}	B15
V _{CC25}	F18	V _{CC33}	AA8	V _{SS}	B17
V _{CC25}	F19	V _{CC33}	AA9	V _{SS}	B19
V _{CC25}	F21	V _{CC33}	AA10	V _{SS}	B21
V _{CC25}	G6	V _{CC33}	AA11	V _{SS}	B23
V _{CC25}	H6	V _{CC33}	AA13	V _{SS}	B25
V _{CC25}	J3	V _{CC33}	AA15	V _{SS}	C2
V _{CC25}	J6	V _{CC33}	AA17	V _{SS}	D25
V _{CC25}	K6	V _{CC33}	AA18	V _{SS}	D4
V _{CC25}	L6	V _{CC33}	AA19	V _{SS}	E2
V _{CC25}	M3	V _{CC33}	AA20	V _{SS}	E6
V _{CC25}	M6	V _{CC33}	AD3	V _{SS}	E8
V _{CC25}	N6	V _{CC33}	AD6	V _{SS}	E10
V _{CC25}	P6	V _{CC33}	AD9	V _{SS}	E12
V _{CC25}	R3	V _{CC33}	AD12	V _{SS}	E14
V _{CC25}	R6	V _{CC33}	AD15	V _{SS}	E16
V _{CC33}	F24	V _{CC33}	AD18	V _{SS}	E18
V _{CC33}	G21	V _{CC33}	AD21	V _{SS}	E20
V _{CC33}	H21	V _{CC33}	AE25	V _{SS}	E22
V _{CC33}	J21	V _{CC33}	AE26	V _{SS}	F5
V _{CC33}	J24	V _{CC33}	AF24	V _{SS}	F25
V _{CC33}	K21	V _{CC33}	AF25	V _{SS}	G2
V _{CC33}	L21	V _{CC33}	AF26	V _{SS}	G22
V _{CC33}	M24	V _{CC33}	T6	V _{SS}	H5
V _{CC33}	N21	V _{CC33}	U6	V _{SS}	H25
V _{CC33}	R21	V _{CC33}	V3	V _{SS}	J2
V _{CC33}	R24	V _{CC33}	V6	V _{SS}	J22
V _{CC33}	U21	V _{CC33}	W6	V _{SS}	K5
V _{CC33}	V21	V _{CC33}	Y6	V _{SS}	K25
V _{CC33}	V24	V _{CCPLL1}	AF5	V _{SS}	L2
V _{CC33}	W21	V _{CCPLL2}	AE7	V _{SS}	L11
V _{CC33}	Y21	V _{REF}	A6	V _{SS}	L12

Table 10. 544-Lead PBGA Package - Alphabetical Signal Listing (Sheet 5 of 5)

Signal	Ball	Signal	Ball	Signal	Ball
V _{SS}	L13	V _{SS}	R11	V _{SS}	AB15
V _{SS}	L14	V _{SS}	R12	V _{SS}	AB17
V _{SS}	L15	V _{SS}	R13	V _{SS}	AB19
V _{SS}	L16	V _{SS}	R14	V _{SS}	AB21
V _{SS}	L22	V _{SS}	R15	V _{SS}	AB25
V _{SS}	M5	V _{SS}	R16	V _{SS}	AC2
V _{SS}	M11	V _{SS}	R22	V _{SS}	AC23
V _{SS}	M12	V _{SS}	T5	V _{SS}	AD25
V _{SS}	M13	V _{SS}	T11	V _{SS}	AE2
V _{SS}	M14	V _{SS}	T12	V _{SS}	AE4
V _{SS}	M15	V _{SS}	T13	V _{SS}	AE6
V _{SS}	M16	V _{SS}	T14	V _{SS}	AE8
V _{SS}	M25	V _{SS}	T15	V _{SS}	AE10
V _{SS}	N2	V _{SS}	T16	V _{SS}	AE12
V _{SS}	N11	V _{SS}	T25	V _{SS}	AE14
V _{SS}	N12	V _{SS}	U2	V _{SS}	AE16
V _{SS}	N13	V _{SS}	U22	V _{SS}	AE18
V _{SS}	N14	V _{SS}	V5	V _{SS}	AE20
V _{SS}	N15	V _{SS}	V25	V _{SS}	AE22
V _{SS}	N16	V _{SS}	W2	V _{SS}	AE24
V _{SS}	N22	V _{SS}	W22	SWE#	H4
V _{SS}	P5	V _{SS}	Y5	WIDTH00	K22
V _{SS}	P11	V _{SS}	Y25	WIDTH01	H22
V _{SS}	P12	V _{SS}	AA2	W/R#	P23
V _{SS}	P13	V _{SS}	AA22	XINT0#	AD26
V _{SS}	P14	V _{SS}	AB5	XINT1#	AC26
V _{SS}	P15	V _{SS}	AB7	XINT2#	AC25
V _{SS}	P16	V _{SS}	AB9	XINT3#	AC24
V _{SS}	P25	V _{SS}	AB11		
V _{SS}	R2	V _{SS}	AB13		

3.2 Package Thermal Specifications

The device is specified for operation when T_C (case temperature) is within the range of 0 °C to 95 °C, depending on operating conditions. Case temperature can be measured in any environment to determine whether the processor is within specified operating range. Case temperature is best measured at the center of the top surface, opposite the ballpad.

3.2.1 Thermal Characteristics

Table 11 summarizes the thermal simulation data for the 80321.

The thermal performance of the 80321 package is represented by the following parameters:

1. Ψ_{JT} , thermal characterization parameter from junction-to-top center

$$\Psi_{JT} = (T_J - T_T) / P$$

where

— $T_T = T_C$, the temperature of the top-center of the package

— Ψ_{JT} simulations are carried out to show the thermal performance of the 80321.

Table 11. 544-Lead PBGA Package Thermal Characteristics

Thermal Resistance Parameter °C/W	
Parameter	Value
Ψ_{JT}	0.6

3.2.2 Thermal Specifications

This section defines the terms used for thermal analysis.

3.2.2.1 Ambient Temperature

Ambient temperature, T_A , is the temperature of the ambient air surrounding the package. In a system environment, ambient temperature is the temperature of the air upstream from the package.

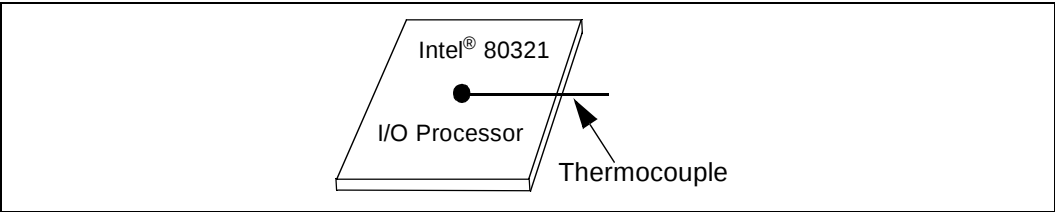
3.2.2.2 Case Temperature

When measuring case temperature, attention to detail is required to ensure accuracy. When a thermocouple is used, calibrate it before taking measurements. Errors may result when the measured surface temperature is affected by the surrounding ambient air temperature. Such errors may be due to a poor thermal contact between thermocouple junction and the surface, heat loss by radiation, or conduction through thermocouple leads.

To minimize measurement errors:

- Use a 35 gauge K-type thermocouple or equivalent.
- Attach the thermocouple bead or junction to the package top surface at a location corresponding to the center of the die (Figure 6). The center of the die gives a more accurate measurement and less variation as the boundary condition changes.
- Attach the thermocouple bead at a 0° angle with respect to the package as shown in Figure 6, when no heatsink is attached.

Figure 6. Thermocouple Attachment—No Heatsink



3.2.3 80321 JTAG Emulator Vendor

Table 12. JTAG Emulator Vendor

Company	Part #
ARM, Ltd. www.arm.com	Multi-ICE Interface Unit ARM KP1-0019A
WindRiver HSI www.windriver.com	visionPROBE/visionICE for Intel XScale® microarchitecture

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Table 13. Absolute Maximum Ratings

Parameter	Maximum Rating	NOTICE: The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design.
Storage temperature	–55° C to +125 °C	
Case temperature under bias	0° C to +95 °C	
Supply voltage V_{CC33} wrt. V_{SS}	–0.5 V to +4.1 V	
Supply voltage V_{CC25} wrt. V_{SS}	–0.5 V to +3.6 V	
Supply voltage V_{CC13} wrt. V_{SS}	–0.5 V to +2.1 VV	
Voltage on any ball wrt. V_{SS}	–0.5 V to $V_{CCP} + 0.5$ V	

WARNING: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

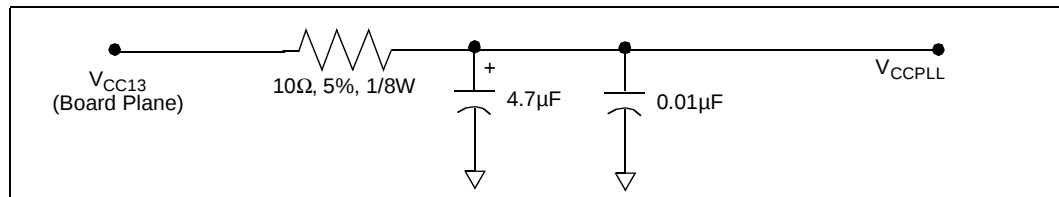
Table 14. Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{CC33}	3.3 V PCI supply voltage	3.0	3.6	V	
V_{CC25}	2.5 V DDR supply voltage	2.3	2.7	V	
V_{CC13}	1.3 V CORE supply voltage	1.235	1.365	V	
V_{CCPLL1}	PLL supply voltage	V_{CC13}	V_{CC13}	V	
V_{CCPLL2}	PLL supply voltage	V_{CC13}	V_{CC13}	V	
V_{REF}	Memory I/O reference voltage	$V_{CC25}/2 - 0.05$	$V_{CC25}/2 + 0.05$	V	
F_{P_CLK}	Input clock frequency	16	133	MHz	
T_C	Case temperature under bias	0	95	°C	

4.2 V_{CCPLL} Pin Requirements

To reduce clock skew, the V_{CCPLL1} , V_{CCPLL2} , V_{SSPLL1} and V_{SSPLL2} balls for the Phase Lock Loop (PLL) circuit are isolated on the package. The lowpass filter, as shown in Figure 7, reduces noise induced clock jitter and its effects on timing relationships in system designs. The 4.7 μ F capacitor must be (low ESR solid tantalum), the 0.01 μ F capacitor must be of the type X7R and the node connecting V_{CCPLL} must be as short as possible. The V_{SSPLL} balls should be connected to the board ground plane.

Figure 7. V_{CCPLL} Lowpass Filter



4.3 Targeted DC Specifications

Table 15. DC Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{IL1}	Input Low Voltage (SDRAM)	-0.3	$V_{REF} - 0.15$	V	3, 5
V_{IH1}	Input High Voltage (SDRAM)	$V_{REF} + 0.15$	$V_{CC25} + 0.3$	V	3, 5
V_{IL2}	Input Low Voltage (Misc.)	-0.3	0.8	V	4
V_{IH2}	Input High Voltage (Misc.)	2.0	$V_{CC33} + 0.3$	V	4
V_{IL3}	Input Low Voltage (PCI-X)	-0.5	$0.35 V_{CC33}$	V	1
V_{IH3}	Input High Voltage (PCI-X/PCI)	$0.5 V_{CC33}$	$V_{CC33} + 0.5$	V	1
V_{IL4}	Input Low Voltage (PCI)	-0.5	$0.3 V_{CC33}$	V	1
V_{OL1}	Output Low Voltage (Misc.)		0.4	V	$I_{OL} = 6 \text{ mA}$ (4)
V_{OH1}	Output High Voltage (Misc.)	2.4		V	$I_{OH} = -2 \text{ mA}$ (4)
V_{OL2}	Output Low Voltage (SDRAM)		0.35	V	$I_{OL} = 15.2 \text{ mA}$ (3, 5)
V_{OH2}	Output High Voltage (SDRAM)	1.95		V	$I_{OH} = -15.2 \text{ mA}$ (3, 5)
V_{OL3}	Output Low Voltage (PCI-X)		$0.1 V_{CC33}$	V	$I_{OL} = 1500 \mu\text{A}$ (1)
V_{OH3}	Output HIGH Voltage (PCI-X)	$0.9 V_{CC33}$		V	$I_{OH} = -500 \mu\text{A}$ (1)
C_{IN}	Input pin Capacitance		8	pF	1, 2
C_{CLK}	Clock pin Capacitance	5	8	pF	1, 2
L_{PIN}	Ball Inductance		15	nH	1, 2

NOTES:

1. As required by the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a.
2. Not tested.
3. SDRAM signals include **MA[12:0]**, **BA[1:0]**, **CAS#**, **CS[1:0]#**, **CKE[1:0]**, **DM[8:0]**, **RAS#**, **WE#**, **RCVENI#**, **RCVENO#**, **M_CK[2:0]**, **M_CK[2:0]#**, **DQ[63:0]**, **DQS[8:0]** and **CB[7:0]**.
4. Miscellaneous signals include all signals that are not PCI or SDRAM signals.
5. Only 2.5 V DDR SDRAM is supported.

Table 16. **I_{CC} Characteristics**

Symbol	Parameter	Typ	Max	Units	Notes
I _{LI1}	Input Leakage Current for each signal except TCK , TMS , TRST# , TDI .		±2	μA	0 < V _{IN} < V _{CC} (1)
I _{LI2}	Input Leakage Current for TCK , TMS , TRST# , TDI .	-140	-250	μA	V _{IN} = 0.45 V (1)
I _{CC13} Active (Thermal)	Core and Analog Current – 600 MHz.	1.2		A	(2)
I _{CC13} Active (Thermal)	Core and Analog Current – 400 MHz.	1.08		A	(2)
I _{CC25} Active (Thermal)	DDR Current – 200 MHz at 2.5 V.	0.38		A	(2)
I _{CC33} Active (Thermal)	PCI/PBI Current – 100 MHz/133 MHz at 3.3 V.	0.34		A	(2)
I _{CC13} Active (Power Supply)	Core and Analog Current – 600 MHz		1.72	A	(3)
I _{CC13} Active (Power Supply)	Core and Analog Current – 400 MHz		1.55	A	(3)
I _{CC25} Active (Power Supply)	DDR Current – 200 MHz at 2.5 V		0.42	A	(3)
I _{CC33} Active (Power Supply)	PCI/PBI Current – 100 MHz/133 MHz at 3.3 V		0.36	A	(3)

NOTES:

1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs with tri-state outputs..
2. I_{CC} Active (Thermal) value is provided for system thermal management. Typical I_{CC} is measured with V_{CC13} = 1.3 V, V_{CC25} = 2.5 V, V_{CC33} = 3.3 V and ambient temperature = 55°C.
3. I_{CC} Active (Power Supply) value is provided for selecting system power supply. It is measured using one of the worst case instruction mixes with V_{CC13} = 1.365 V, V_{CC25} = 2.75 V, V_{CC33} = 3.63 V and ambient temperature = 55°C.

4.4 Targeted AC Specifications

4.4.1 Clock Signal Timings

Table 17. Clock Timings

Symbol	Parameter	PCI-X 133		PCI-X 100		PCI-X 66		PCI 66		PCI 33		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
T _{F1}	PCI clock Frequency	100	133	66	100	50	66	33	66	16	33	MHz	1
T _{C1}	PCI clock Cycle Time	7.5	10	10	15	15	20	15	30	30	60	ns	1, 3
T _{CH1}	PCI clock High Time	3		3		6		6		11		ns	
T _{CL1}	PCI clock Low Time	3		3		6		6		11		ns	
T _{SR1}	PCI clock Slew Rate	1.5	4	1.5	4	1.5	4	1.5	4	1	4	V/ns	2
Spread Spectrum Requirements													
f _{mod}	PCI clock modulation frequency	30	33	30	33	30	33	30	33			KHz	
f _{spread}	PCI clock frequency spread	-1	0	-1	0	-1	0	-1	0			%	
Symbol	Parameter							PC200				Units	Notes
								Min		Max			
T _{F2}	DDR SDRAM clock Frequency									100		MHz	
T _{C2}	DDR SDRAM clock Cycle Time							10				ns	
T _{CH2}	DDR SDRAM clock High Time							4.5		5.5		ns	
T _{CL2}	DDR SDRAM clock Low Time							4.5		5.5		ns	
T _{CS2}	DDR SDRAM clock Period Stability									± 90		ps	
T _{skew2}	DDR SDRAM clock skew for M_CK[2:0] and M_CK[2:0]#									200		ps	
Symbol	Parameter					PBI 100		PBI 66		PBI 33		Units	Notes
						Min	Max	Min	Max	Min	Max		
T _{F3}	PBI clock Frequency						100		66		33	MHz	
T _{C3}	PBI clock Cycle Time					10		15		30		ns	
T _{CH3}	PBI clock High Time					3		6		11		ns	
T _{CL3}	PBI clock Low Time					3		6		11		ns	
T _{CS3}	PBI clock Period Stability						± 90		± 90		± 90	ps	

NOTES:

1. The clock frequency may not change beyond the spread-spectrum limits except while **P_RST#** is asserted.
2. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.
3. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

4.4.2 PCI Interface Signal Timings

Table 18. PCI Signal Timings

Symbol	Parameter	PCI-X 133 PCI-X 100		PCI-X 66		PCI 66		PCI 33		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
T _{OV1}	Clock to Output Valid Delay for bused signals	0.7	3.8	0.7	3.8	1	6	2	11	ns	1, 2, 3
T _{OV2}	Clock to Output Valid Delay for point to point signals	0.7	3.8	0.7	3.8	2	6	2	12	ns	1, 2, 3
T _{OF}	Clock to Output Float Delay		7		7		14		28	ns	1, 7
T _{IS1}	Input Setup to clock for bused signals	1.2		1.7		3		7		ns	3, 4, 8
T _{IS2}	Input Setup to clock for point to point signals	1.2		1.7		5		10, 12		ns	3, 4
T _{IH1}	Input Hold time from clock	0.5		0.5		0		0		ns	4
T _{RST}	Reset Active Time	1		1		1		1		ms	
T _{RF}	Reset Active to output float delay		40		40		40		40	ns	5, 6
T _{IS3}	REQ64# to Reset setup time	10		10		10		10		clocks	
T _{IH2}	Reset to REQ64# hold time	0	50	0	50	0	50	0	50	ns	
T _{IS4}	PCI-X initialization pattern to Reset setup time	10		10						clocks	
T _{IH3}	Reset to PCI-X initialization pattern hold time	0	50	0	50					ns	

NOTES:

- See the timing measurement conditions in Figure 9 "Output Timing Measurement Waveforms" on page 49.
- See Figure 15 "PCI/PCI-X TOV(max) Rising Edge AC Test Load" on page 53, Figure 16 "PCI/PCI-X TOV(max) Falling Edge AC Test Load" on page 53 and Figure 17 "PCI/PCI-X TOV(min) AC Test Load" on page 54.
- Setup time for point-to-point signals applies to REQ# and GNT# only. All other signals are bused.
- See the timing measurement conditions in Figure 10 "Input Timing Measurement Waveforms" on page 50.
- RST# is asserted and deasserted asynchronously with respect to CLK.
- All output drivers must be floated when RST# is active.
- For purposes of Active/Float timing measurements, the HI-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

4.4.3 DDR SDRAM Interface Signal Timings

Table 19. DDR SDRAM Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T _{VB1}	DQ, CB and DM output valid time before associated DQS	1.3		ns	4
T _{VA1}	DQ, CB and DM output valid time after associated DQS	1.3		ns	4
T _{VB2}	DQS output valid time before M _{_CK}		1.4	ns	4
T _{VA2}	DQS output valid time after M _{_CK}		1.0	ns	4
T _{VB3}	Address and Control write output valid before M _{_CK}	4.2		ns	4
T _{VA3}	Address and Control write output valid after M _{_CK}	3.3		ns	4
T _{VB4}	DQS read input valid time before DQ		1.6	ns	5
T _{VA4}	DQS read input valid time after DQ		1.6	ns	5
T _{VB5}	RCVENO# output valid time before M _{_CK}		1.4	ns	5
T _{VA5}	RCVENO# output valid time after M _{_CK}		1.0	ns	5
T _{VB6}	RCVENI# input valid time before DQS	3.0		ns	5
T _{VA6}	RCVENI# hold from DQS valid	0.8		ns	5

NOTES:

1. See Figure 9 "Output Timing Measurement Waveforms" on page 49.
2. See Figure 10 "Input Timing Measurement Waveforms" on page 50.
3. These output valid times are specified with a 0 pF loading.
4. See Figure 12 "DDR SDRAM Write Timings" on page 51.
5. See Figure 13 "DDR SDRAM Read Timings" on page 52.

4.4.4 Peripheral Bus Interface Signal Timings

Table 20. Peripheral Bus Signal Timings

Sym	Parameter	Min	Max	Units	Notes
T _{OV1}	Output Valid Delay from PB_CLK	1	5.5	ns	1, 3
T _{OF}	Output Float Delay from PB_CLK	1	5.5	ns	1, 3
T _{IS1}	Input Setup to PB_CLK	4.9		ns	2
T _{IH1}	Input Hold from PB_CLK	2		ns	2

NOTES:

1. See Figure 9 "Output Timing Measurement Waveforms" on page 49.
2. See Figure 10 "Input Timing Measurement Waveforms" on page 50.
3. See Figure 14 "AC Test Load for all Signals Except PCI and DDR SDRAM" on page 53.

4.4.5 I²C Interface Signal Timings

Table 21. I²C Signal Timings

Symbol	Parameter	Std. Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F _{SCL}	SCL Clock Frequency	0	100	0	400	KHz	
T _{BUF}	Bus Free Time Between STOP and START Condition	4.7		1.3		μs	1
T _{HDSTA}	Hold Time (repeated) START Condition	4		0.6		μs	1, 3
T _{LOW}	SCL Clock Low Time	4.7		1.3		μs	1, 2
T _{HIGH}	SCL Clock High Time	4		0.6		μs	1, 2
T _{SUSTA}	Setup Time for a Repeated START Condition	4.7		0.6		μs	1
T _{HDDAT}	Data Hold Time	0	3.45	0	0.9	μs	1
T _{SUDAT}	Data Setup Time	250		100		ns	1
T _{SR}	SCL and SDA Rise Time		1000	20+0.1C _b	300	ns	1, 4
T _{SF}	SCL and SDA Fall Time		300	20+0.1C _b	300	ns	1, 4
T _{SUSTO}	Setup Time for STOP Condition	4		0.6		μs	1

NOTES:

1. See Figure 11 "I²C Interface Signal Timings" on page 50.
2. Not tested.
3. After this period, the first clock pulse is generated.
4. C_b = the total capacitance of one bus line, in pF.

4.4.6 SSP Interface Signal Timings

Table 22. SSP Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T _{IS}	Input Setup to SSCKO	9		ns	
T _{IH}	Input Hold from SSCKO	0		ns	
T _{OV}	Output Valid Delay from SSCKO	-1	2	ns	
T _{OV}	Output Valid Delay from SSCKI to SSCKO in external clock mode.	3	10	ns	

4.4.7 Boundary Scan Test Signal Timings

Table 23. Boundary Scan Test Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T _{BSF}	TCK Frequency	0	66	MHz	
T _{BSCH}	TCK High Time	7.5		ns	Measured at 1.5 V (1)
T _{BSCL}	TCK Low Time	7.5		ns	Measured at 1.5 V (1)
T _{BSCR}	TCK Rise Time		5	ns	0.8 V to 2.0 V (1)
T _{BSCF}	TCK Fall Time		5	ns	2.0 V to 0.8 V (1)
T _{BSIS1}	Input Setup to TCK	3		ns	4
T _{BSIH1}	Input Hold from TCK	3		ns	4
T _{BSOV1}	TDO Output Valid Delay from falling edge of TCK.	1	11	ns	2, 3
T _{OF1}	TDO Output Float Delay from falling edge of TCK.	1	11	ns	2, 5

NOTES:

1. Not tested.
2. Outputs precharged to V_{CC5}.
3. See [Figure 9 "Output Timing Measurement Waveforms" on page 49](#).
4. See [Figure 10 "Input Timing Measurement Waveforms" on page 50](#).
5. A float condition occurs when the output current becomes less than ILO. Float delay is not tested. See [Figure 9 "Output Timing Measurement Waveforms" on page 49](#).

4.5 AC Timing Waveforms

Figure 8. Clock Timing Measurement Waveforms

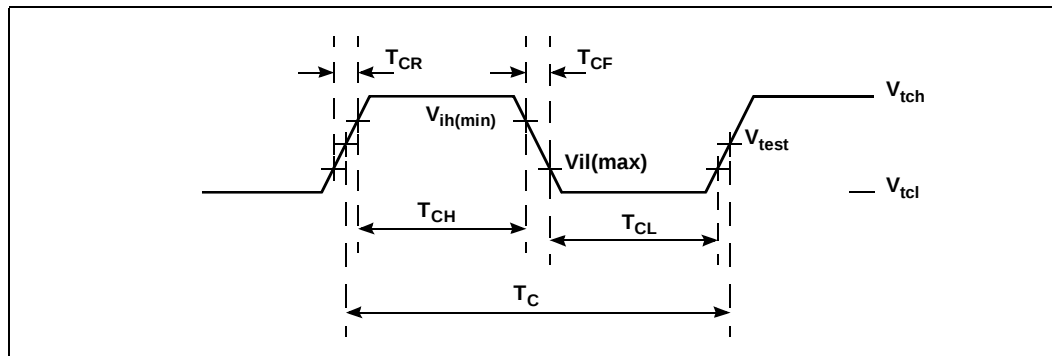


Figure 9. Output Timing Measurement Waveforms

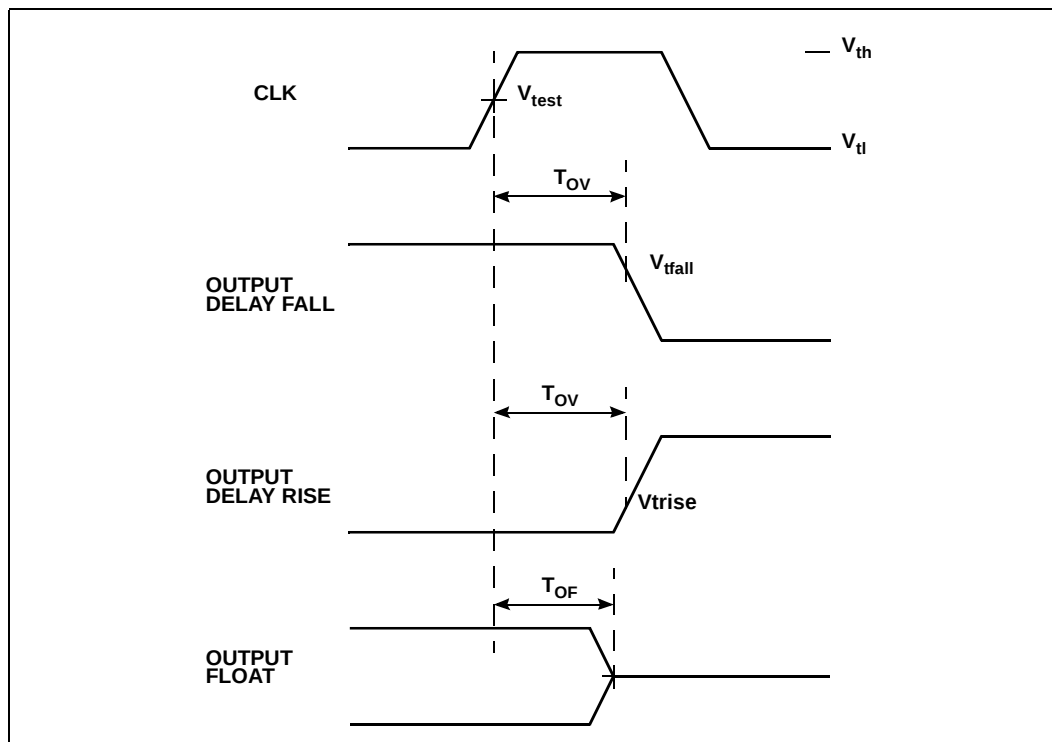


Figure 10. Input Timing Measurement Waveforms

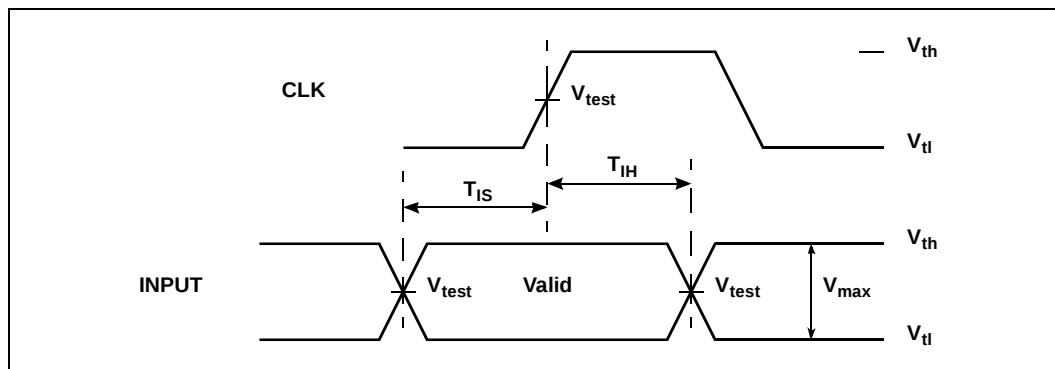


Figure 11. I²C Interface Signal Timings

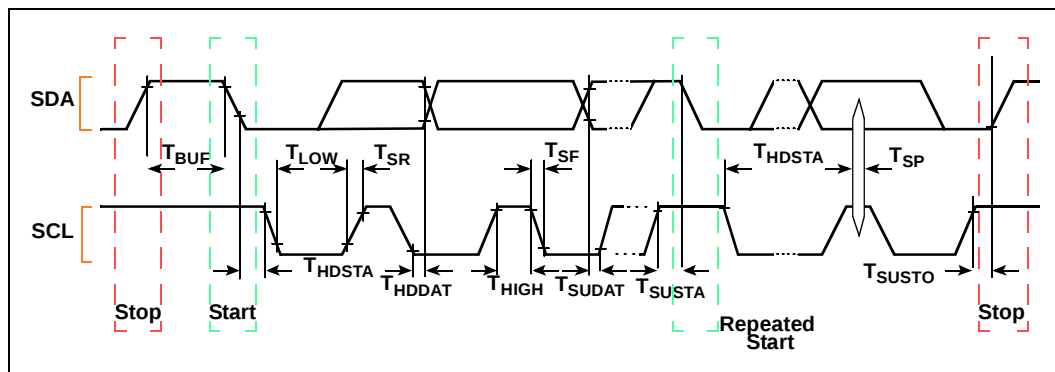


Figure 12. DDR SDRAM Write Timings

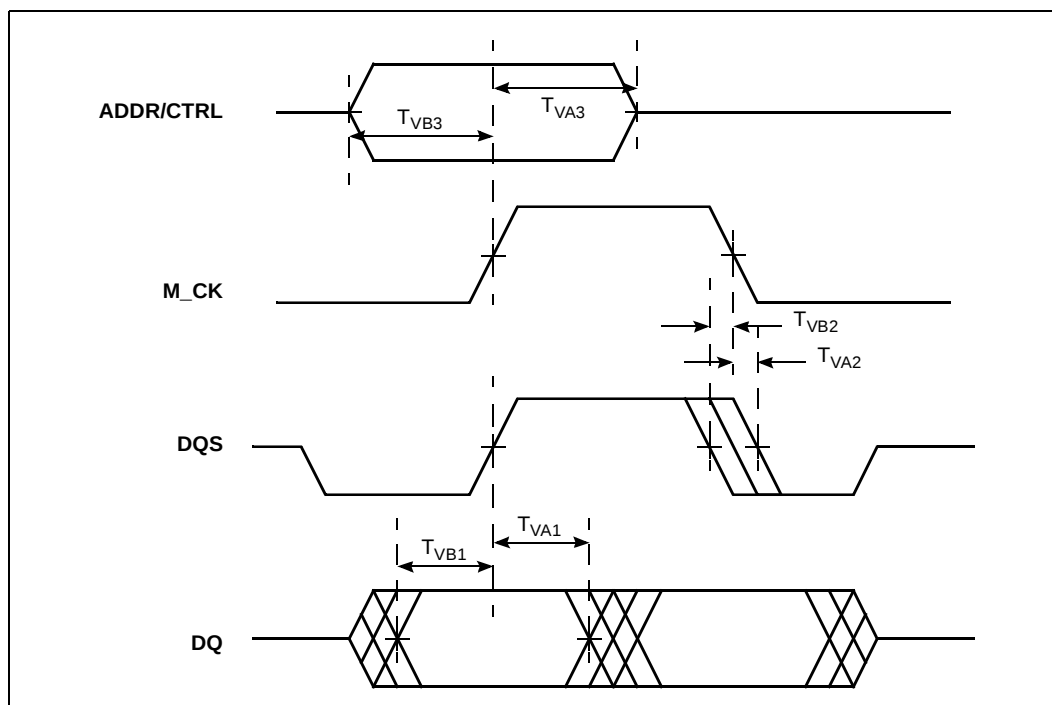
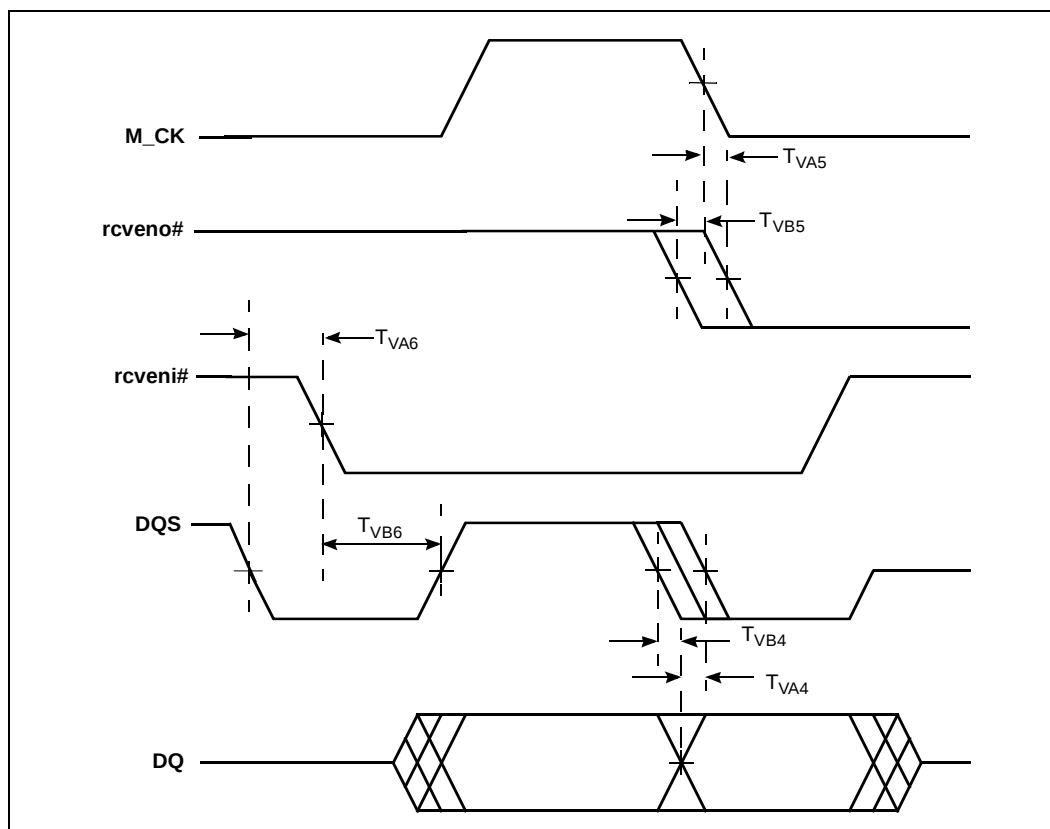


Figure 13. DDR SDRAM Read Timings



4.6 AC Test Conditions

Table 26. AC Measurement Conditions

Symbol	PCI-X	PCI	DDR	PBI	Units	Notes
V_{tch}	$0.6 V_{CC33}$	$0.6 V_{CC33}$	-	-	V	
V_{tcl}	$0.2 V_{CC33}$	$0.2 V_{CC33}$	-	-	V	
V_{th}	$0.6 V_{CC33}$	$0.6 V_{CC33}$	2.0	2.0	V	
V_{tl}	$0.25 V_{CC33}$	$0.2 V_{CC33}$	0.5	0.8	V	
V_{test}	$0.4 V_{CC33}$	$0.4 V_{CC33}$	1.25	1.5	V	
V_{trise}	$0.285 V_{CC33}$	$0.285 V_{CC33}$	1.25	1.5	V	
V_{tfall}	$0.615 V_{CC33}$	$0.615 V_{CC33}$	1.25	1.5	V	
V_{max}	$0.4 V_{CC33}$	$0.4 V_{CC33}$	1.5	1.2	V	
Slew Rate	1.5	1.5	1.5	1.5	V/nS	1

1. Input signal slew rate is measured between V_{il} and V_{ih} .

Figure 14. AC Test Load for all Signals Except PCI and DDR SDRAM

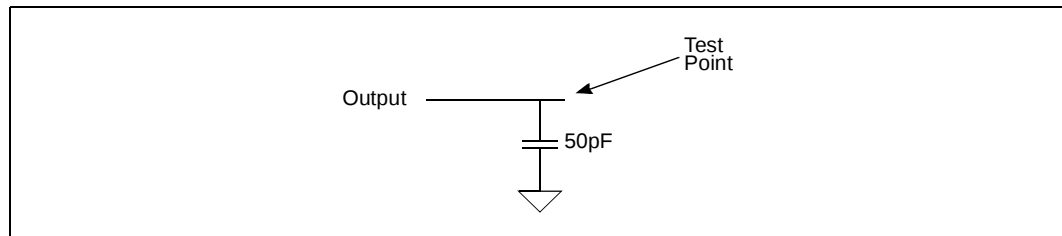


Figure 15. PCI/PCI-X $T_{OV(max)}$ Rising Edge AC Test Load

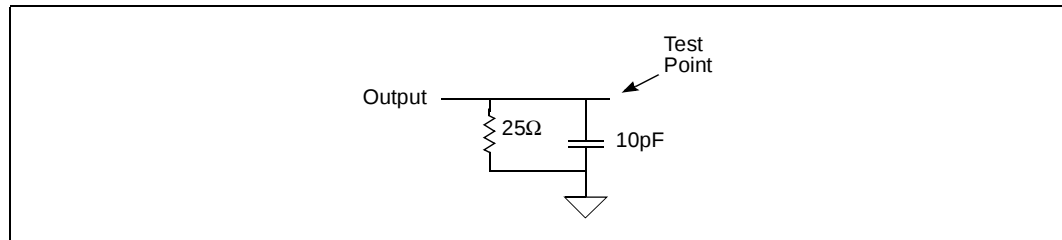


Figure 16. PCI/PCI-X $T_{OV(max)}$ Falling Edge AC Test Load

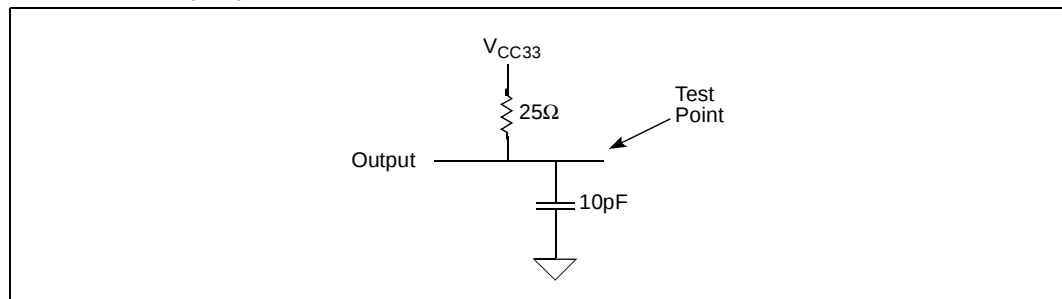


Figure 17. PCI/PCI-X $T_{OV(min)}$ AC Test Load

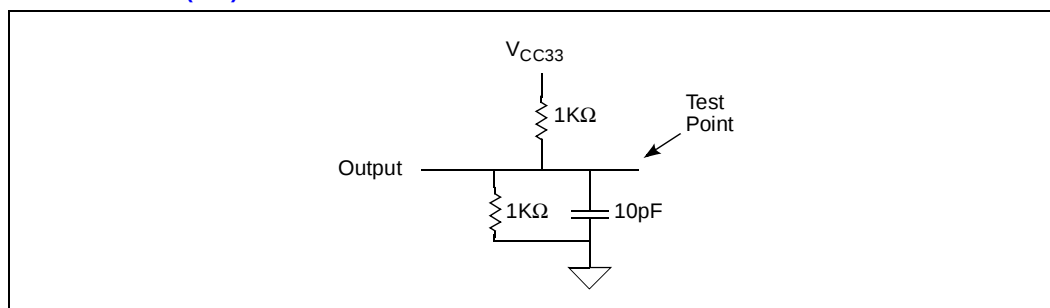


Figure 18. PCI_RST# vs. PWRDELAY Timings During Power-Up

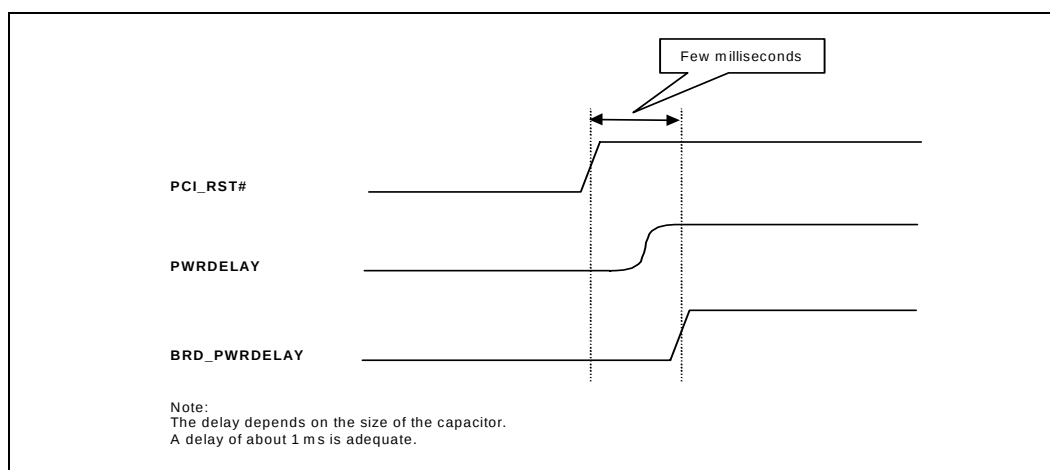


Figure 19. PCI_RST# vs. PWRDELAY Timings During Power-Down

