DATA SHEET

BF1100WR
Dual-gate MOS-FET

Product specification

1995 Apr 25

Dual-gate MOS-FET BF1100WR

FEATURES

- Specially designed for use at 9 to 12 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications such as television tuners and professional communications equipment.

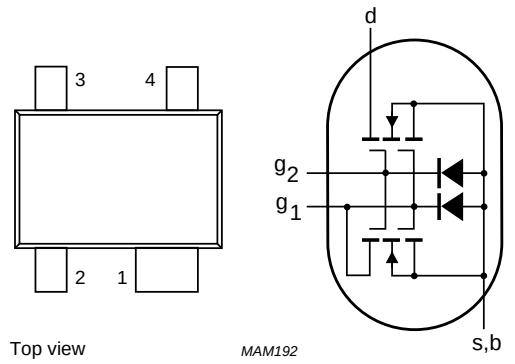
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT343R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MF.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	14	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	280	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		24	28	33	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		–	2.2	2.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 800 MHz	–	2	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	14	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	see Fig.2; up to T_{amb} = 50 °C; note 1	–	280	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

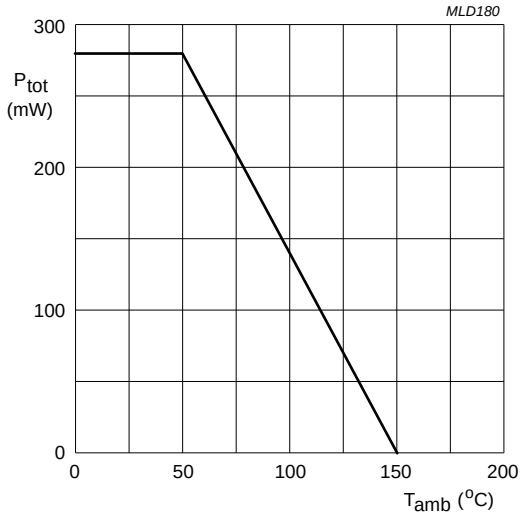


Fig.2 Power derating curve.

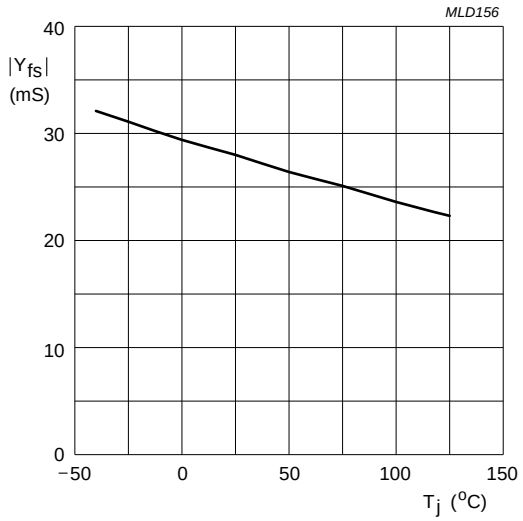


Fig.3 Forward transfer admittance as a function of junction temperature; typical values.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	T_s = 91 °C; note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}S}$ = 1 mA	13.2	20	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}S}$ = 1 mA	13.2	20	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 9 V; I_D = 20 μA	0.3	1	V
		$V_{G2\text{-}S}$ = 4 V; V_{DS} = 12 V; I_D = 20 μA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S}$ = 4 V; V_{DS} = 9 V; I_D = 20 μA	0.3	1.2	V
		$V_{G1\text{-}S}$ = 4 V; V_{DS} = 12 V; I_D = 20 μA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 9 V; R_{G1} = 180 kΩ; note 1	8	13	mA
		$V_{G2\text{-}S}$ = 4 V; V_{DS} = 12 V; R_{G1} = 250 kΩ; note 2	8	13	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S}$ = V_{DS} = 0; $V_{G1\text{-}S}$ = 12 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S}$ = V_{DS} = 0; $V_{G2\text{-}S}$ = 12 V	–	50	nA

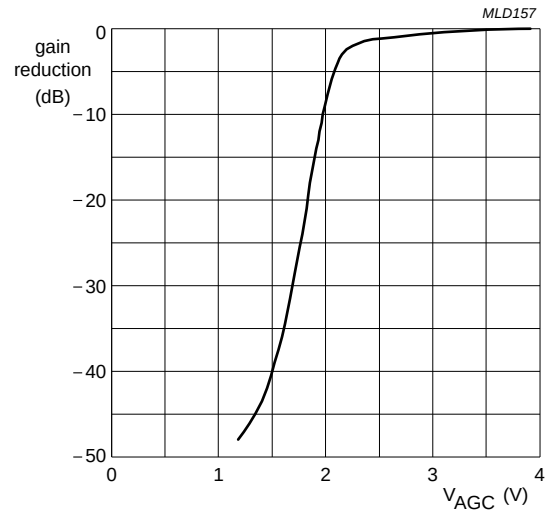
Notes

1. R_{G1} connects gate 1 to V_{GG} = 9 V; see Fig.26.
2. R_{G1} connects gate 1 to V_{GG} = 12 V; see Fig.26.

DYNAMIC CHARACTERISTICS

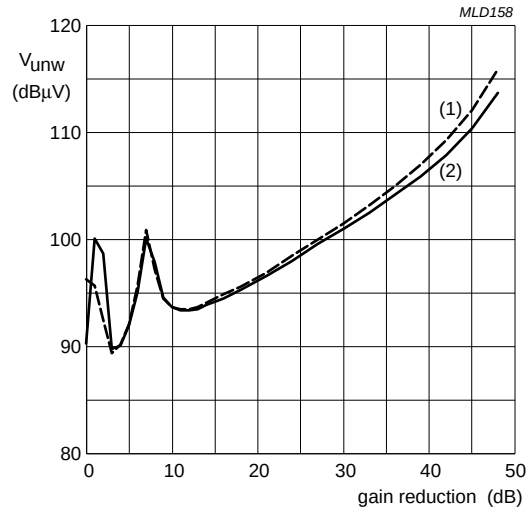
Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; I_D = 10 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C				
		V_{DS} = 9 V	24	28	33	mS
		V_{DS} = 12 V	24	28	33	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz				
		V_{DS} = 9 V	–	2.2	2.6	pF
		V_{DS} = 12 V	–	2.2	2.6	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz				
		V_{DS} = 9 V	–	1.6	–	pF
		V_{DS} = 12 V	–	1.4	–	pF
C_{os}	drain-source capacitance	f = 1 MHz				
		V_{DS} = 9 V	–	1.4	1.8	pF
		V_{DS} = 12 V	–	1.1	1.5	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz				
		V_{DS} = 9 V	–	25	35	fF
		V_{DS} = 12 V	–	25	35	fF
F	noise figure	f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$				
		V_{DS} = 9 V	–	2	2.8	dB
		V_{DS} = 12 V	–	2	2.8	dB



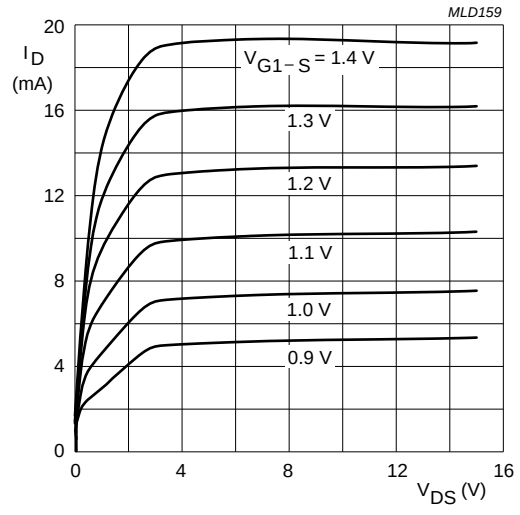
f = 50 MHz.
T_j = 25 °C.

Fig.4 Gain reduction as a function of the AGC voltage; typical values.



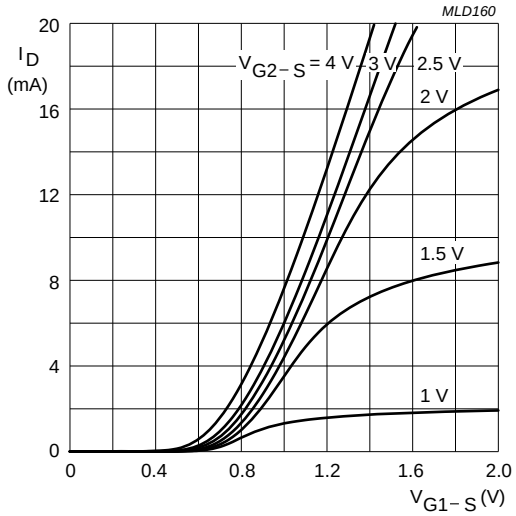
(1) R_G = 250 kΩ to V_{GG} = 12 V.
(2) R_G = 180 kΩ to V_{GG} = 9 V.
f_w = 50 MHz; f_{unw} = 60 MHz; T_{amb} = 25 °C.

Fig.5 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.26.



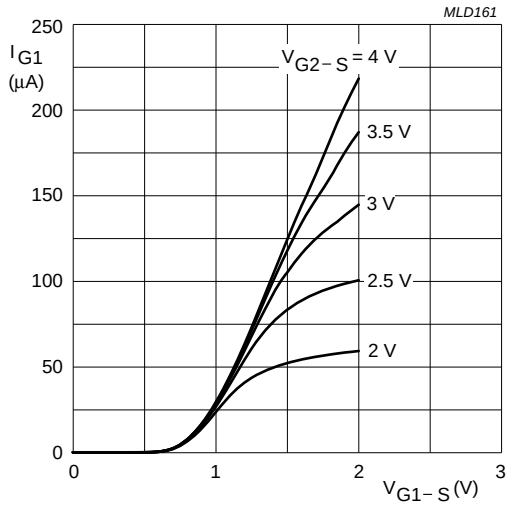
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



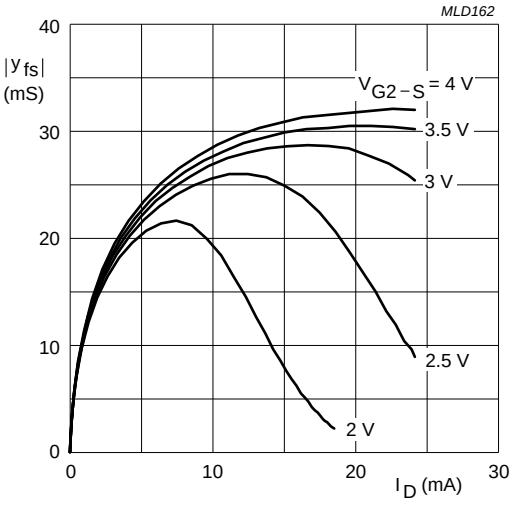
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.7 Transfer characteristics; typical values.



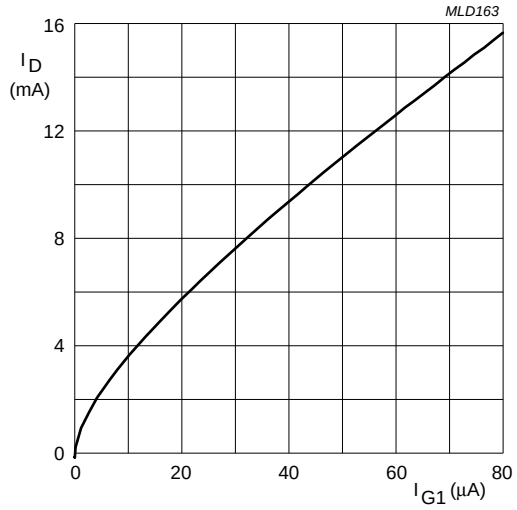
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.8 Gate 1 current as a function of gate 1 voltage; typical values.



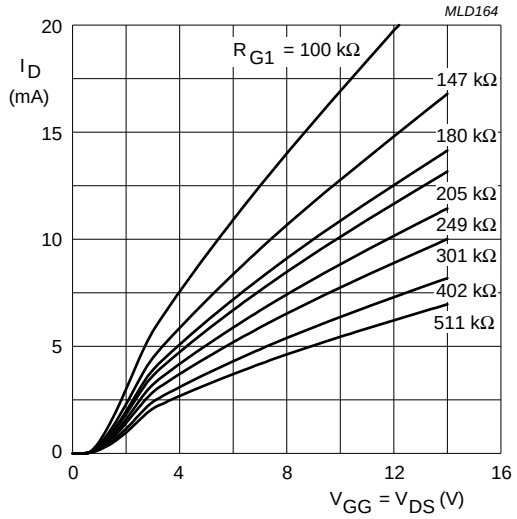
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.9 Forward transfer admittance as a function of drain current; typical values.



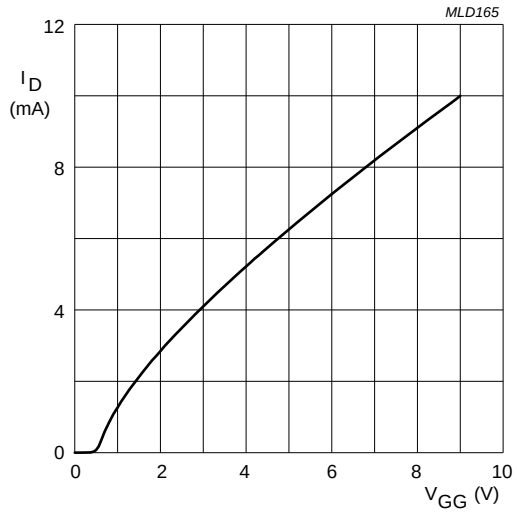
V_{DS} = 9 to 12 V.
$V_{G2\text{-}S}$ = 4 V.
T_j = 25 °C.

Fig.10 Drain current as a function of gate 1 current; typical values.



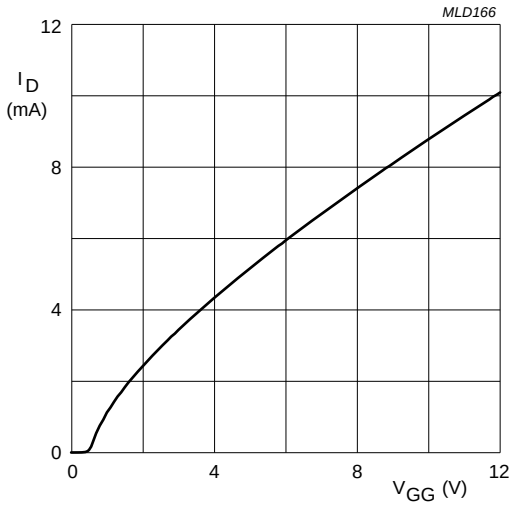
$V_{G2\text{-}S}$ = 4 V.
R_{G1} connected to V_{GG}.
T_j = 25 °C.

Fig.11 Drain current as a function of gate 1 supply voltage (= V_{GG}) and drain supply voltage; typical values; see Fig.26.



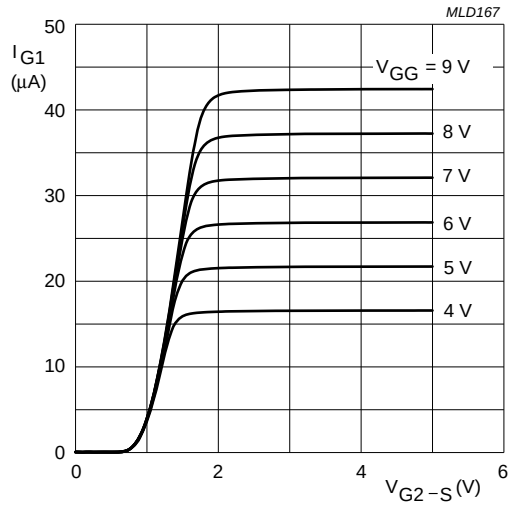
V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 180 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.12 Drain current as a function of gate 1 voltage (= V_{GG}); typical values; see Fig.26.



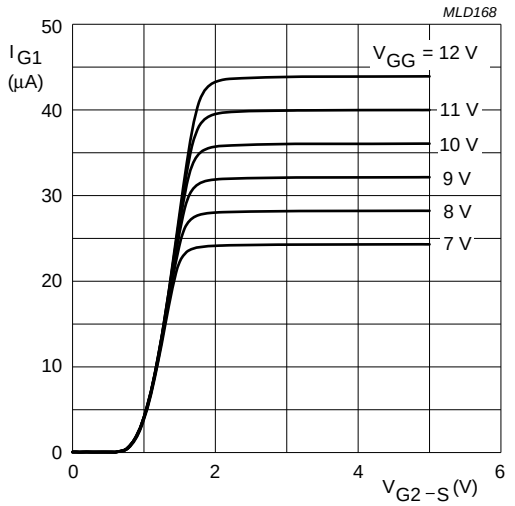
V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 250 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.13 Drain current as a function of gate 1 voltage (= V_{GG}); typical values; see Fig.26.



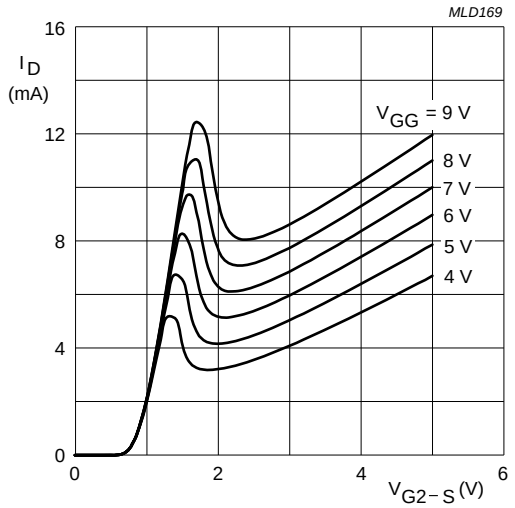
V_{DS} = 9 V.
R_{G1} = 180 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.14 Gate 1 current as a function of gate 2 voltage; typical values.



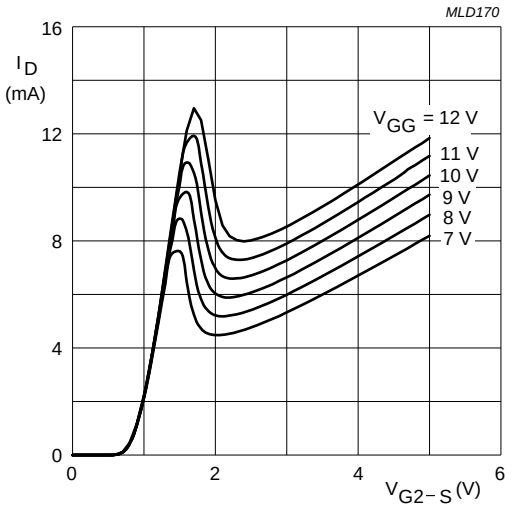
V_{DS} = 12 V.
R_{G1} = 250 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.15 Gate 1 current as a function of gate 2 voltage; typical values.



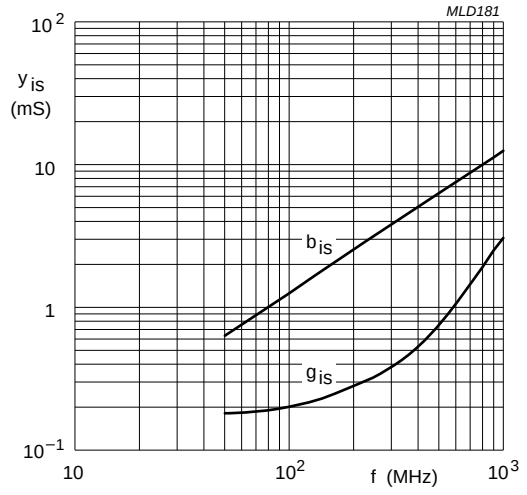
V_{DS} = 9 V.
R_{G1} = 180 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.16 Drain current as a function of the gate 2 voltage; typical values; see Fig.26.



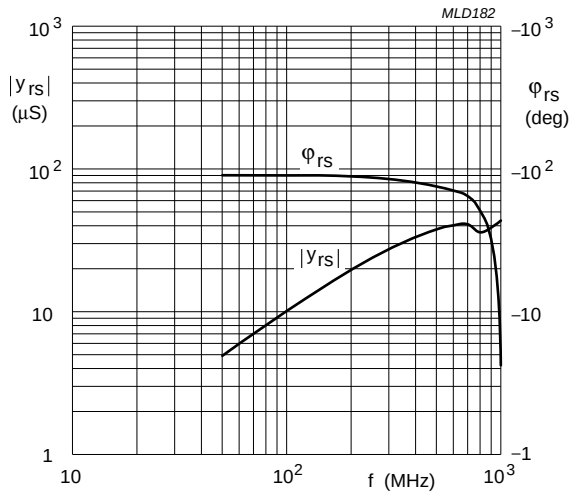
V_{DS} = 12 V.
R_{G1} = 250 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.17 Drain current as a function of the gate 2 voltage; typical values; see Fig.26.



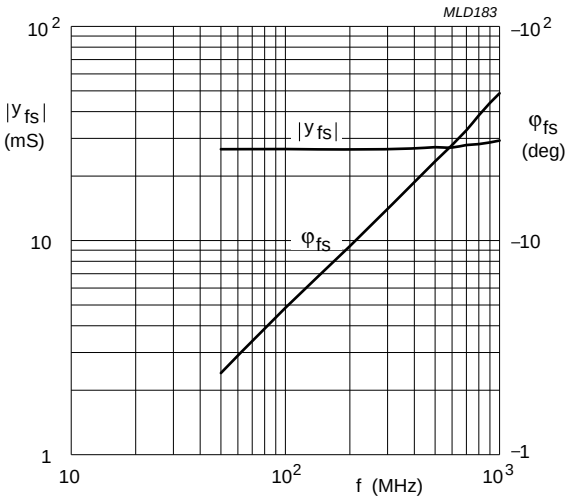
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.18 Input admittance as a function of frequency; typical values.



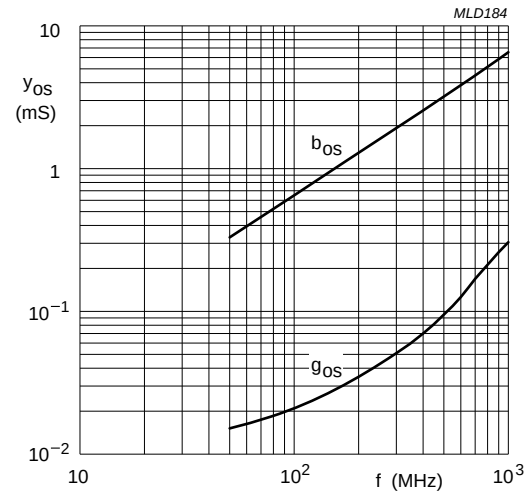
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.19 Reverse transfer admittance and phase as a function of frequency; typical values.



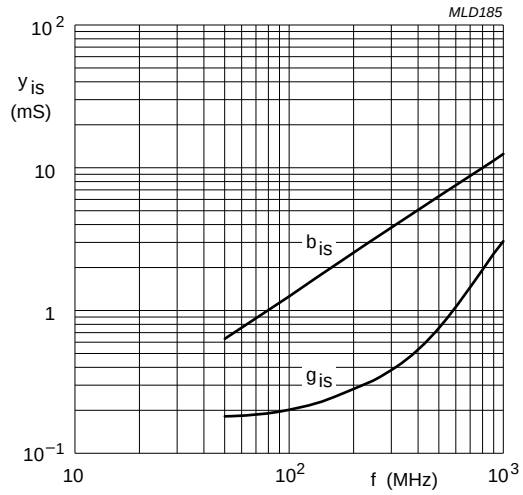
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Forward transfer admittance and phase as a function of frequency; typical values.



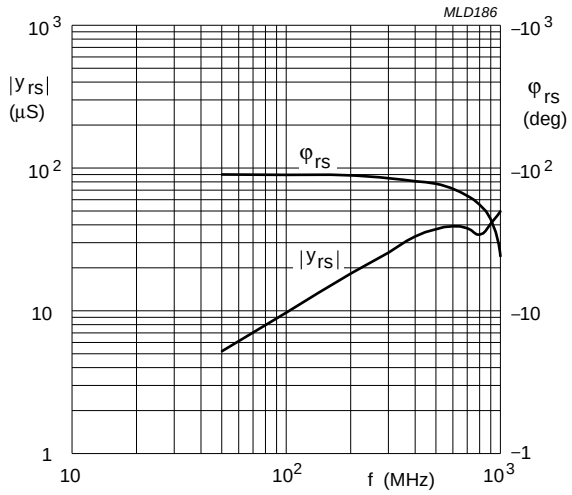
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Output admittance as a function of frequency; typical values.



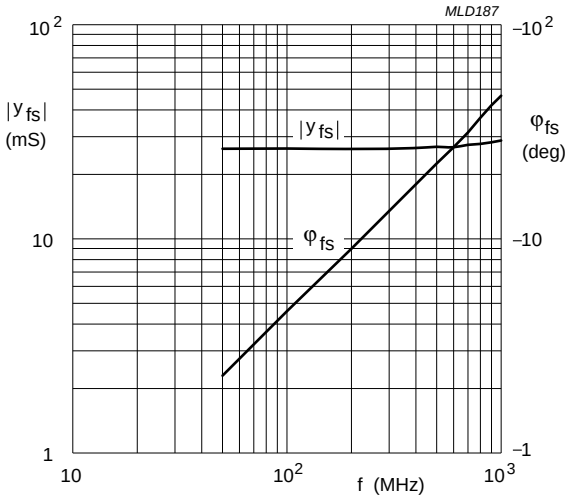
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.22 Input admittance as a function of frequency; typical values.



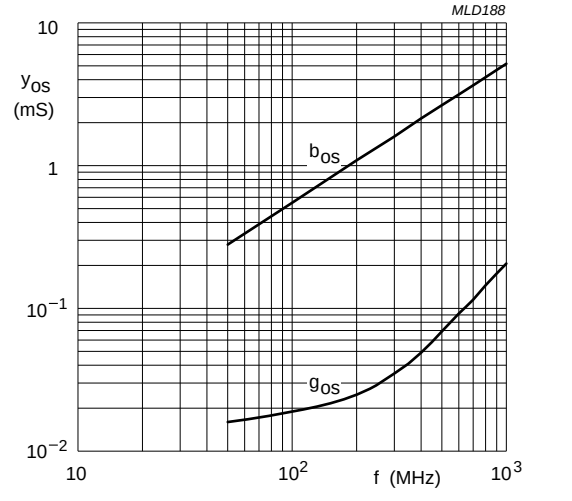
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.23 Reverse transfer admittance and phase as a function of frequency; typical values.



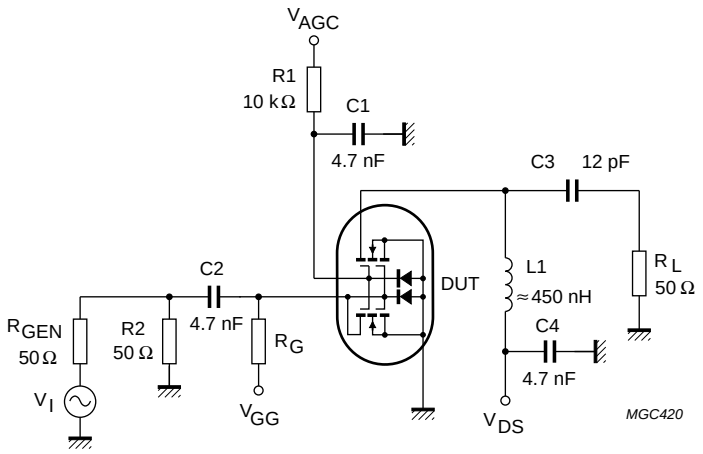
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.24 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.25 Output admittance as a function of frequency; typical values.



For $V_{GG} = V_{DS} = 9$ V, $R_G = 180$ kΩ.
For $V_{GG} = V_{DS} = 12$ V, $R_G = 250$ kΩ.

Fig.26 Cross-modulation test circuit.

Table 1 Scattering parameters: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	−3.9	2.618	175.1	0.001	137.9	1.000	−1.9
100	0.981	−7.3	2.602	170.5	0.001	80.4	0.999	−4.0
200	0.975	−14.4	2.577	160.7	0.002	74.0	0.995	−7.6
300	0.965	−21.6	2.555	151.6	0.002	79.3	0.994	−11.3
400	0.947	−28.3	2.513	141.8	0.003	80.5	0.992	−15.0
500	0.927	−34.9	2.449	133.4	0.003	82.8	0.988	−18.5
600	0.913	−41.7	2.339	124.6	0.003	78.9	0.984	−22.0
700	0.890	−47.9	2.361	115.4	0.003	80.6	0.982	−25.3
800	0.869	−54.0	2.302	106.4	0.003	93.9	0.979	−28.8
900	0.845	−59.7	2.228	97.6	0.003	104.8	0.976	−32.1
1000	0.823	−65.4	2.167	89.6	0.003	129.3	0.974	−35.5

Table 2 Noise data: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.67	43.9	0.89

Table 3 Scattering parameters: V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

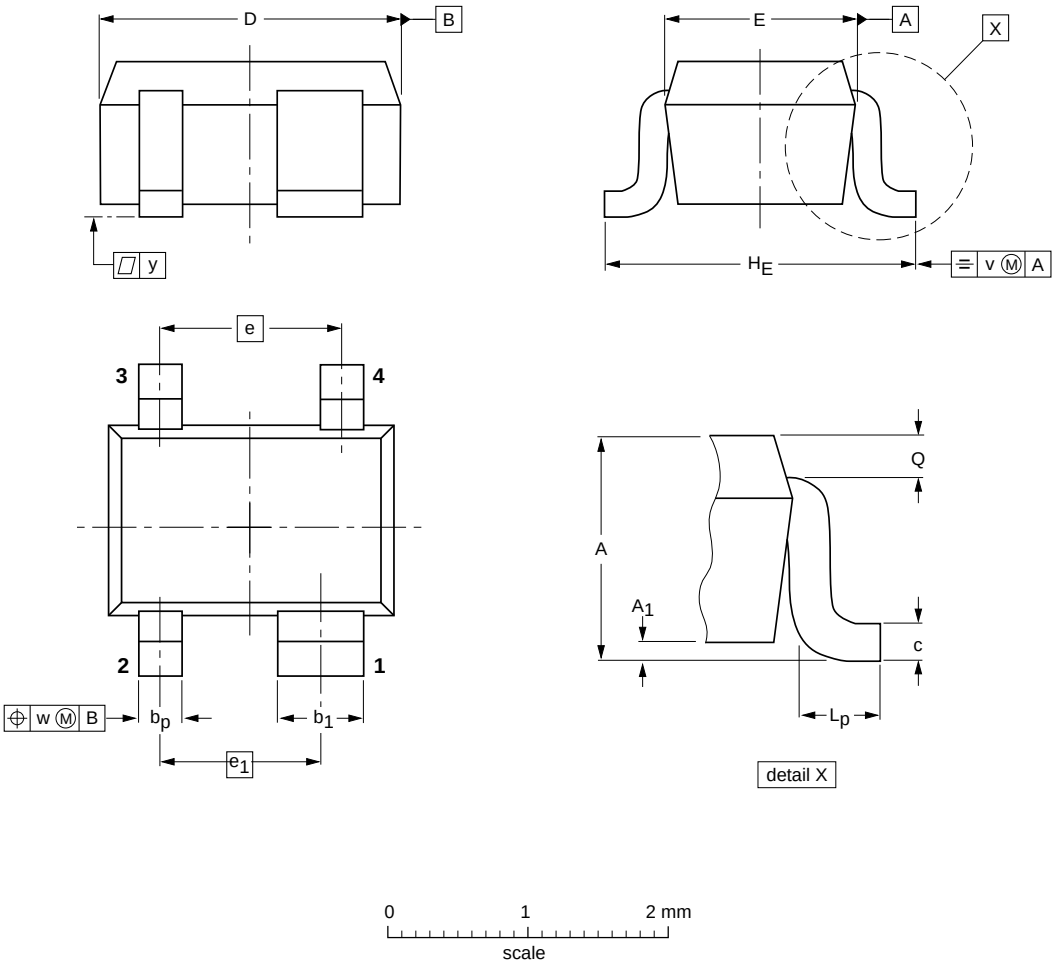
f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	−3.7	2.576	175.3	0.000	125.0	1.000	−1.6
100	0.980	−7.4	2.563	170.9	0.001	111.2	1.000	−3.3
200	0.973	−14.6	2.541	161.6	0.002	83.0	0.997	−6.4
300	0.962	−21.5	2.519	152.9	0.002	85.2	0.996	−9.3
400	0.946	−28.5	2.479	143.5	0.003	79.4	0.995	−12.4
500	0.929	−35.0	2.419	135.5	0.003	78.2	0.991	−15.3
600	0.912	−41.6	2.373	127.2	0.003	80.0	0.989	−18.1
700	0.895	−47.8	2.336	118.7	0.003	83.4	0.987	−20.9
800	0.868	−53.8	2.284	110.0	0.003	91.3	0.985	−23.7
900	0.845	−59.8	2.213	101.6	0.003	95.9	0.983	−26.5
1000	0.823	−65.7	2.160	94.1	0.003	112.2	0.981	−29.3

Table 4 Noise data: V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.66	43.3	0.97

PACKAGE OUTLINE

Plastic surface-mounted package; reverse pinning; 4 leads **SOT343R**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						~~97-05-21~~ 06-03-16

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

For additional information please visit: **http://www.nxp.com**
For sales offices addresses send e-mail to: **salesaddresses@nxp.com**

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