

HM621100A Series

1048576-word × 1-bit High Speed CMOS Static RAM

The Hitachi HM621100A is a high speed 1M Static RAM organized as 1048576-word × 1-bit. It realizes high speed access time (20/25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM621100A, packaged in a 400-mil plastic SOJ is available for high density mounting.

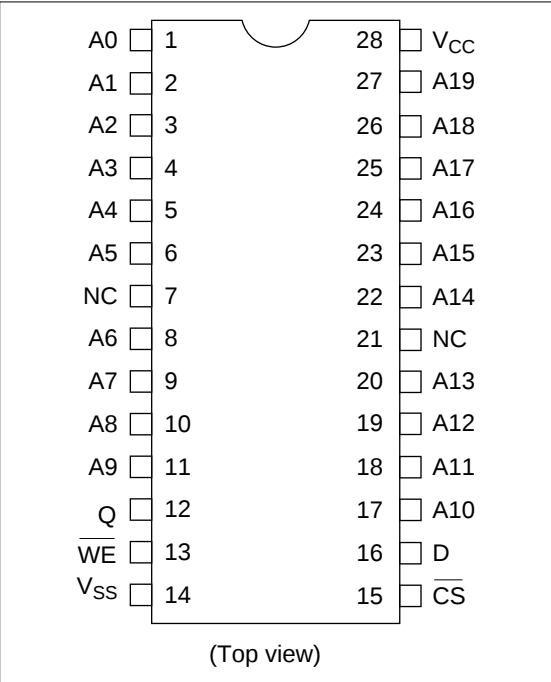
Features

- Single 5 V supply and high density 28-pin package (DIP and SOJ)
- High speed
Access time: 20/25/35 ns (max)
- Low power dissipation
Active mode: 350 mW (typ)
Standby mode: 100 μ W (typ)
- Completely static memory required
No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible
All inputs and outputs

Ordering Information

Type No.	Access time	Package
HM621100AP-20	20 ns	400-mil 28-pin plastic DIP (DP-28C)
HM621100AP-25	25 ns	
HM621100AP-35	35 ns	
HM621100ALP-20	20 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM621100ALP-25	25 ns	
HM621100ALP-35	35 ns	
HM621100AJP-20	20 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM621100AJP-25	25 ns	
HM621100AJP-35	35 ns	
HM621100ALJP-20	20 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM621100ALJP-25	25 ns	
HM621100ALJP-35	35 ns	

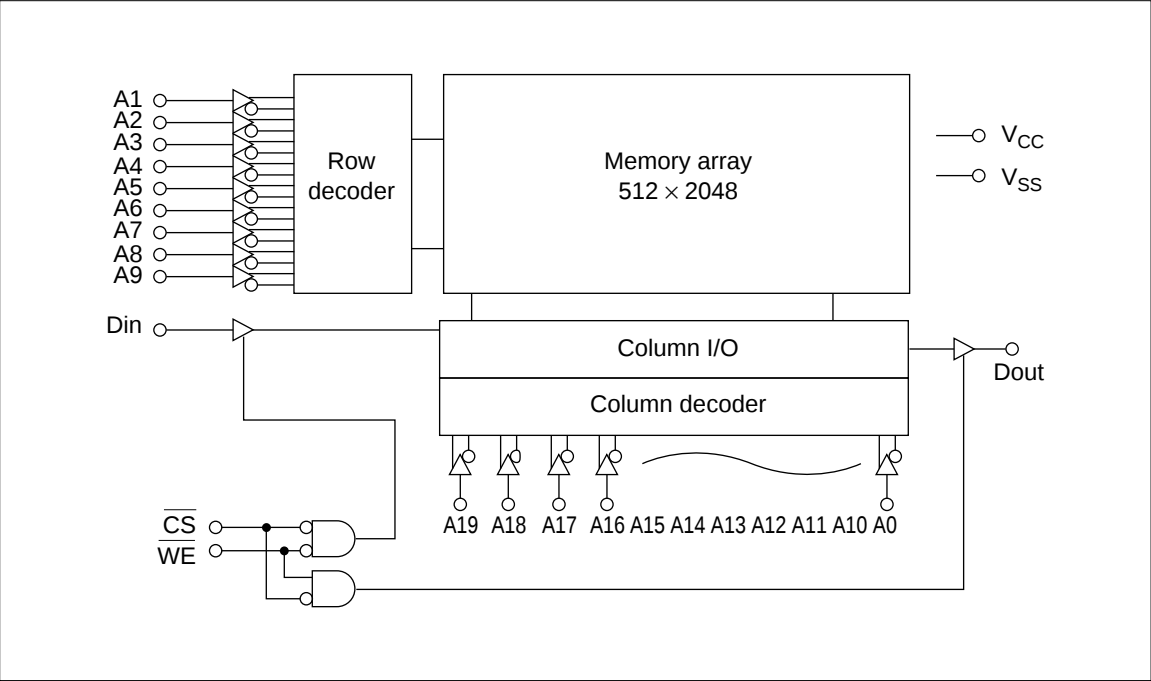
Pin Arrangement



Pin Description

Pin Name	Function
A0 – A19	Address
D	Input
Q	Output
CS	Chip select
WE	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{\text{CS}}$	$\overline{\text{WE}}$	Mode	V_{CC} current	Output pin	Ref. cycle
H	X	Not selected	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
L	H	Read	I_{CC}	Dout	Read cycle
L	L	Write	I_{CC}	High-Z	Write cycle

Note: X : H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{in}	-0.5^{*1} to +7.0	V
Power dissipation	P_{T}	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	-55 to +125	°C
Storage temperature range under bias	T_{bias}	-10 to +85	°C

Note: 1. $V_{\text{in min}} = -2.0$ V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions ($T_{\text{a}} = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	-0.5^{*1}	—	0.8	V

Note: 1. $V_{\text{IL min}} = -2.0$ V for pulse width ≤ 10 ns.

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	HM621100A-20			HM621100A-25/35			Unit	Test conditions
		Min	Typ ^{*1}	Max	Min	Typ ^{*1}	Max		
Input leakage current	$ I_{LI} $	—	—	2.0	—	—	2.0	μA	$V_{CC} = \max$ $V_{in} = V_{SS}$ to V_{CC}
Output leakage current	$ I_{LO} $	—	—	2.0	—	—	2.0	μA	$\overline{CS} = V_{IH}$ $V_{I/O} = V_{SS}$ to V_{CC}
Operating power supply current	I_{CC}	—	—	150	—	—	120	mA	$\overline{CS} = V_{IL}$, $I_{I/O} = 0\text{ mA}$, min cycle
Standby power supply current	I_{SB}	—	—	60	—	—	40	mA	$\overline{CS} = V_{IH}$, min cycle
Standby power supply current (1)	I_{SB1}^{*2}	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$ $0\text{ V} \leq V_{in} \leq 0.2\text{ V}$ or $V_{in} \geq V_{CC} - 0.2\text{ V}$
	I_{SB1}^{*3}	—	—	100	—	—	100	μA	
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	$I_{OL} = 8\text{ mA}$
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	$I_{OH} = -4\text{ mA}$

Notes: 1. Typical values are at $V_{CC} = 5.0\text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

2. P and JP version

3. LP and LJP version

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Min	Max	Unit	Test conditions
Input capacitance	C_{in}	—	5 ^{*2}	pF	$V_{in} = 0\text{ V}$
			6 ^{*3}		
Output capacitance	C_{out}	—	8	pF	$V_{out} = 0\text{ V}$

Note: 1. This parameter is sampled and not 100% tested.

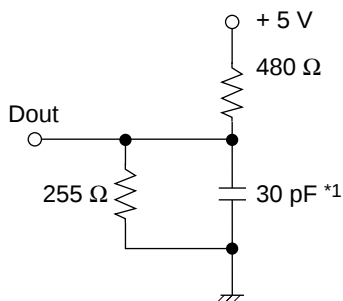
2. SOJ package

3. DIP package

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, unless otherwise noted.)

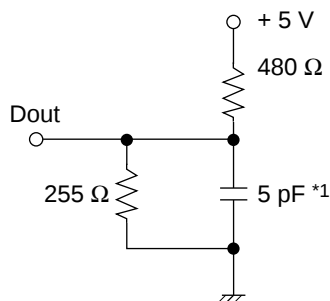
Test Conditions

- Input pulse levels: 0 V to 3.0 V
- Input rise and fall times: 4 ns
- Input timing reference levels: 1.5 V
- Output timing reference levels: 1.5 V
- Output load: See figures



Output load (A)

Note: 1. Including scope and jig



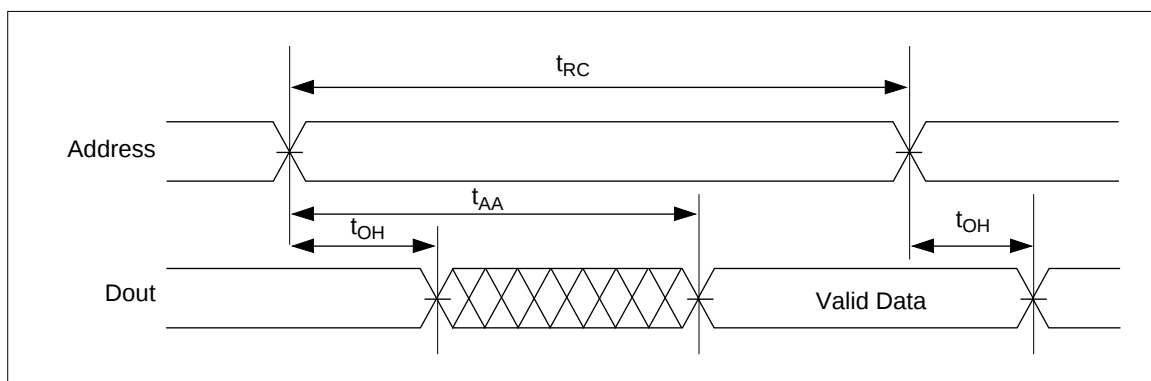
Output load (B)

(For t_{HZ} , t_{LZ} , t_{WZ} and t_{OW})

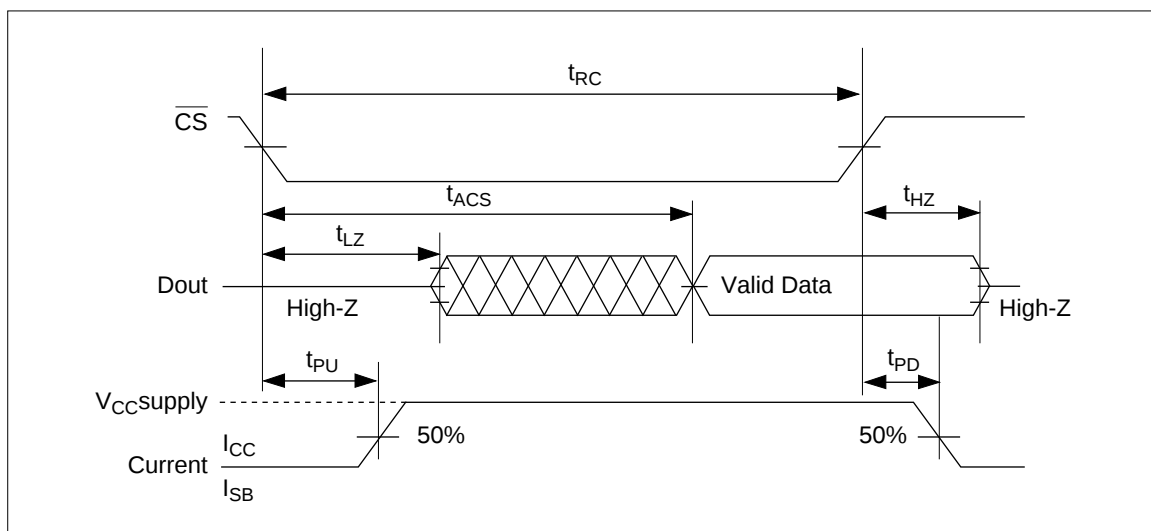
Read Cycle

Parameter	Symbol	HM621100A-20		HM621100A-25		HM621100A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	20	—	25	—	35	—	ns
Address access time	t_{AA}	—	20	—	25	—	35	ns
Chip select access time	t_{ACS}	—	20	—	25	—	35	ns
Chip selection to output in low-Z	t_{LZ}^{*1}	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}^{*1}	0	10	0	12	0	15	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	12	—	15	—	25	ns

Read Timing Waveform (1) *2, *3



Read Timing Waveform (2) *2, *4

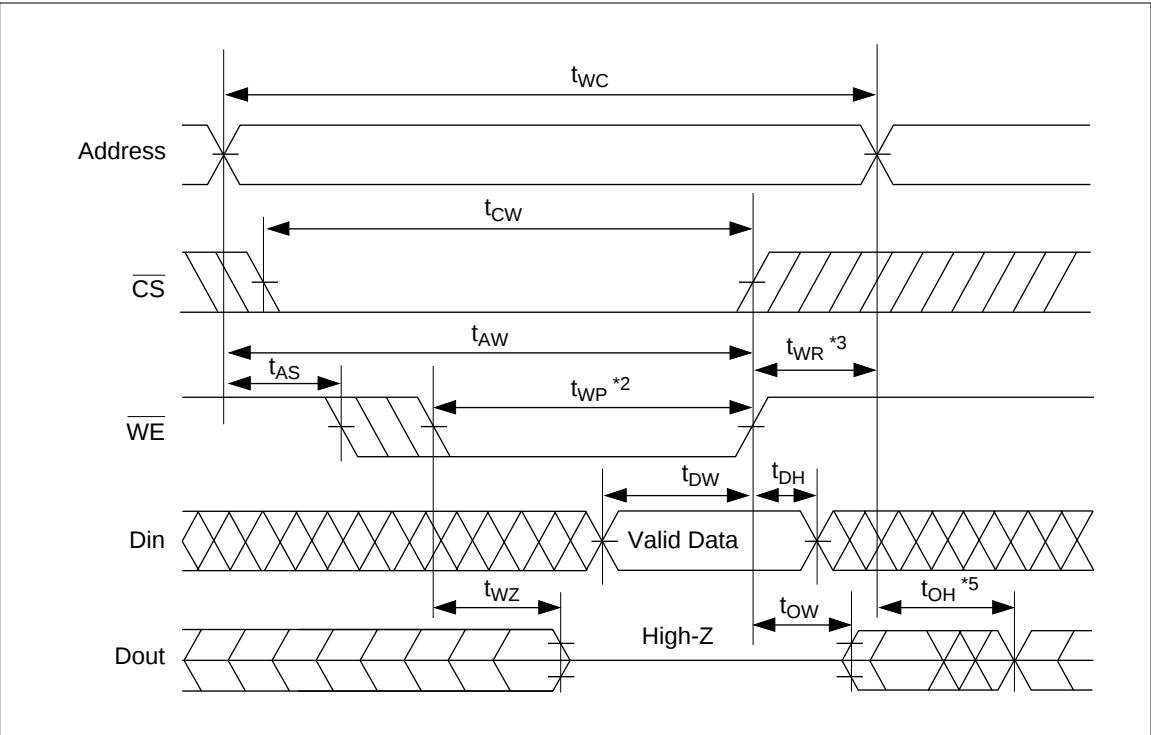


- Notes:
1. Transition is measured ± 200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
 2. $\overline{WE}$ is high for read cycle.
 3. Device is continuously selected, $\overline{CS} = V_{IL}$.
 4. Address valid prior to or coincident with $\overline{CS}$ transition low.

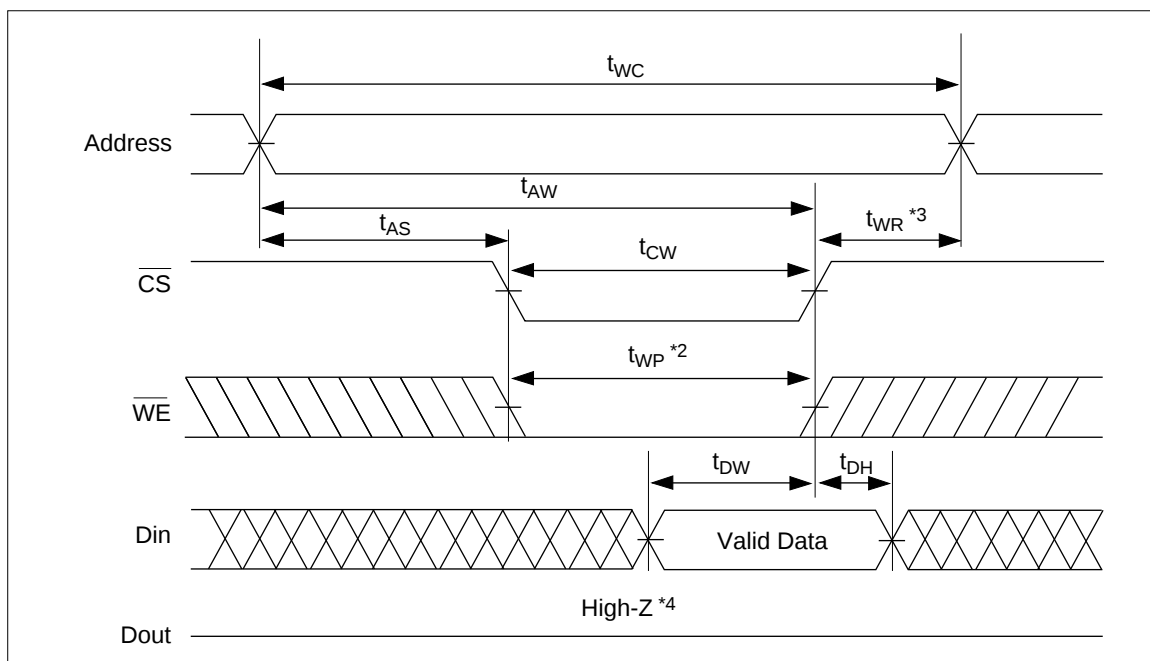
Write Cycle

Parameter	Symbol	HM621100A-20		HM621100A-25		HM621100A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	20	—	25	—	35	—	ns
Chip selection to end of write	t_{CW}	15	—	17	—	25	—	ns
Address valid to end of write	t_{AW}	16	—	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	17	—	25	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Write to output in high-Z	t_{WZ}^{*1}	0	12	0	15	0	15	ns
Data to write time overlap	t_{DW}	12	—	15	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}^{*1}	0	—	0	—	0	—	ns

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) (CS Controlled)



- Notes:
1. Transition is measured ± 200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
 2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
 3. t_{WR}^{*3} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
 4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
 5. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

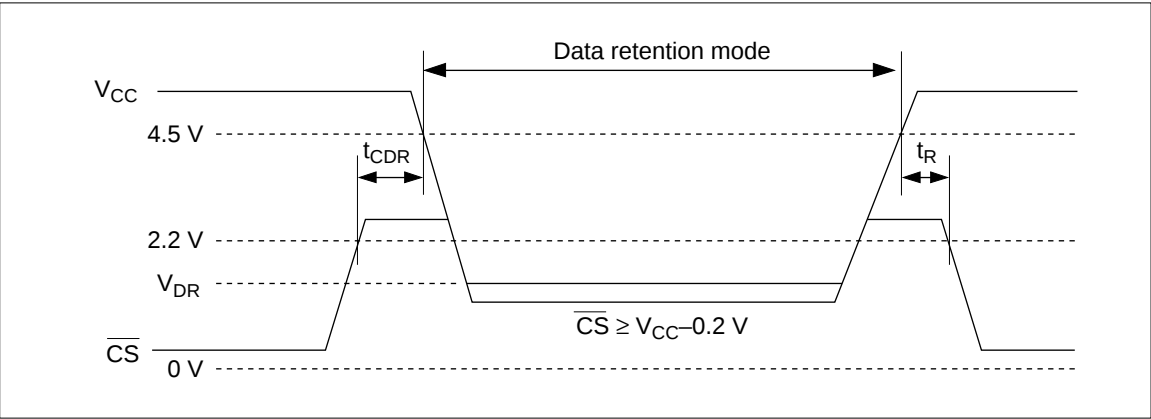
Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^{\circ}\text{C}$)

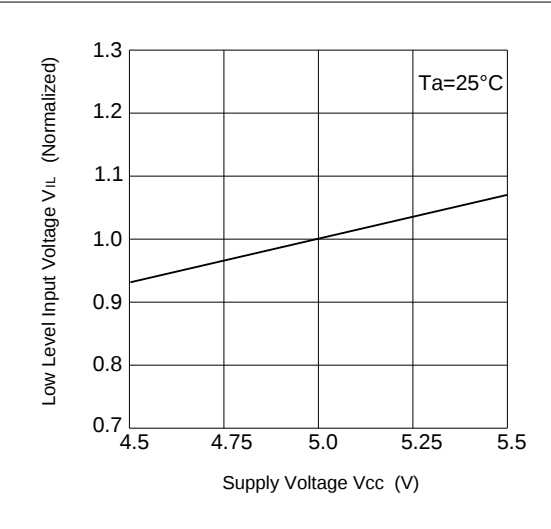
This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$, $V_{in} \geq V_{CC} - 0.2\text{ V}$ or $0\text{ V} \leq V_{in} \leq 0.2\text{ V}$
Data retention current	I_{CCDR}	—	2	50^{*1}	μA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

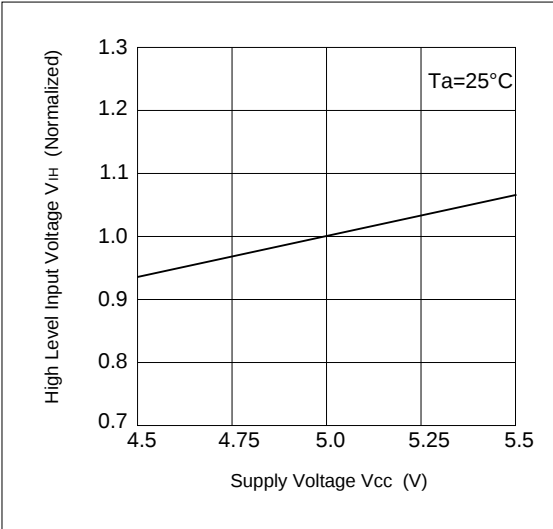
Note: 1. $V_{CC} = 3.0\text{ V}$

Low V_{CC} Data Retention Timing Waveform

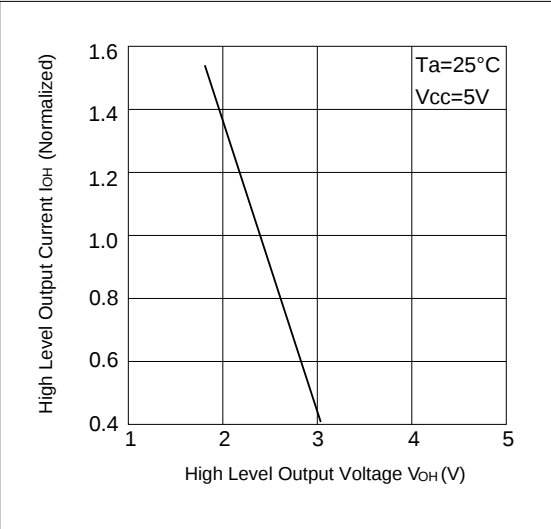




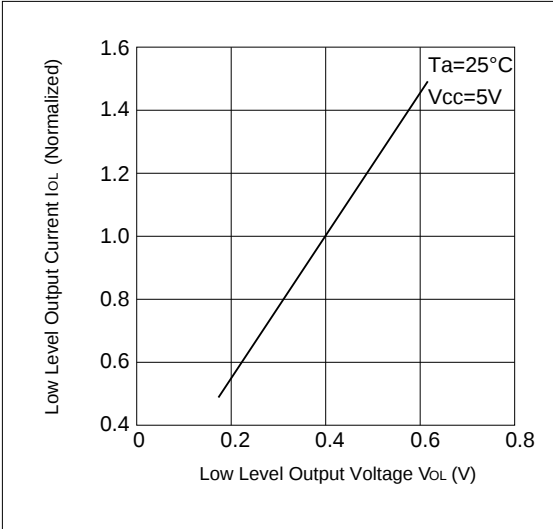
Low Level Input Voltage vs. Supply Voltage



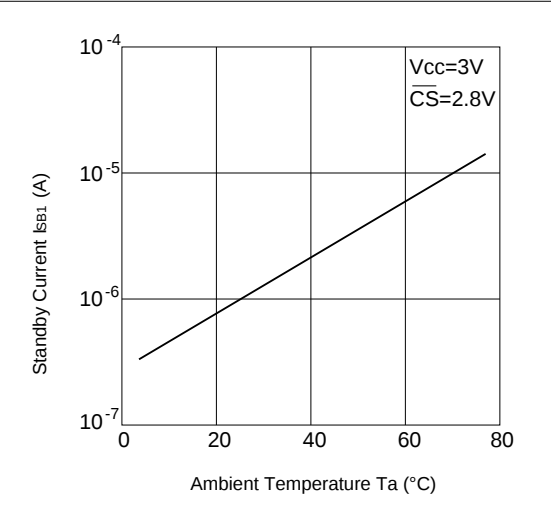
High Level Input Voltage vs. Supply Voltage



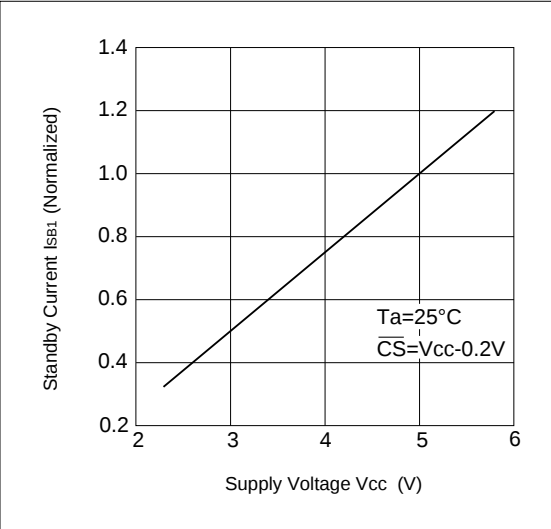
High Level Output Current vs. High Level Output Voltage



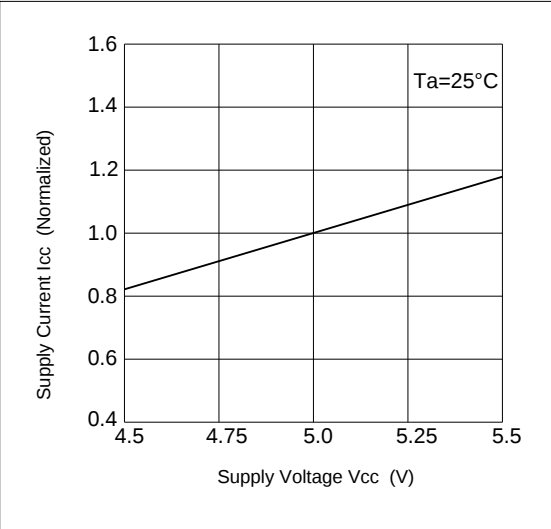
Low Level Output Current vs. Low Level Output Voltage



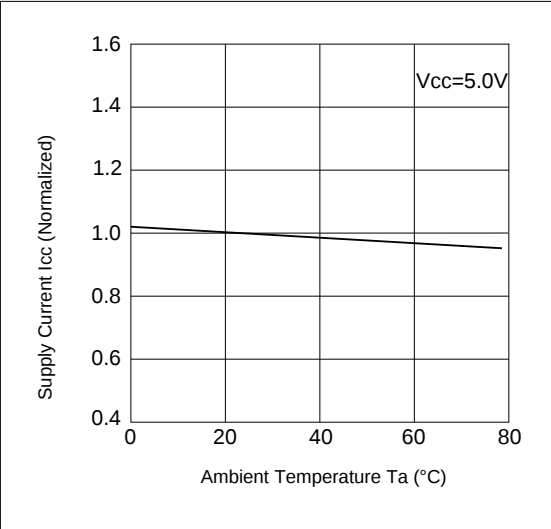
Standby Current vs. Ambient Temperature



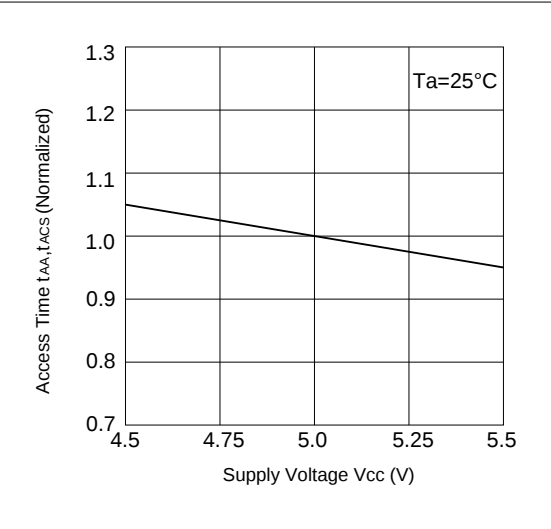
Standby Current vs. Supply Voltage



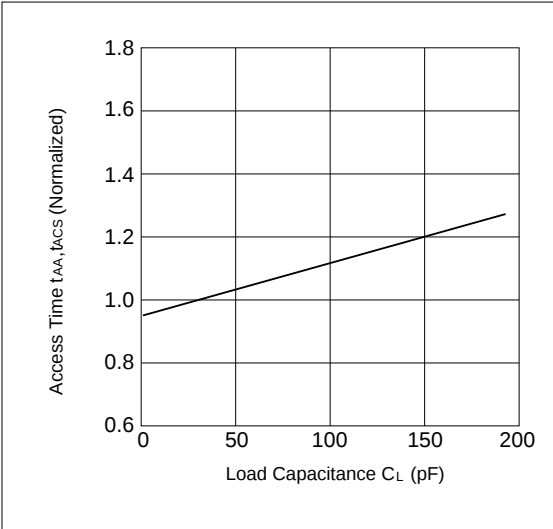
Supply Current vs. Supply Voltage



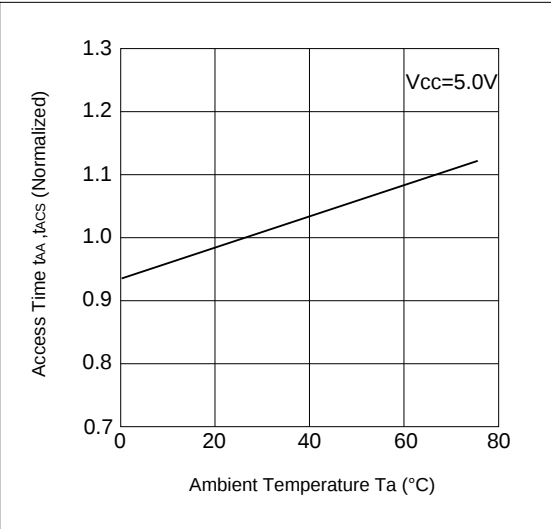
Supply Current vs. Ambient Temperature



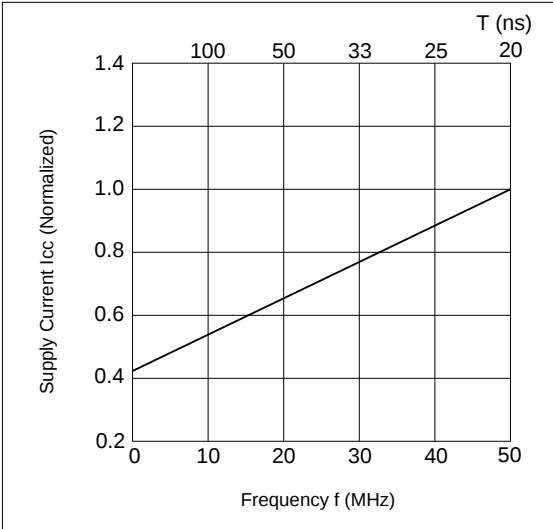
Access Time vs. Supply Voltage



Access Time vs. Load Capacitance



Access Time vs. Ambient Temperature



Supply Current vs. Frequency