

## Features

- High and low side gate driver
- Fully operational up to 200V
- Floating channel designed for bootstrap operation
- 2A source and sink currents
- Extended supply voltage range: 10V to 20V
- CMOS compatible inputs
- CMOS Schmitt-triggered inputs
- Outputs in phase with inputs
- Under Voltage Lock Out function
- Matched propagation delay times
- Automotive Qualified<sup>†</sup>
- Leadfree, RoHS compliant

## Product Summary

Topology	High & Low Side Driver
V <sub>S-MAX</sub>	200V
V <sub>OUT</sub>	10V – 20V
I <sub>o+</sub> & I <sub>o-</sub>	2 A
t <sub>ON</sub> & t <sub>OFF</sub>	60ns (typ)
Delay matching	20ns (max)

## Typical Applications

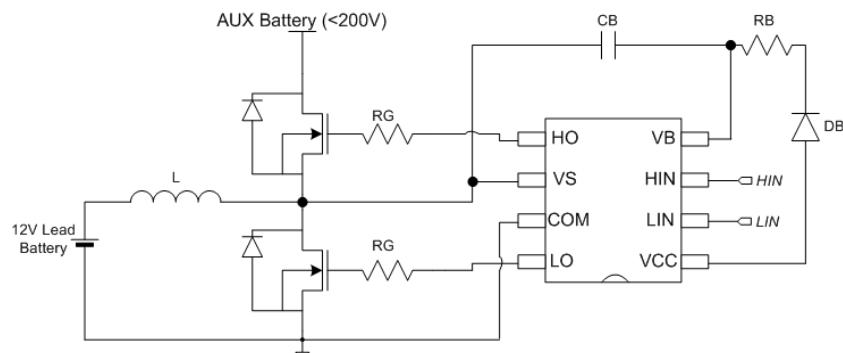
- Mid to low voltage DC-DC Converter for Micro and Mild Hybrid Vehicle
- Multiphase buck boost converters
- Direct Fuel Injection

## Package



SOIC-8N

## Typical Connection Diagram



Orderable Part Number	Package Type	Standard Pack		Note
		Form	Quantity	
AUIRS2012STR	SOIC8-N	Tape & Reel	2500	

## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM lead. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature ( $T_A$ ) is 25°C, unless otherwise specified.

Symbol	Definition	Min.	Max.	Units
$V_{CC}$	Fixed supply voltage	-0.3	20	V
$V_{LO}$	Low Side output voltage	-0.3	$V_{CC}+0.3$	
$V_{IN}$	Logic input voltage (HIN & LIN)	-0.3	5.0	
$V_B$	High side floating supply voltage	-0.3	$V_S+20$	
$V_S$	High side floating offset voltage	$V_B-20$	200	
$V_{HO}$	High Side floating output voltage	$V_S-0.3$	$V_B+0.3$	
$dV_S/dt$	Allowable offset transient	-	50	V/ns
$R_{thJA}$	Thermal resistance, junction to ambient	—	100	°C/W
$T_J$	Junction temperature	—	150	°C
$T_S$	Storage temperature	-55	150	
$T_L$	Lead temperature (soldering, 10 seconds)	—	300	

## Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltage referenced to COM.

Symbol	Definition	Min.	Max.	Units
$V_{CC}$	Fixed supply voltage	10	20	V
$V_{LO}$	Low Side output voltage	0	$V_{CC}$	
$V_{IN}$	Logic input voltage (HIN & LIN)	COM	5.0	
$V_B$	High side floating supply voltage	$V_S+10$	$V_S+20$	
$V_S$	High side floating offset voltage	Note 1	200	
$V_{HO}$	High Side floating output voltage	$V_S$	$V_B$	
$F_{sw}$	Switching frequency**		400	kHz
$R_{in}$	Input resistance*	100	5k	Ω
$T_A$	Ambient Temperature	-40	125	°C

Note 1: Logic operational for VS of -5V to 200V. Logic state held of -5V to -VBS.

\* input resistance value to be calculated based on the desired rise time and switching frequency.

\*\* thermal balance to be verified accordingly

## Static Electrical Characteristics

Unless otherwise specified, these specifications apply for an operating junction temperature range of  $-40^{\circ}\text{C} \leq \text{Ta} \leq 125^{\circ}\text{C}$  and power supplies  $V_{\text{BIAS}}$  (i.e.  $V_{\text{CC}}$  &  $V_{\text{BS}}$ ) = 15V. The  $V_{\text{IN}}$ ,  $V_{\text{TH}}$  and  $I_{\text{IN}}$  parameters are referenced to COM and are applicable to all logic input leads: HIN and LIN. The  $V_{\text{O}}$  and  $I_{\text{O}}$  parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$V_{\text{IL}}$	Logic "0" input voltage			0.7	V	$V_{\text{CC}}=10\text{V}-20\text{V}$
$V_{\text{IH}}$	Logic "1" input voltage	2.5				
$V_{\text{OL}}$	Low Level output voltage			0.1		
$V_{\text{OH}}$	High Level output voltage, $V_{\text{BIAS}} - V_{\text{O}}$			2.45		
$I_{\text{IN+}}$	Logic "1" input bias current		40	60	$\mu\text{A}$	$V_{\text{IN}}=3.3\text{V}$
$I_{\text{IN-}}$	Logic "0" input bias current			2		$V_{\text{IN}}=0\text{V}$
$C_{\text{IN}}$	Equivalent input capacitance <sup>(†)</sup>		7		pF	
$I_{\text{QBS}}$	Quiescent $V_{\text{BS}}$ supply current		100	250	$\mu\text{A}$	$V_{\text{IN}}=0\text{V}$ or $3.3\text{V}$
$I_{\text{QCC}}$	Quiescent $V_{\text{CC}}$ supply current		100	250		
$I_{\text{LK}}$	Offset supply leakage current			20		$V_{\text{B}}=V_{\text{S}}=200\text{V}$
$V_{\text{CCUVHYS}}$	$V_{\text{CC}}$ supply undervoltage hysteresis		1		V	
$V_{\text{CCUV+}}$	$V_{\text{CC}}$ supply undervoltage turn on threshold	6	7	8		
$V_{\text{CCUV-}}$	$V_{\text{CC}}$ supply undervoltage turn off threshold	5	6	7		
$V_{\text{BSUVHYS}}$	$V_{\text{CC}}$ supply undervoltage hysteresis		1			
$V_{\text{BSUV+}}$	$V_{\text{CC}}$ supply undervoltage turn on threshold	6	7	8		
$V_{\text{BSUV-}}$	$V_{\text{CC}}$ supply undervoltage turn off threshold	5	6	7		
$I_{\text{O+}}$	Output high short circuit pulsed current <sup>(†)</sup>		2		A	$V_{\text{O}}=0\text{V}$ , $PW=10\text{us}$ , $\text{Ta}=25\text{C}$
$I_{\text{O-}}$	Output high short circuit pulsed current <sup>(†)</sup>		2			$V_{\text{O}}=15\text{V}$ , $PW=10\text{us}$ , $\text{Ta}=25\text{C}$

(†) Guaranteed by design

## Dynamic Electrical Characteristics

Unless otherwise specified, these specifications apply for an operating junction temperature range of  $-40^{\circ}\text{C} \leq \text{Ta} \leq 125^{\circ}\text{C}$  and power supplies  $V_{\text{BIAS}}$  (i.e.  $V_{\text{CC}} & V_{\text{BS}} = 15\text{V}$ ,  $\text{CL} = 1000\text{pF}$ ). Refer to Figure 1 for switching time definition.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
<b>Propagation delay characteristics</b>						
$t_{\text{ON}}$	Turn-on propagation delay	—	60	120	ns	VS=0V and 200V
$t_{\text{OFF}}$	Turn-off propagation delay	—	60	120		VS=0V and 200V
$t_r$	Turn-on rise time	—	22	46		
$t_f$	Turn-off fall time	—	15	35		
DM1	Channel to channel turn on delay matching			20		
DM2	Channel to channel turn off delay matching			20		

## Input/Output table

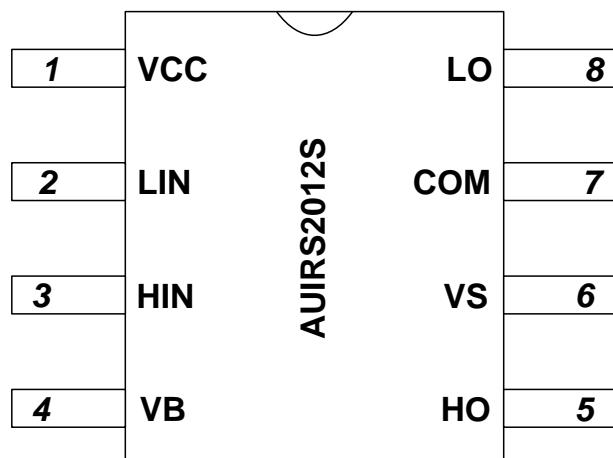
HIN	LIN	HO	LO
L	L	L	L
H	L	H	L
L	H	L	H
H	H	H	H

This table is held true in the voltages ranges defined in the recommended operating conditions section.

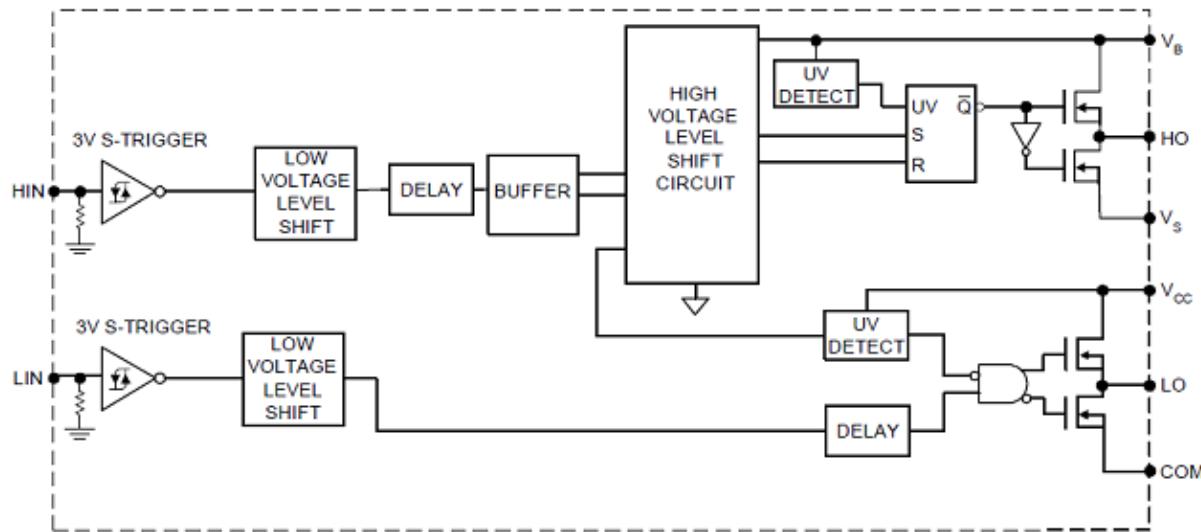
## Lead Definitions

PIN	Symbol	Description
1	VCC	Supply voltage
2	LIN	Logic input for low side gate driver – in phase with LO
3	HIN	Logic input for high side gate driver – in phase with HO
4	VB	High side floating supply
5	HO	High side gate drive output
6	VS	High side floating supply reference
7	COM	Low side reference
8	LO	Low side gate drive output

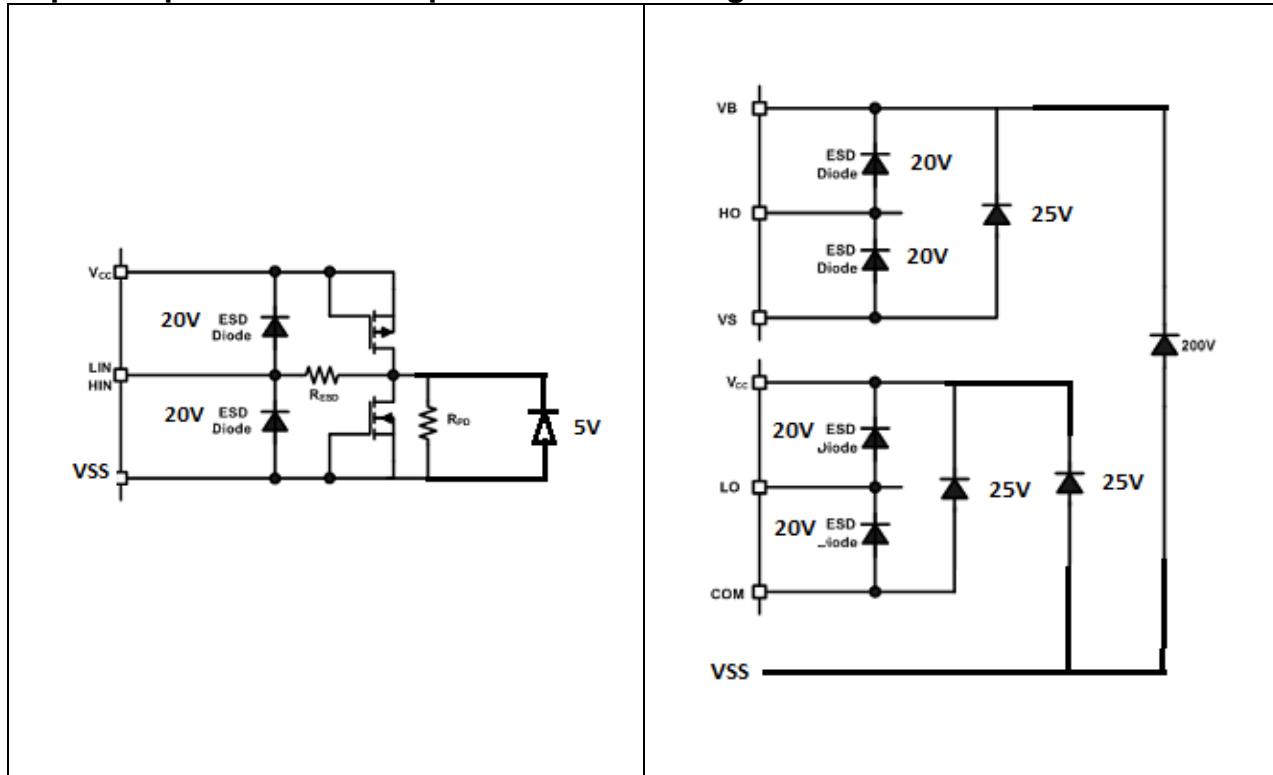
## Lead Assignment



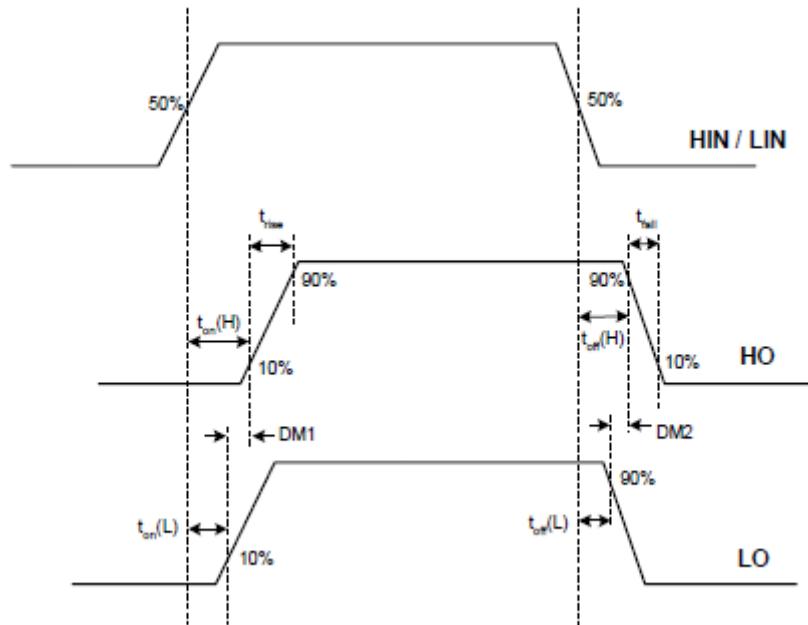
## Functional Block Diagram:



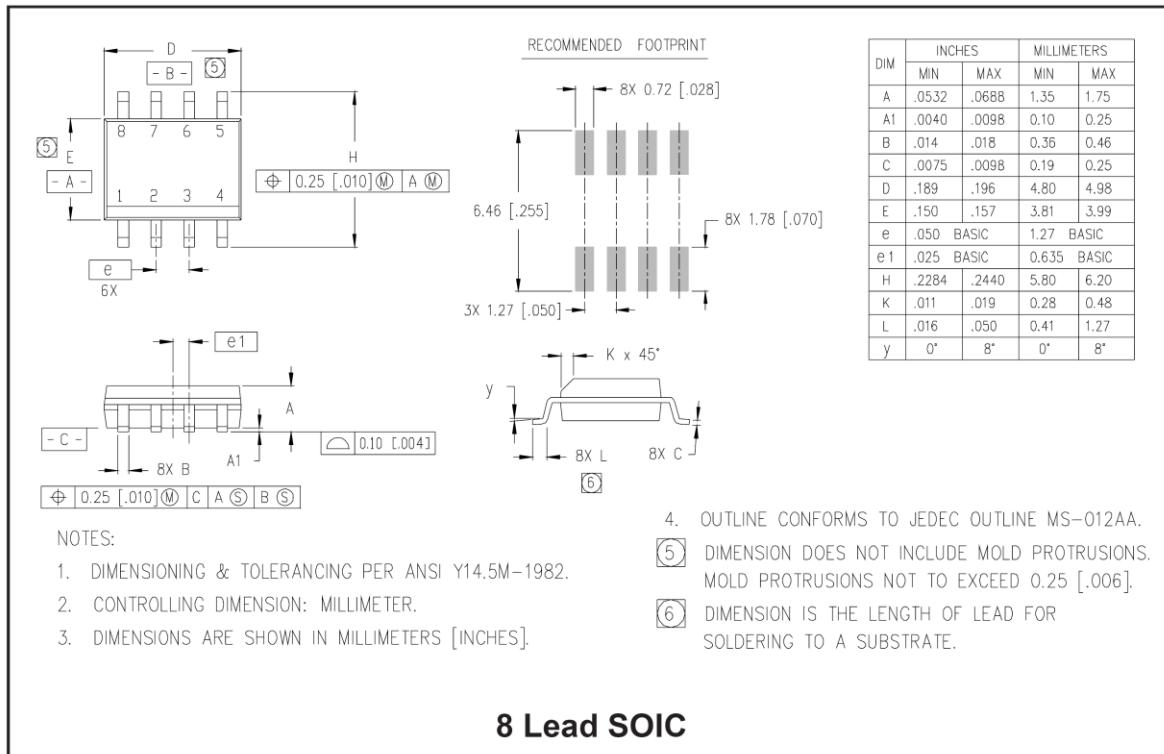
## Input/Output/Enable Pin Equivalent Circuit Diagrams



## Timing waveforms



## Package Information



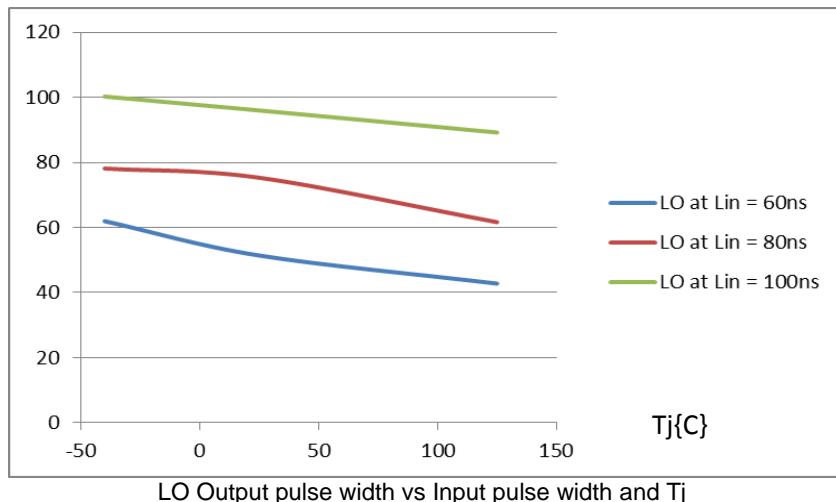
## Application Information

When using the AUIRS2012S, some precautions have to be taken when very short Hin/Lin pulses are applied. In the following figures, the typical output pulse versus input pulse width distortion is shown, for both HO and LO and for three different input pulse widths.

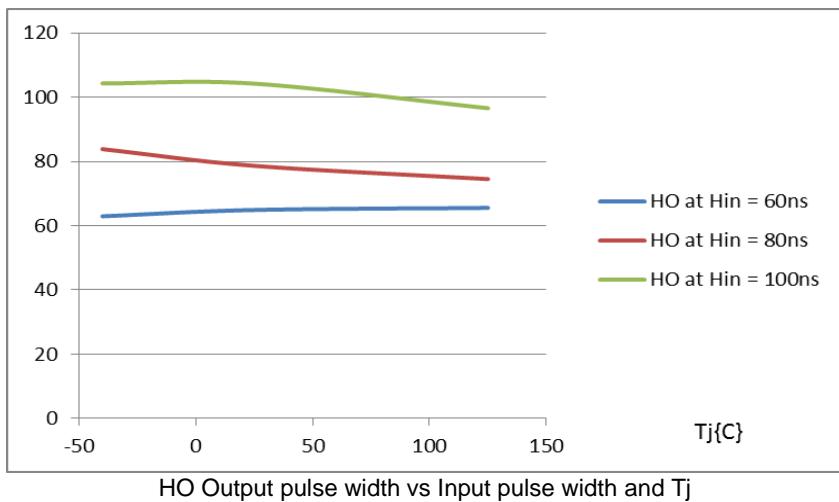
As an example, applying a 60nsec Lin results in a 60nsec LO only at very low temperatures. At far as  $T_j$  increases LO width decreases to a bit more than 40nsec when  $T_j = T_{jmax}$ .

Different is the case when Hin short pulse is applied. Because of the effect of the internal level shifter, the HO pulse width is more stable with temperature.

Output pulse width [ns]



Output pulse width [ns]



## Qualification Information

<b>Qualification Level</b>		Automotive (per AEC-Q100)	
		Comments: This part number passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		SOIC8-N	MSL3,260C (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Machine Model	Class M2 (150V) (per AEC-Q100-003)	
	Human Body Model	Class H2 (2500V) (AEC-Q100-002)	
	Charged Device Model	Class C4 (875V) (per AEC-Q100-011) AEC-Q101-005	
<b>IC Latch-UP Test</b>		Class II, Level A (per AEC-Q100-004)	
<b>RoHS Compliant</b>		Yes	

† Qualification standards can be found at International Rectifier web site: <http://www.irf.com>

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