

SN54ABT543, SN74ABT543 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS157A – JANUARY 1991 – REVISED JULY 1994

- State-of-the-Art *EPIC-II^B*™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

description

The 'ABT543 octal transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow.

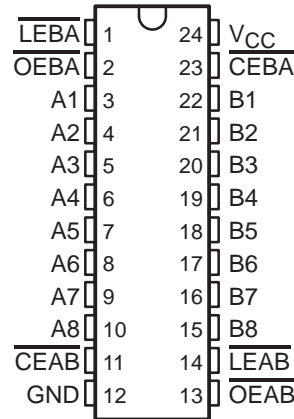
The A-to-B enable (\overline{CEAB}) input must be low in order to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

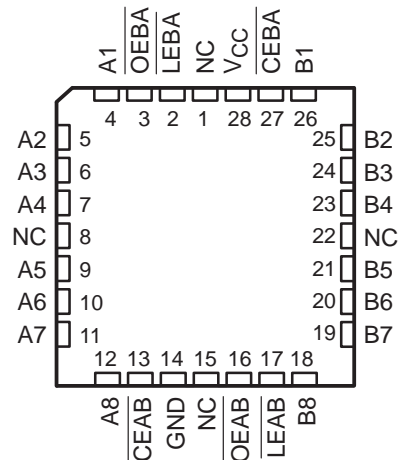
The SN74ABT543 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT543 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT543 is characterized for operation from -40°C to 85°C .

SN54ABT543 . . . JT PACKAGE
SN74ABT543 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT543 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

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**TEXAS
INSTRUMENTS**

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WITH 3-STATE OUTPUTS

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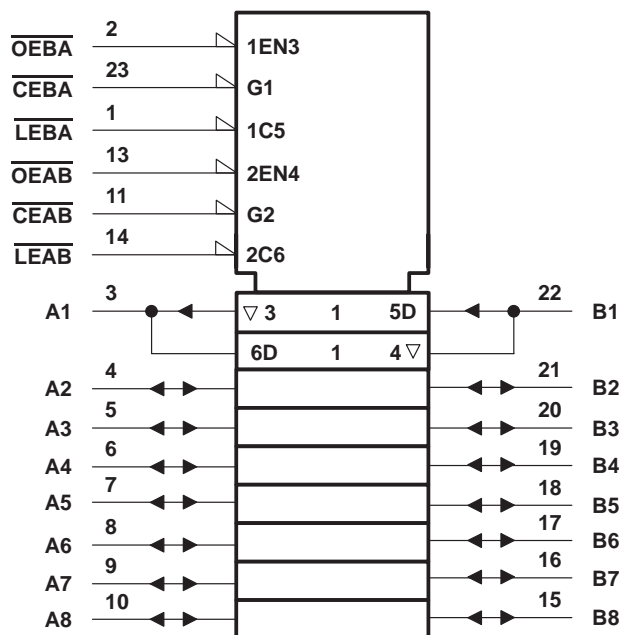
FUNCTION TABLE†

INPUTS				OUTPUT B
$\overline{\text{CEAB}}$	$\overline{\text{LEAB}}$	$\overline{\text{OEAB}}$	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0^\ddagger
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.

‡ Output level before the indicated steady-state input conditions were established.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, and NT packages.

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The diagram illustrates the logic for the A1 channel. It features six inputs: OEBA (2), CEBA (23), LEBA (1), OEAB (13), CEAB (11), and LEAB (14). These inputs are connected to four 2-input AND gates. The outputs of these AND gates are connected to a network of logic components including inverters, buffers (labeled C1 1D), and multiplexers. The final output is B1 (22). A bracket at the bottom indicates that this logic is replicated for the other six channels.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT543	96 mA
SN74ABT543	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package	0.65 W
DW package	1.7 W
NT package	1.3 W
Storage temperature range	-65°C to 150°C

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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recommended operating conditions (see Note 3)

			SN54ABT543		SN74ABT543		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$T_A = 25^\circ\text{C}$			SN54ABT543		SN74ABT543		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$				–1.2		–1.2		–1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$		2.5			2.5		2.5		V
	$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$		3			3		3		
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -24\text{ mA}$	2			2				
		$I_{OH} = -32\text{ mA}$	2*					2		
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$			0.55		0.55			V
		$I_{OL} = 64\text{ mA}$			0.55*				0.55	
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND	Control inputs			± 1		± 1		± 1	μA
		A or B ports			± 100		± 100		± 100	
I_{OZH}^\ddagger	$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$				10§		10§		10§	μA
I_{OZL}^\ddagger	$V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$				–10§		–10§		–10§	μA
I_{off}	$V_{CC} = 0$, V_I or $V_O \leq 4.5\text{ V}$				± 100				± 100	μA
I_{CEX}	$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$	Outputs high			50		50		50	μA
I_O^\parallel	$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND	A or B ports								
		Outputs high			1	250		250		μA
		Outputs low			24	34§		34§		mA
		Outputs disabled			0.5	250		250		μA
$\Delta I_{CC}^\#$	$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	$V_I = 2.5\text{ V}$ or 0.5 V	Control inputs			4					pF
C_{io}	$V_O = 2.5\text{ V}$ or 0.5 V	A or B ports			7					pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ This data sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		SN54ABT543		SN74ABT543		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, \overline{LEAB} or \overline{LEBA} low		3.5		3.5		3.5		ns
t_{su}	Setup time	Data before \overline{LEAB} or $\overline{LEBA}\uparrow$	High	3.5	3.5		3.5		ns
			Low	3	3		3		
		Data before \overline{CEAB} or $\overline{CEBA}\uparrow$	High	3.5	3.5		3.5		
			Low	3	3		3		
t_h	Hold time	Data after \overline{LEAB} or $\overline{LEBA}\uparrow$		1†	1†		1†		ns
		Data after \overline{CEAB} or $\overline{CEBA}\uparrow$		1†	1†		1†		

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

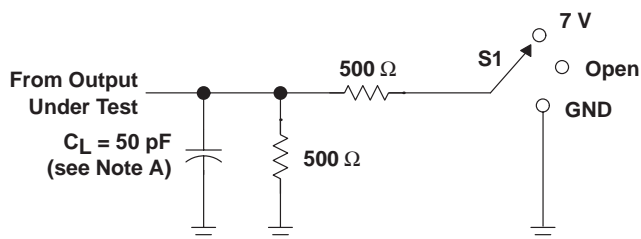
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$			SN54ABT543		SN74ABT543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.9	4.4	5.9	1.9		1.9	6.9	ns
t_{PHL}			1.9	4.4	5.9	1.9		1.9	6.9	
t_{PLH}	\overline{LEBA} or \overline{LEAB}	A or B	1.6	4.1	5.6	1.6		1.6	6.6	ns
t_{PHL}			2.1	4.6	6.1	2.1		2.1	7.1	
t_{PZH}	\overline{OEBA} or \overline{OEAB}	A or B	1.4	3.9	5.4	1.4		1.4	6.4	ns
t_{PZL}			2.5	5	6.5	2.5		2.5	7.5	
t_{PHZ}	\overline{OEBA} or \overline{OEAB}	A or B	2.5†	5.9	7.4	2.5†		2.5†	8.4	ns
t_{PLZ}			3	5.5	7	3		3	8	
t_{PZH}	\overline{CEBA} or \overline{CEAB}	A or B	1.4	3.9	5.4	1.4		1.4	6.4	ns
t_{PZL}			2.5	5	6.5	2.5		2.5	7.5	
t_{PHZ}	\overline{CEBA} or \overline{CEAB}	A or B	3.2†	5.9	7.4	3.2†		3.2†	8.4	ns
t_{PLZ}			3	5.5	7	3		3	8	

† This data sheet limit may vary among suppliers.

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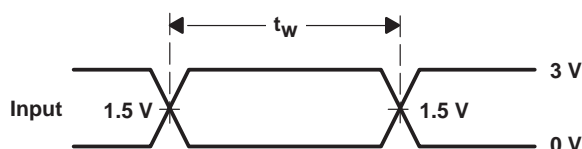
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PARAMETER MEASUREMENT INFORMATION

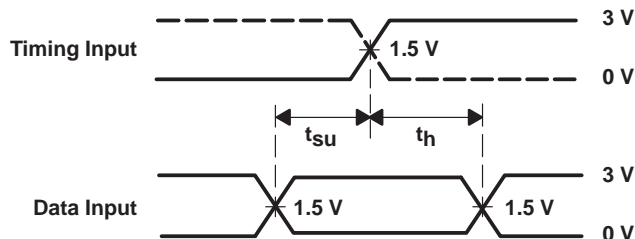


LOAD CIRCUIT FOR OUTPUTS

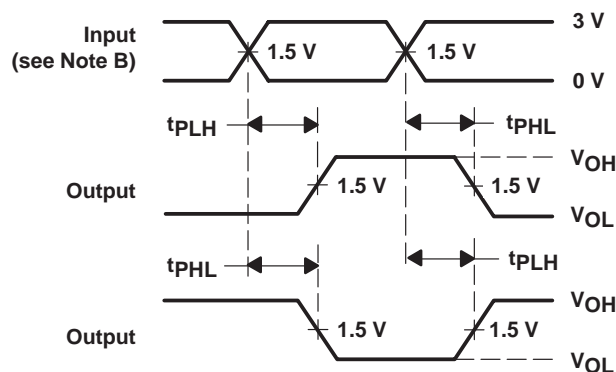
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



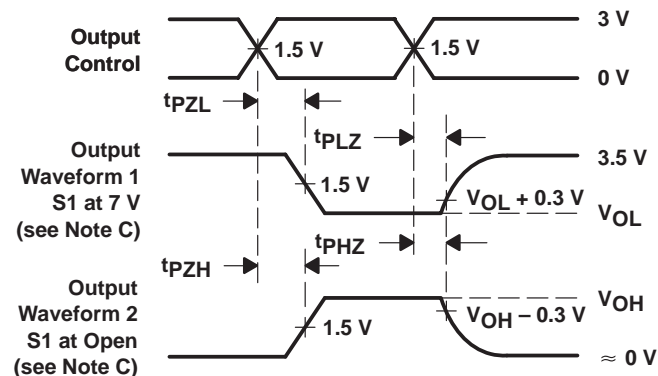
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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