

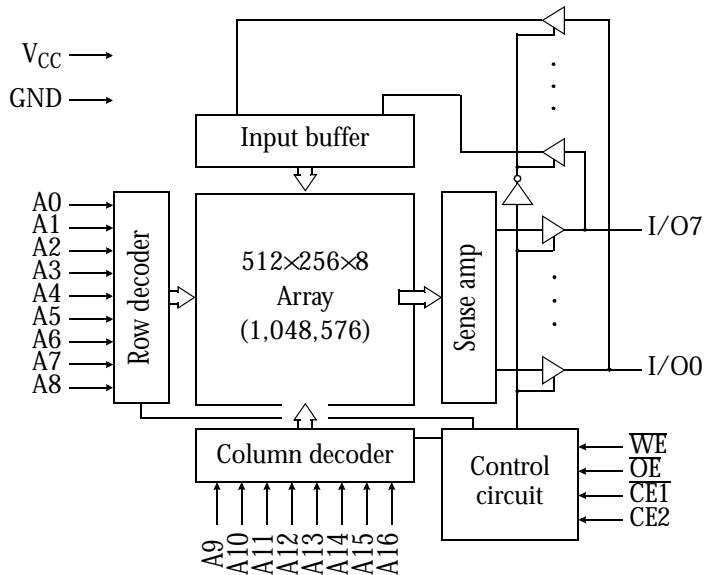


## 5V/3.3V 128K×8 CMOS SRAM (Evolutionary Pinout)

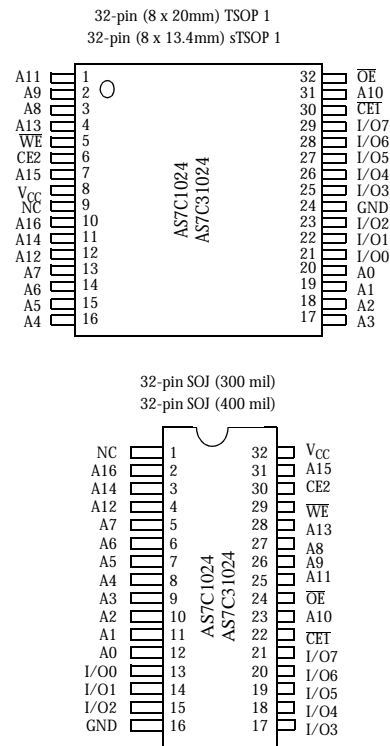
## Features

- AS7C1024 (5V version)
- AS7C31024 (3.3V version)
- Industrial and commercial temperatures
- Organization: 131,072 words × 8 bits
- High speed
  - 12/15/20 ns address access time
  - 6, 7, 8 ns output enable access time
- Low power consumption: ACTIVE
  - 825 mW (c) / max @ 12 ns
  - 360 mW (AS7C31024) / max @ 12 ns
- Low power consumption: STANDBY
  - 55 mW (AS7C1024) / max CMOS
  - 36 mW (AS7C31024) / max CMOS
- Easy memory expansion with  $\overline{CE1}$ , CE2,  $\overline{OE}$  inputs
- TTL/LVTTL-compatible, three-state I/O
- 32-pin JEDEC standard packages
  - 300 mil SOJ
  - 400 mil SOJ
  - 8 × 20mm TSOP 1
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

## Logic block diagram



## Pin arrangement



## Selection guide

		-12	-15	-20	Unit
Maximum address access time		12	15	20	ns
Maximum output enable access time		6	7	8	ns
Maximum operating current	AS7C1024	140	125	110	mA
	AS7C31024	90	80	75	mA
Maximum CMOS standby current	AS7C1024	10	10	15	mA
	AS7C31024	10	10	15	mA



## Functional description

The AS7C1024 and AS7C31024 are high performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) devices organized as 131,072 words  $\times$  8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times ( $t_{AA}$ ,  $t_{RC}$ ,  $t_{WC}$ ) of 12/15/20 ns with output enable access times ( $t_{OE}$ ) of 6, 7, 8 ns are ideal for high performance applications. Active high and low chip enables ( $\overline{CE1}$ , CE2) permit easy memory expansion with multiple-bank systems.

When  $\overline{CE1}$  is high or CE2 is low the devices enter standby mode. If inputs are still toggling, the device will consume  $I_{SB}$  power. If the bus is static, then full standby power is reached ( $I_{SB1}$  or  $I_{SB2}$ ). For example, the AS7C31024 is guaranteed not to exceed 0.33mW under nominal full standby conditions. All devices in this family will retain data when VCC is reduced as low as 2.0V.

A write cycle is accomplished by asserting write enable ( $\overline{WE}$ ) and both chip enables ( $\overline{CE1}$ , CE2). Data on the input pins I/O0-I/O7 is written on the rising edge of  $\overline{WE}$  (write cycle 1) or the active-to-inactive edge of  $\overline{CE1}$  or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ( $\overline{OE}$ ) or write enable ( $\overline{WE}$ ).

A read cycle is accomplished by asserting output enable ( $\overline{OE}$ ) and both chip enables ( $\overline{CE1}$ , CE2), with write enable ( $\overline{WE}$ ) high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable is inactive, output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

## Absolute maximum ratings

Parameter		Symbol	Min	Max	Unit
Voltage on V <sub>CC</sub> relative to GND	AS7C1024	V <sub>t1</sub>	-0.50	+7.0	V
	AS7C31024	V <sub>t1</sub>	-0.50	+5.0	V
Voltage on any pin relative to GND		V <sub>t2</sub>	-0.50	V <sub>CC</sub> +0.50	V
Power dissipation		P <sub>D</sub>	–	1.0	W
Storage temperature (plastic)		T <sub>stg</sub>	-65	+150	°C
Ambient temperature with V <sub>CC</sub> applied		T <sub>bias</sub>	-55	+125	°C
DC current into outputs (low)		I <sub>OUT</sub>	–	20	mA

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Truth table

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High Z	Standby ( $I_{SB}$ , $I_{SB1}$ )
X	L	X	X	High Z	Standby ( $I_{SB}$ , $I_{SB1}$ )
L	H	H	H	High Z	Output disable ( $I_{CC}$ )
L	H	H	L	D <sub>OUT</sub>	Read ( $I_{CC}$ )
L	H	L	X	D <sub>IN</sub>	Write ( $I_{CC}$ )

Key: X = Don't Care, L = Low, H = High



### Recommended operating conditions

Parameter	Device	Symbol	Min	Nominal	Max	Unit
Supply voltage	AS7C1024	$V_{CC}$	4.5	5.0	5.5	V
	AS7C31024	$V_{CC}$	3.0	3.3	3.6	V
Input voltage	AS7C1024	$V_{IH}$	2.2	–	$V_{CC} + 0.5$	V
	AS7C31024	$V_{IH}$	2.0	–	$V_{CC} + 0.5$	V
		$V_{IL}^{\dagger}$	–0.5	–	0.8	V
Ambient operating temperature	commercial	$T_A$	0	–	70	°C
	industrial	$T_A$	–40	–	85	°C

<sup>†</sup>  $V_{ILmin} = -3.0V$  for pulse width less than  $t_{RC/2}$ .

### DC operating characteristics (over the operating range)<sup>1</sup>

Parameter	Sym	Test conditions	Device	–12		–15		–20		Unit
				Min	Max	Min	Max	Min	Max	
Input leakage current	$ I_{LI} $	$V_{CC} = \text{Max}, V_{IN} = \text{GND to } V_{CC}$		–	1	–	1	–	1	μA
Output leakage current	$ I_{LO} $	$V_{CC} = \text{Max}, \overline{CE1} = V_{IH} \text{ or } CE2 = V_{IL}, V_{OUT} = \text{GND to } V_{CC}$		–	1	–	1	–	1	μA
Operating power supply current	$I_{CC}$	$V_{CC} = \text{Max}, \overline{CE1} = V_{IL}, CE2 = V_{IH}, f = f_{Max}, I_{OUT} = 0 \text{ mA}$	AS7C1024	–	140	–	125	–	110	mA
			AS7C31024	–	90	–	80	–	75	
Standby power supply current	$I_{SB}$	$V_{CC} = \text{Max}, \overline{CE1} \geq V_{IH} \text{ and/or } CE2 \leq V_{IL}, V_{IN} = V_{IH} \text{ or } V_{IL}, f = f_{Max}, I_{OUT} = 0 \text{ mA}$	AS7C1024	–	75	–	65	–	60	mA
			AS7C31024	–	50	–	40	–	35	
	$I_{SB1}$	$V_{CC} = \text{Max}, \overline{CE1} \geq V_{CC} - 0.2V, V_{IN} \leq \text{GND} + 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V, f = 0$	AS7C1024	–	10	–	10	–	15	mA
			AS7C31024	–	10	–	10	–	15	
Output voltage	$V_{OL}$	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$		–	0.4	–	0.4	–	0.4	V
	$V_{OH}$	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$		2.4	–	2.4	–	2.4	–	V

Shaded areas contain advance information.

### Capacitance ( $f = 1 \text{ MHz}, T_a = 25 \text{ °C}, V_{CC} = \text{NOMINAL}$ )<sup>2</sup>

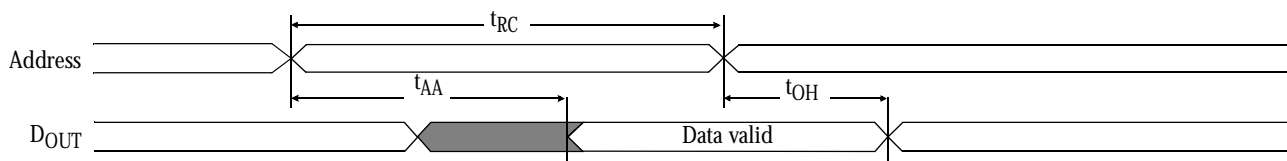
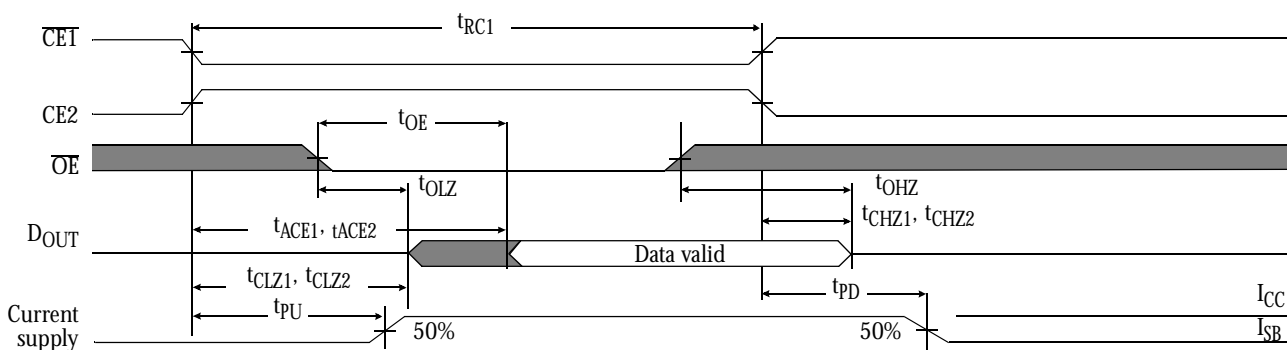
Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	$C_{IN}$	A, $\overline{CE1}$ , CE2, $\overline{WE}$ , $\overline{OE}$	$V_{IN} = 0V$	5	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{IN} = V_{OUT} = 0V$	7	pF

Read cycle (over the operating range)<sup>3,9,12</sup>

Parameter	Symbol	-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read cycle time	$t_{RC}$	12	–	15	–	20	–	ns	
Address access time	$t_{AA}$	–	12	–	15	–	20	ns	3
Chip enable ( $\overline{CE1}$ ) access time	$t_{ACE1}$	–	12	–	15	–	20	ns	3, 12
Chip enable (CE2) access time	$t_{ACE2}$	–	12	–	15	–	20	ns	3, 12
Output enable ( $\overline{OE}$ ) access time	$t_{OE}$	–	6	–	7	–	8	ns	
Output hold from address change	$t_{OH}$	3	–	3	–	3	–	ns	5
$\overline{CE1}$ Low to output in low Z	$t_{CLZ1}$	3	–	3	–	3	–	ns	4, 5, 12
CE2 High to output in low Z	$t_{CLZ2}$	3	–	3	–	3	–	ns	4, 5, 12
$\overline{CE1}$ Low to output in high Z	$t_{CHZ1}$	–	3	–	4	–	5	ns	4, 5, 12
CE2 Low to output in high Z	$t_{CHZ2}$	–	3	–	4	–	5	ns	4, 5, 12
$\overline{OE}$ Low to output in low Z	$t_{OLZ}$	0	–	0	–	0	–	ns	4, 5
$\overline{OE}$ High to output in high Z	$t_{OHZ}$	–	3	–	4	–	5	ns	4, 5
Power up time	$t_{PU}$	0	–	0	–	0	–	ns	4, 5, 12
Power down time	$t_{PD}$	–	12	–	15	–	20	ns	4, 5, 12

## Key to switching waveforms

Rising input     
 Falling input     
 Undefined / don't care

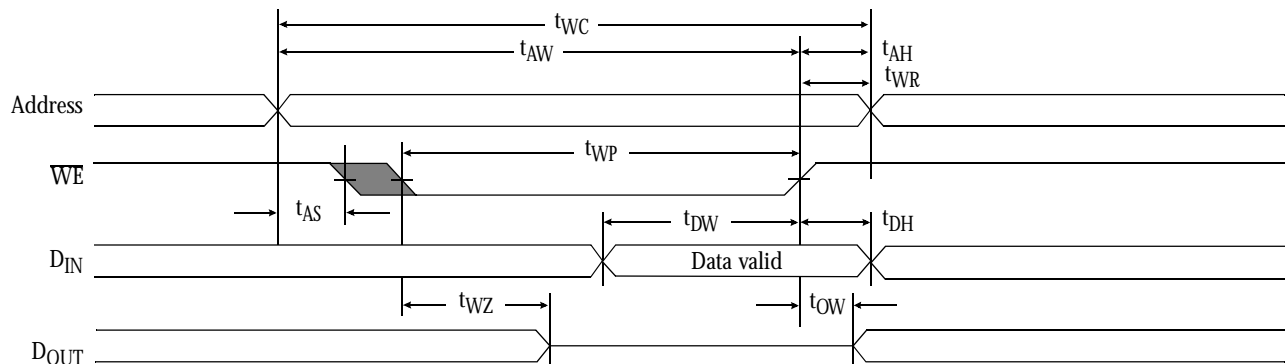
Read waveform 1 (address controlled)<sup>3,6,7,9,12</sup>Read waveform 2 ( $\overline{CE1}$ , CE2, and  $\overline{OE}$  controlled)<sup>3,6,8,9,12</sup>



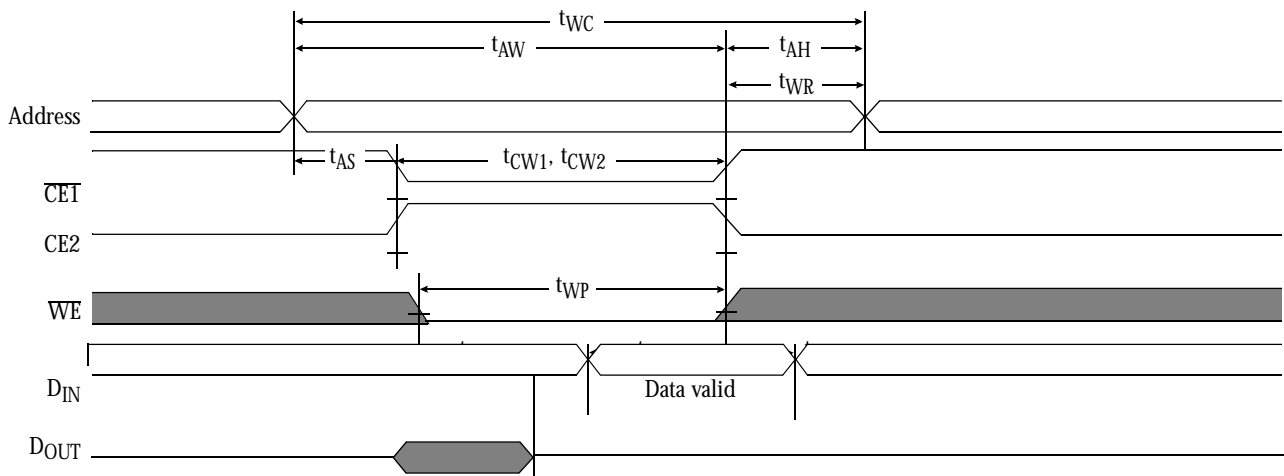
### Write cycle (over the operating range)<sup>11, 12</sup>

Parameter	Symbol	-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write cycle time	$t_{WC}$	12	–	15	–	20	–	ns	
Chip enable ( $\overline{CE1}$ ) to write end	$t_{CW1}$	10	–	12	–	12	–	ns	12
Chip enable ( $\overline{CE2}$ ) to write end	$t_{CW2}$	10	–	12	–	12	–	ns	12
Address setup to write end	$t_{AW}$	10	–	12	–	12	–	ns	
Address setup time	$t_{AS}$	0	–	0	–	0	–	ns	12
Write pulse width	$t_{WP}$	8	–	9	–	12	–	ns	
Write recovery time	$t_{WR}$	0	–	0	–	0	–	ns	
Address hold from end of write	$t_{AH}$	0	–	0	–	0	–	ns	
Data valid to write end	$t_{DW}$	6	–	9	–	10	–	ns	
Data hold time	$t_{DH}$	0	–	0	–	0	–	ns	4, 5
Write enable to output in high Z	$t_{WZ}$	–	5	–	5	–	5	ns	4, 5
Output active from write end	$t_{OW}$	3	–	3	–	3	–	ns	4, 5

### Write waveform 1 ( $\overline{WE}$ controlled)<sup>10,11,12</sup>



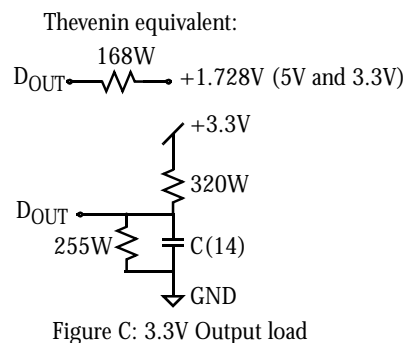
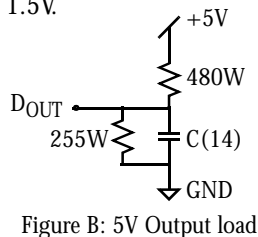
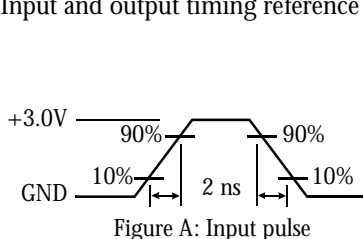
### Write waveform 2 ( $\overline{CE1}$ and $\overline{CE2}$ controlled)<sup>10,11,12</sup>





## AC test conditions

- 5V output load: see Figure B or Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

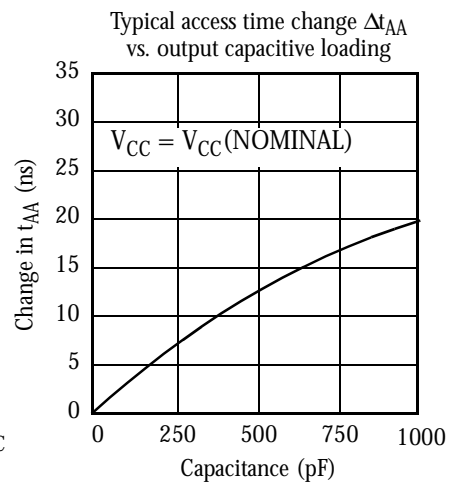
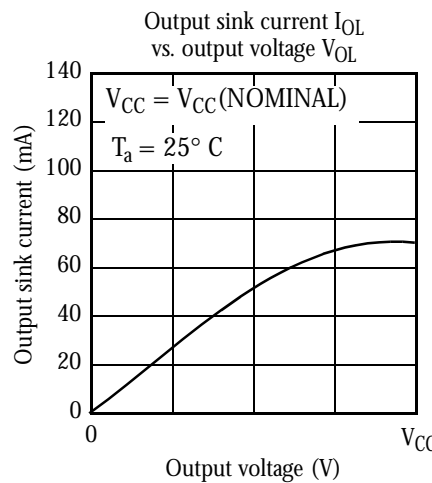
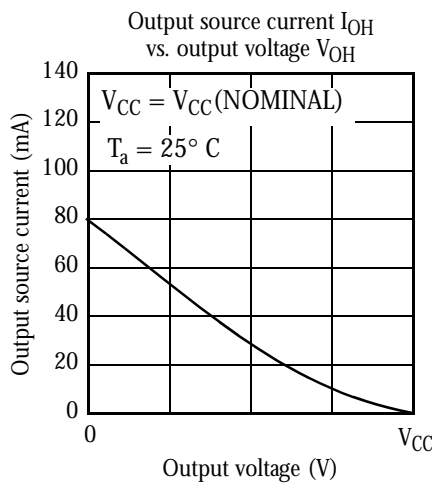
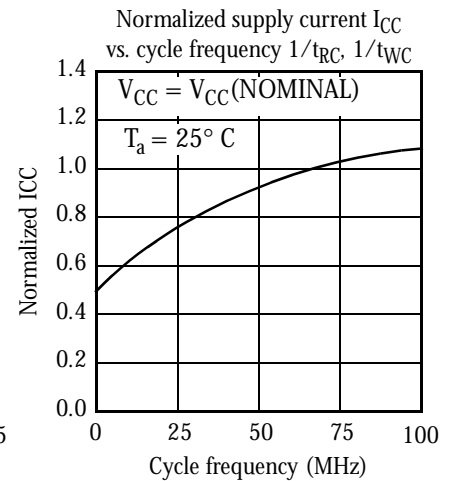
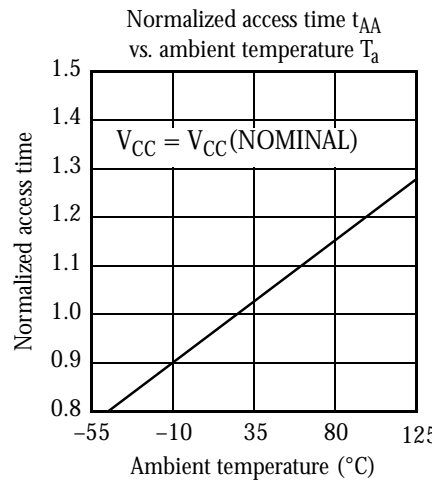
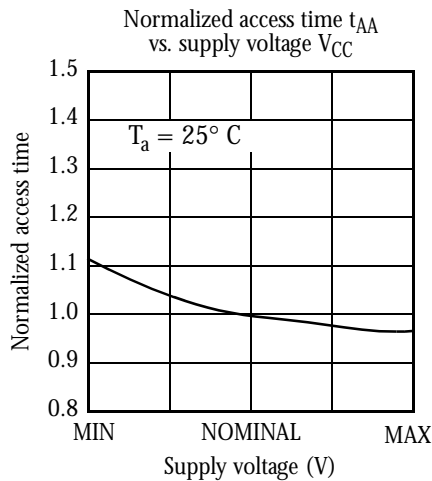
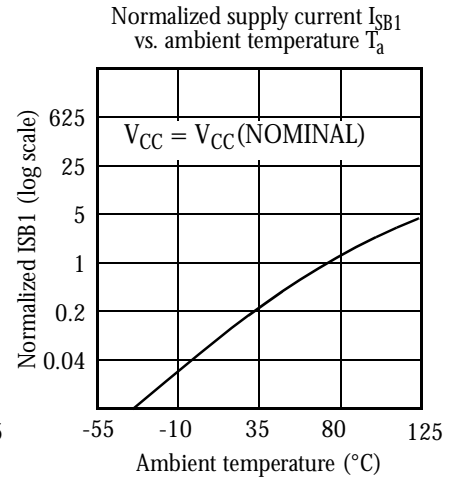
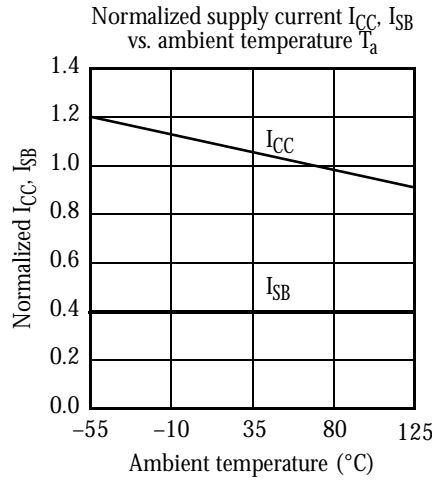
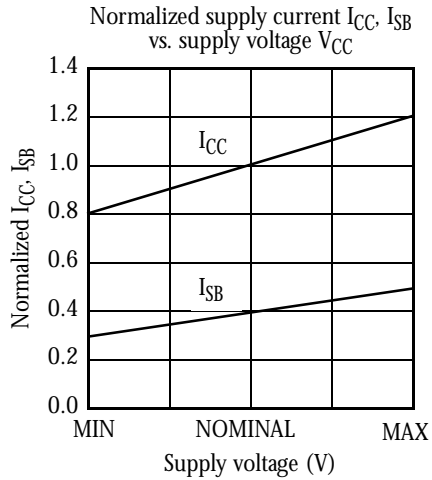


## Notes

- 1 During  $V_{CC}$  power-up, a pull-up resistor to  $V_{CC}$  on  $\overline{CE1}$  is required to meet  $I_{SB}$  specification.
- 2 This parameter is sampled and not 100% tested.
- 3 For test conditions, see AC Test Conditions, Figures A, B, and C.
- 4  $t_{CLZ}$  and  $t_{CHZ}$  are specified with  $C_L = 5\text{pF}$ , as in Figure C. Transition is measured  $\pm 500\text{mV}$  from steady-state voltage.
- 5 This parameter is guaranteed, but not 100% tested.
- 6  $\overline{WE}$  is High for read cycle.
- 7  $\overline{CE1}$  and  $\overline{OE}$  are Low and  $\overline{CE2}$  is High for read cycle.
- 8 Address valid prior to or coincident with  $\overline{CE1}$  transition Low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10  $\overline{CE1}$  or  $\overline{WE}$  must be High or  $\overline{CE2}$  Low during address transitions. Either  $\overline{CE1}$  or  $\overline{WE}$  asserting high terminates a write cycle.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12  $\overline{CE1}$  and  $\overline{CE2}$  have identical timing
- 13  $C = 30\text{pF}$ , except all high Z and low Z parameters,  $C = 5\text{pF}$ .

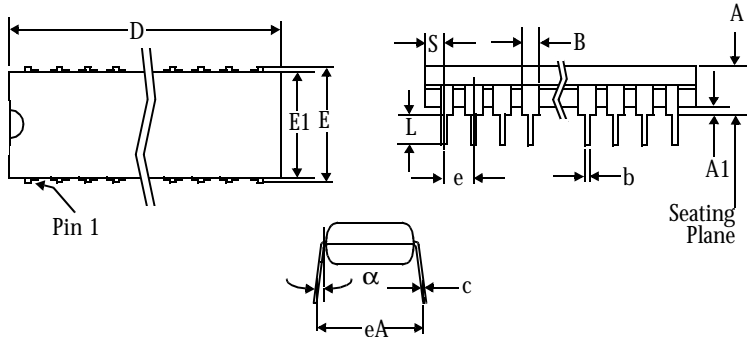


## Typical DC and AC characteristics

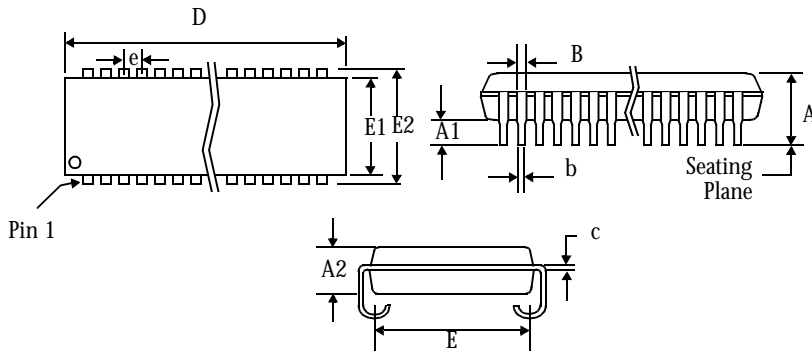




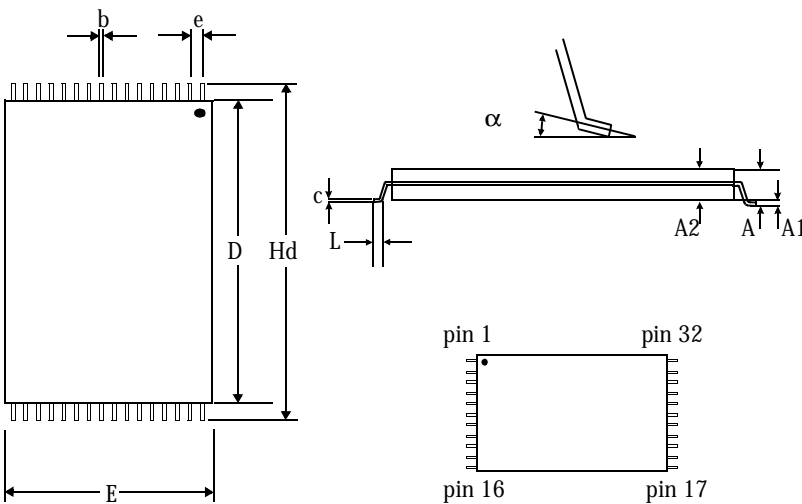
## Package dimensions



	32-pin PDIP	
	Min in mils	Max in mils
A	-	0.180
A1	0.015	-
B	0.045	0.055
b	0.015	0.021
c	0.008	0.012
D	-	1.571
E	0.300	0.325
E1	0.280	0.295
e	0.100 BSC	
eA	0.330	0.370
L	0.110	0.142
a	0°	15°
S	-	0.043



	32-pin SOJ 300 mil		32-pin SOJ 400 mil	
	Min	Max	Min	Max
A	-	0.145	-	0.145
A1	0.025	-	0.025	-
A2	0.086	0.105	0.086	0.115
B	0.026	0.032	0.026	0.032
b	0.014	0.020	0.015	0.020
c	0.006	0.013	0.007	0.013
D	0.820	0.830	0.820	0.830
E	0.250	0.275	0.360	0.380
E1	0.292	0.305	0.395	0.405
E2	0.330	0.340	0.435	0.445
e	0.050 BSC		0.050 BSC	



	32-pin TSOP 8x20 mm	
	Min in mm	Max in mm
A	-	1.20
A1	0.05	0.15
A2	0.95	1.05
b	0.17	0.27
c	0.10	0.21
D	18.20	18.60
e	0.50 nominal	
E	7.80	8.20
Hd	19.80	20.20
L	0.50	0.70
α	0°	5°





## Ordering codes

Package \ Access time	Volt/Temp	12 ns	15 ns	20 ns
Plastic SOJ, 300 mil	5V commercial	AS7C1024-12TJC	AS7C1024-15TJC	AS7C1024-20TJC
	5V industrial	AS7C1024-12TJI	AS7C1024-15TJI	AS7C1024-20TJI
	3.3V commercial	AS7C31024-12TJC	AS7C31024-15TJC	AS7C31024-20TJC
	3.3V industrial	AS7C31024-12TJI	AS7C31024-15TJI	AS7C31024-20TJI
Plastic SOJ, 400 mil	5V commercial	AS7C1024-12JC	AS7C1024-15JC	AS7C1024-20JC
	5V industrial	AS7C1024-12JI	AS7C1024-15JI	AS7C1024-20JI
	3.3V commercial	AS7C31024-12JC	AS7C31024-15JC	AS7C31024-20JC
	3.3V industrial	AS7C31024-12JI	AS7C31024-15JI	AS7C31024-20JI
TSOP 8 × 20 mm	5V commercial	AS7C1024-12TC	AS7C1024-15TC	AS7C1024-20TC
	5V industrial	AS7C1024-12TI	AS7C1024-15TI	AS7C1024-20TI
	3.3V commercial	AS7C31024-12TC	AS7C31024-15TC	AS7C31024-20TC
	3.3V industrial	AS7C31024-12TI	AS7C31024-15TI	AS7C31024-20TI

## Part numbering system

AS7C	X	1024	-XX	X	X
SRAM prefix	Blank=5V CMOS 3=3.3V CMOS	Device number	Access time	Package: TP=PDIP 300 mil T=TSOP1 8×20 mm J=SOJ 400 mil TJ=SOJ 300 mil	Temperature range C = Commercial, 0°C to 70°C I = Industrial, -40°C to 85°C