

Video Amplifier

NE592

The NE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

Features

- 120 MHz Unity Gain Bandwidth
- Adjustable Gains from 0 to 400
- Adjustable Pass Band
- No Frequency Compensation Required
- Wave Shaping with Minimal External Components
- MIL-STD Processing Available
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Floppy Disk Head Amplifier
- Video Amplifier
- Pulse Amplifier in Communications
- Magnetic Memory
- Video Recorder Systems

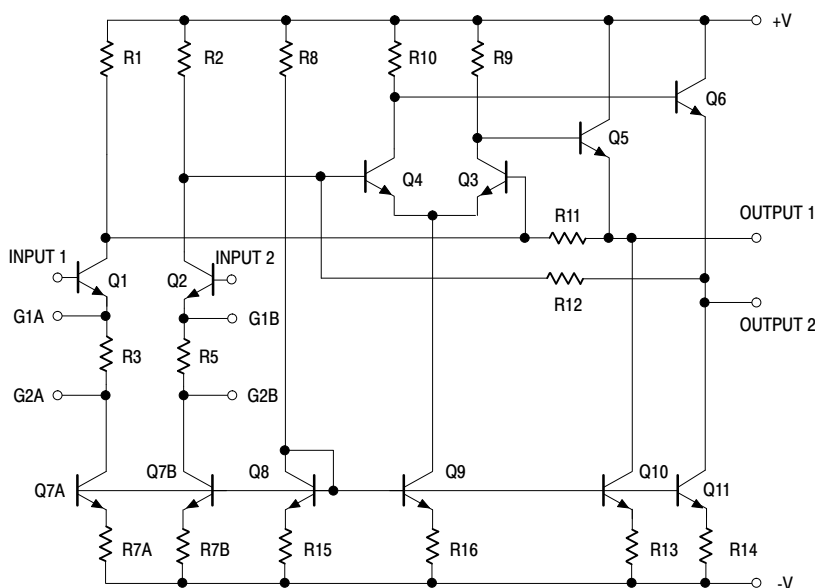
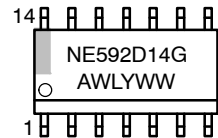
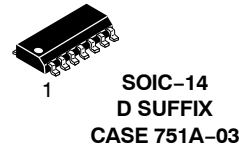
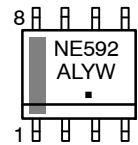
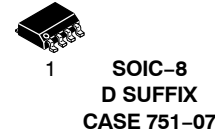


Figure 1. Block Diagram

MARKING DIAGRAMS



A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week
▪ or G = Pb-Free Package

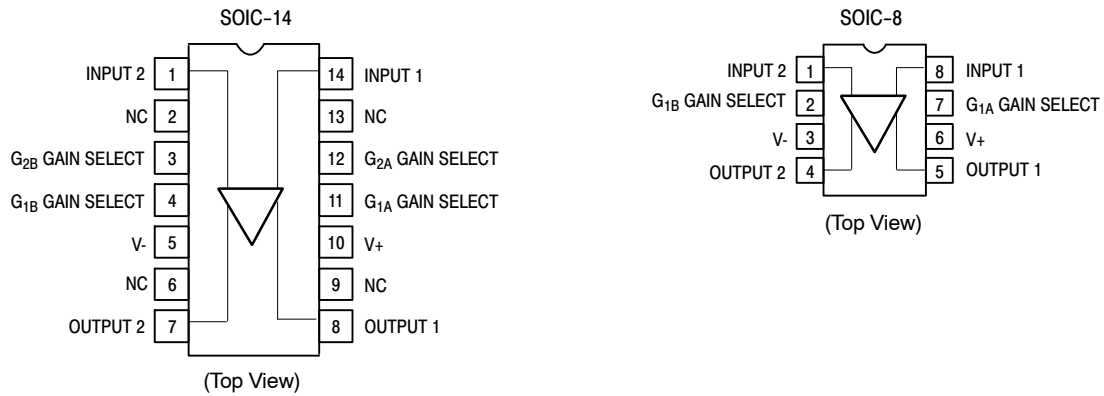
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 8.

NE592

PIN CONNECTIONS



MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	±8.0	V
Differential Input Voltage	V _{IN}	±5.0	V
Common-Mode Input Voltage	V _{CM}	±6.0	V
Output Current	I _{OUT}	10	mA
Operating Ambient Temperature Range	T _A	0 to +70	°C
Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	65 to +150	°C
Maximum Power Dissipation, T _A = 25°C (Still Air) (Note 1) SOIC-14 Package SOIC-8 Package	P _{D MAX}	0.98 0.79	W
Thermal Resistance, Junction-to-Ambient SOIC-14 Package SOIC-8 Package	R _{θJA}	145 182	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Derate above 25°C at the following rates:
SOIC-14 package at 6.9 mW/°C
SOIC-8 package at 5.5 mW/°C

NE592

DC ELECTRICAL CHARACTERISTICS ($V_{SS} = \pm 6.0$ V, $V_{CM} = 0$, typicals at $T_A = +25^\circ\text{C}$, min and max at $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, unless otherwise noted. Recommended operating supply voltages $V_S = \pm 6.0$ V.)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
Differential Voltage Gain Gain 1 (Note 2) Gain 2 (Notes 3 and 4)	$R_L = 2.0$ k Ω , $V_{OUT} = 3.0$ V _{P-P}	A_{VOL}	250 80	400 100	600 120	V/V
Input Resistance Gain 1 (Note 2) Gain 2 (Notes 3 and 4)	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	R_{IN}	– 10 8.0	4.0 30 –	– – –	k Ω
Input Capacitance	Gain 2 (Note 4)	C_{IN}	–	2.0	–	pF
Input Offset Current	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	I_{OS}	– –	0.4 –	5.0 6.0	μA
Input Bias Current	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	I_{BIAS}	– –	9.0 –	30 40	μA
Input Noise Voltage	BW 1.0 kHz to 10 MHz	V_{NOISE}	–	12	–	μV_{RMS}
Input Voltage Range	–	V_{IN}	± 1.0	–	–	V
Common-Mode Rejection Ratio Gain 2 (Note 4)	$V_{CM} \pm 1.0$ V, $f < 100$ kHz, $T_A = 25^\circ\text{C}$ $V_{CM} \pm 1.0$ V, $f < 100$ kHz, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $V_{CM} \pm 1.0$ V, $f < 5.0$ MHz	CMRR	60 50 –	86 – 60	– – –	dB
Supply Voltage Rejection Ratio Gain 2 (Note 4)	$\Delta V_S = \pm 0.5$ V	PSRR	50	70	–	dB
Output Offset Voltage Gain 1 Gain 2 (Note 4) Gain 3 (Note 5) Gain 3 (Note 5)	$R_L = \infty$ $R_L = \infty$ $R_L = \infty$, $T_A = 25^\circ\text{C}$ $R_L = \infty$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	V_{OS}	– – – –	– – 0.35 –	1.5 1.5 0.75 1.0	V
Output Common-Mode Voltage	$R_L = \infty$, $T_A = 25^\circ\text{C}$	V_{CM}	2.4	2.9	3.4	V
Output Voltage Swing Differential	$R_L = 2.0$ k Ω , $T_A = 25^\circ\text{C}$ $R_L = 2.0$ k Ω , $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	V_{OUT}	3.0 2.8	4.0 –	– –	V
Output Resistance	–	R_{OUT}	–	20	–	Ω
Power Supply Current	$R_L = \infty$, $T_A = 25^\circ\text{C}$ $R_L = \infty$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	I_{CC}	– –	18 –	24 27	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{SS} = \pm 6.0$ V, $V_{CM} = 0$, unless otherwise noted. Recommended operating supply voltages $V_S = \pm 6.0$ V.)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
Bandwidth Gain 1 (Note 2) Gain 2 (Notes 3 and 4)	–	BW	– –	40 90	– –	MHz
Rise Time Gain 1 (Note 2) Gain 2 (Notes 3 and 4)	$V_{OUT} = 1.0$ V _{P-P}	t_R	– –	10.5 4.5	12 –	ns
Propagation Delay Gain 1 (Note 2) Gain 2 (Notes 3 and 4)	$V_{OUT} = 1.0$ V _{P-P}	t_{PD}	– –	7.5 6.0	10 –	ns

- Gain select Pins G_{1A} and G_{1B} connected together.
- Gain select Pins G_{2A} and G_{2B} connected together.
- Applies to 14-pin version only.
- All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

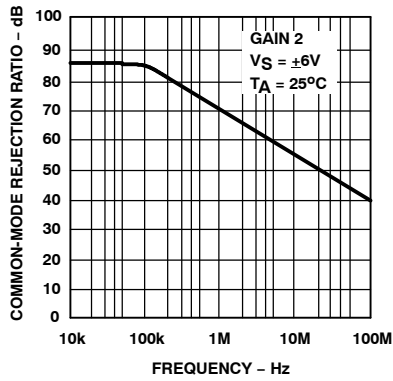


Figure 2. Common-Mode Rejection Ratio as a Function of Frequency

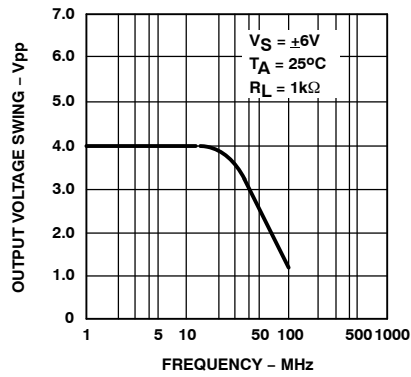


Figure 3. Output Voltage Swing as a Function of Frequency

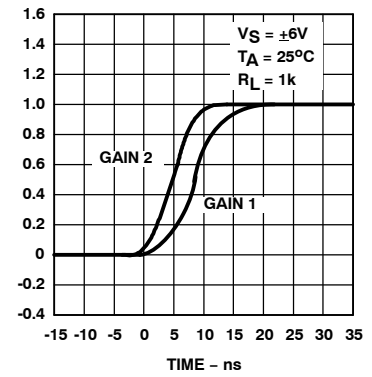


Figure 4. Pulse Response

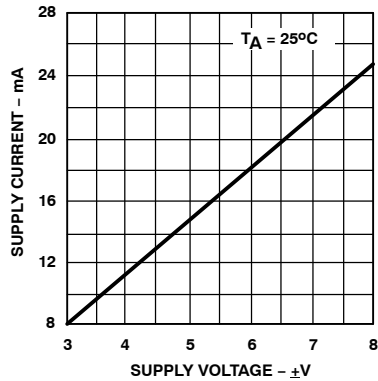


Figure 5. Supply Current as a Function of Temperature

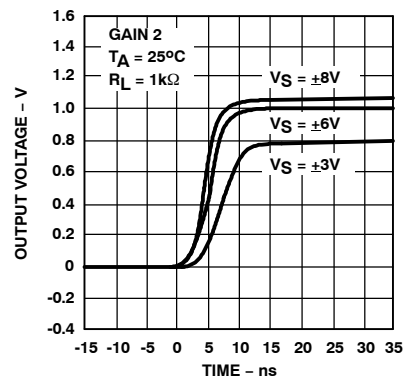


Figure 6. Pulse Response as a Function of Supply Voltage

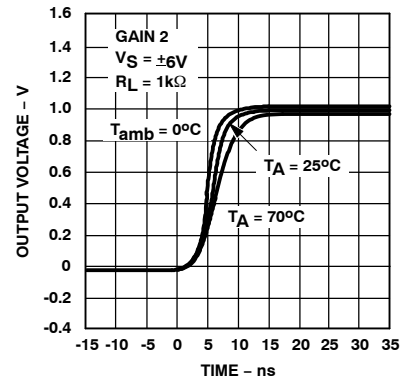


Figure 7. Pulse Response as a Function of Temperature

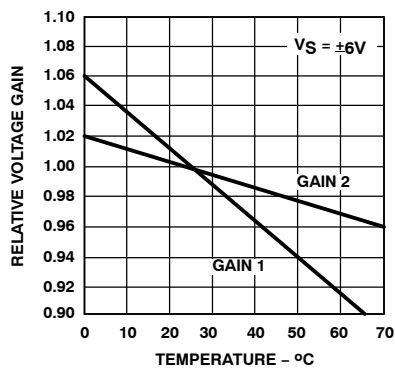


Figure 8. Voltage Gain as a Function of Temperature

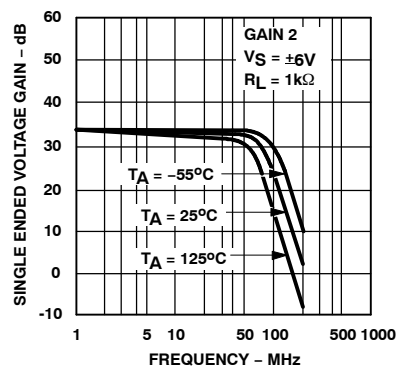


Figure 9. Gain vs. Frequency as a Function of Temperature

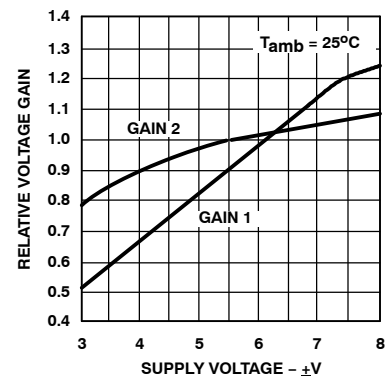


Figure 10. Voltage Gain as a Function of Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

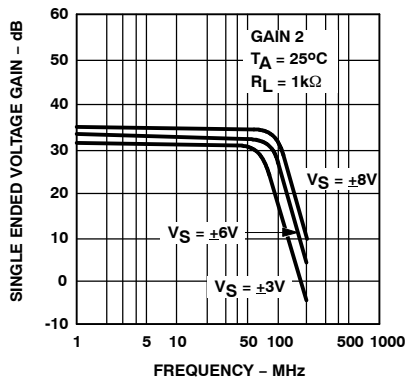


Figure 11. Gain vs. Frequency as a Function of Supply Voltage

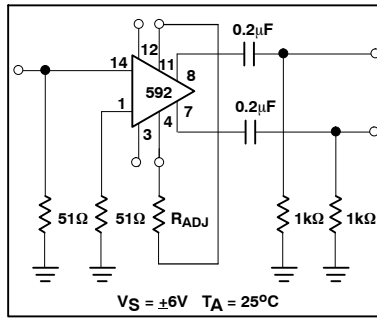


Figure 12. Voltage Gain Adjust Circuit

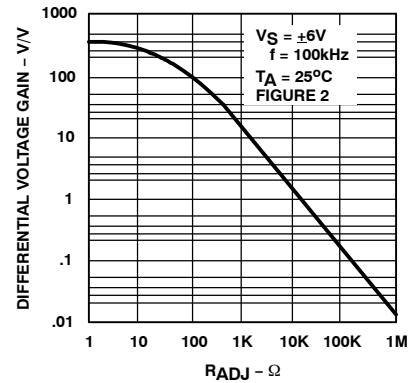


Figure 13. Voltage Gain as a Function of RADJ (Figure 2)

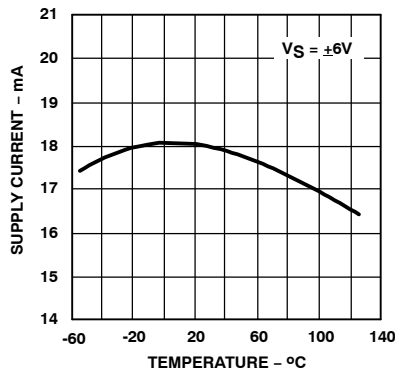


Figure 14. Supply Current as a Function of Temperature

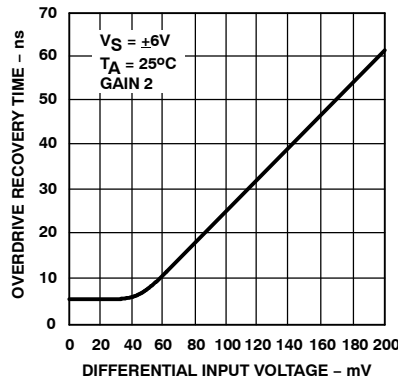


Figure 15. Differential Overdrive Recovery Time

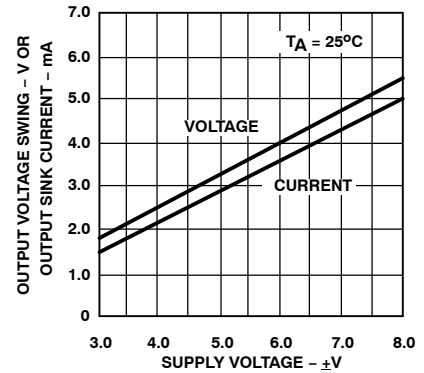


Figure 16. Output Voltage and Current Swing as a Function of Supply Voltage

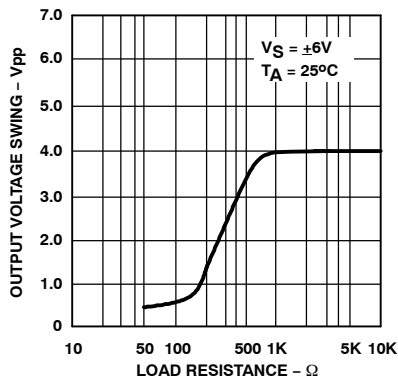


Figure 17. Output Voltage Swing as a Function of Load Resistance

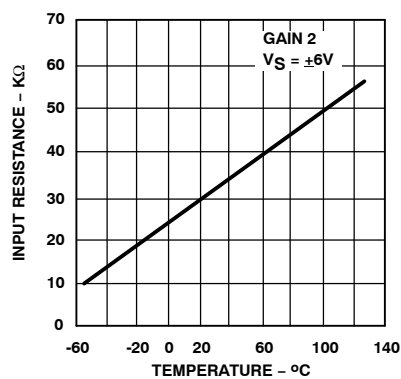


Figure 18. Input Resistance as a Function of Temperature

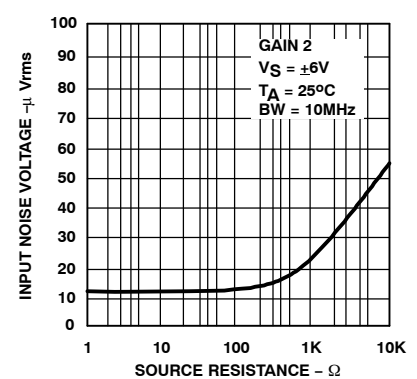


Figure 19. Input Noise Voltage as a Function of Source Resistance

TYPICAL PERFORMANCE CHARACTERISTICS

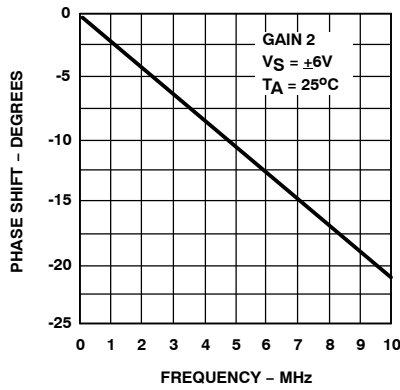


Figure 20. Phase Shift as a Function of Frequency

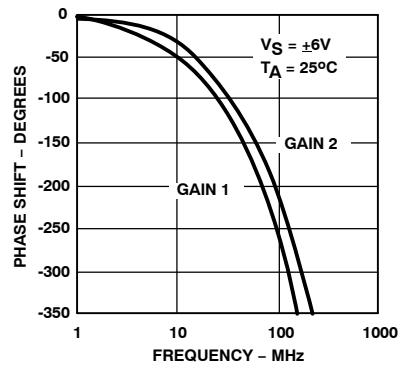


Figure 21. Phase Shift as a Function of Frequency

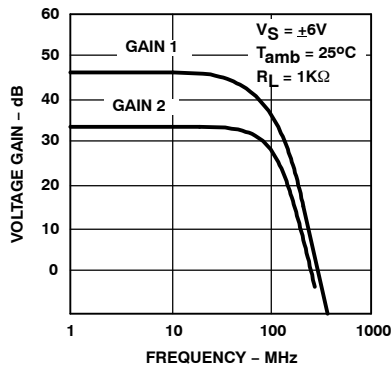


Figure 22. Voltage Gain as a Function of Frequency

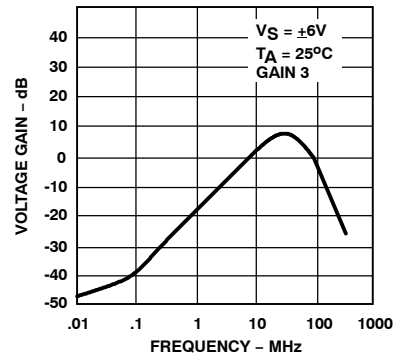


Figure 23. Voltage Gain as a Function of Frequency

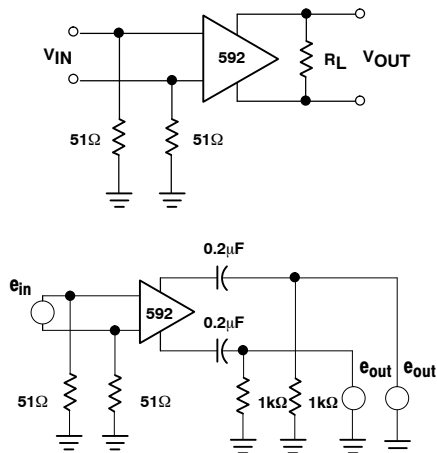
TEST CIRCUITS ($T_A = 25^\circ\text{C}$, UNLESS OTHERWISE NOTED.)

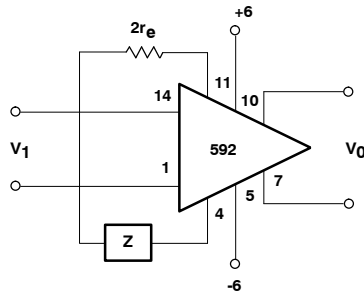
Figure 24. Test Circuits

NE592

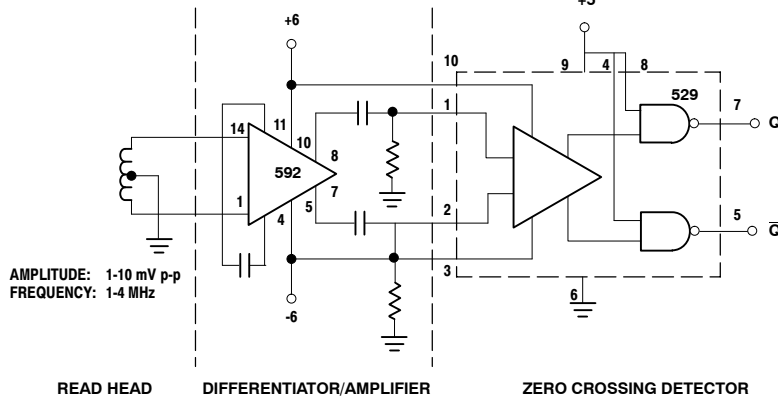
NOTE:

$$\frac{V_0(s)}{V_1(s)} \approx \frac{1.4 \cdot 10^4}{Z(s) + 2r_e}$$

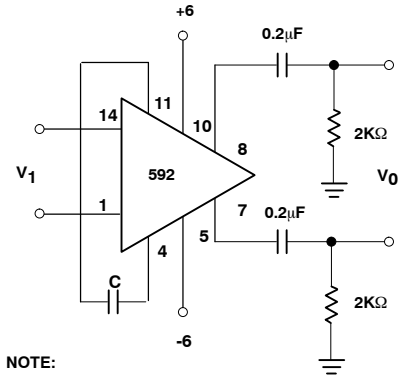
$$\approx \frac{1.4 \cdot 10^4}{Z(s) + 32}$$



Basic Configuration



Disc/Tape Phase-Modulated Readback Systems



NOTE:

For frequency $F_1 \ll 1/2 \pi (32) C$

$$V_O \approx 1.4 \times 10^4 C \frac{dV_i}{dt}$$

Differentiation with High Common-Mode Noise Rejection

Figure 25. Typical Applications

Z NETWORK	FILTER TYPE	$V_0(s)$ TRANSFER $V_1(s)$ FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L} \left[\frac{1}{s + R/L} \right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R} \left[\frac{s}{s + 1/RC} \right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L} \left[\frac{s}{s^2 + R/Ls + 1/LC} \right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R} \left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC} \right]$

NOTES:

In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω .

$S = j\Omega$

$\Omega = 2\pi f$

Figure 26. Filter Networks

NE592

ORDERING INFORMATION

Device	Temperature Range	Package	Shipping†
NE592D8R2G	0 to +70°C	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NE592D14R2G		SOIC-14 (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 6)

NE592D8G	0 to +70°C	SOIC-8 (Pb-Free)	98 Units/Rail
NE592D14G		SOIC-14 (Pb-Free)	55 Units/Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

6. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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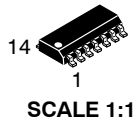
SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

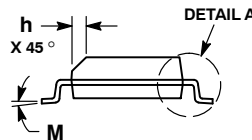
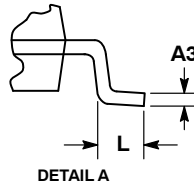
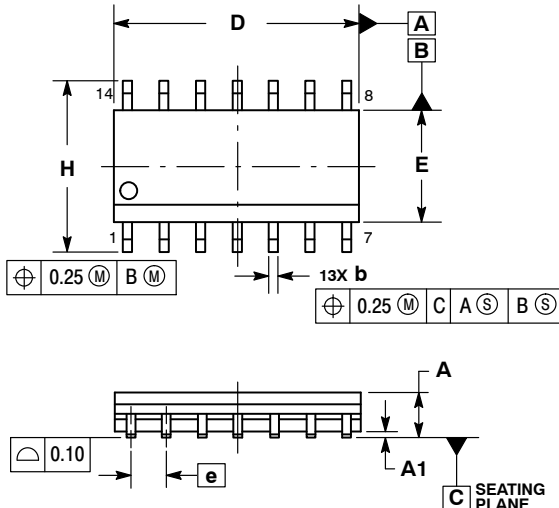
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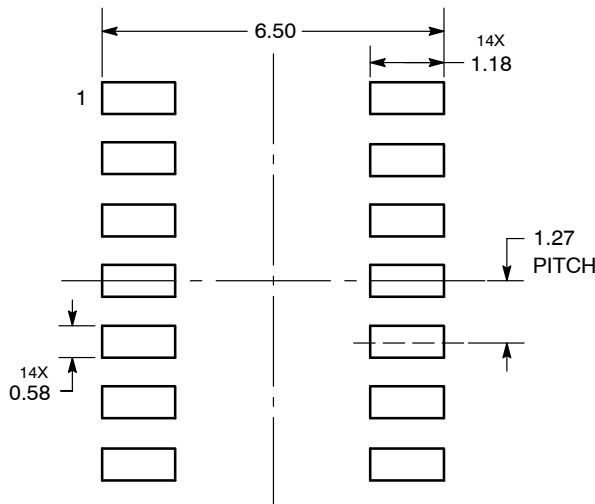


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

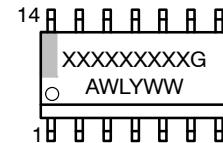
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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