

To all our customers

Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: <http://www.renesas.com>

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.

3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.

The information described here may contain technical inaccuracies or typographical errors.

Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.

Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (<http://www.renesas.com>).

4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.

HA16116FP/FPJ, HA16121FP/FPJ

Switching Regulator for Chopper Type DC/DC Converter



ADE-204-019A (Z)

Rev.1
Dec. 2000

Description

HA16116FP/FPJ and HA16121FP/FPJ are dual-channel PWM switching regulator controller ICs for use in chopper-type DC/DC converters.

This IC series incorporates totem pole gate drive circuits to allow direct driving of a power MOS FET. The output logic is preset for booster, step-down, or inverting control in a DC/DC converter. This logic assumes use of an N-channel power MOS FET for booster control, and a P-channel power MOS FET for step-down or inverting control.

HA16116 includes a built-in logic circuit for step-down control only, and one for use in both step-down and inverting control. HA16121 has a logic circuit for booster control only and one for both step-down and inverting control.

Both ICs have a pulse-by-pulse current limiter, which limits PWM pulse width per pulse as a means of protecting against overcurrent, and which uses an on/off timer for intermittent operation. Unlike conventional methods that use a latch timer for shutdown, when the pulse-by-pulse current limiter continues operation beyond the time set in the timer, the IC is made to operate intermittently (flickering operation), resulting in sharp vertical setting characteristics. When the overcurrent condition subsides, the output is automatically restored to normal.

The dual control circuits in the IC output identical triangle waveforms, for completely synchronous configuring a compact, high efficiency dual-channel DC/DC converter, with fewer external components than were necessary previously.

Functions

- 2.5 V reference voltage (Vref) regulator
- Triangle wave form oscillator
- Dual overcurrent detector
- Dual totem pole output driver
- UVL (under voltage lock out) system
- Dual error amplifier
- Vref overvoltage detector
- Dual PWM comparator

Features

- Wide operating supply voltage range* (3.9 V to 40.0 V)
- Wide operating frequency range (600 kHz maximum operation)
- Direct power MOS FET driving (output current ± 1 A peak in maximum rating)
- Pulse-by-pulse overcurrent protection circuit with intermittent operation function (When overcurrent state continues beyond time set in timer, the IC operates intermittently to prevent excessive output current.)
- Grounding the ON/OFF pin turns the IC off, saving power dissipation. (HA16116: $I_{OFF} = 10 \mu A$ max.; HA16121: $I_{OFF} = 150 \mu A$ max.)
- Built-in UVL circuit (UVL voltage can be varied with external resistance.)
- Built-in soft start and quick shutoff functions

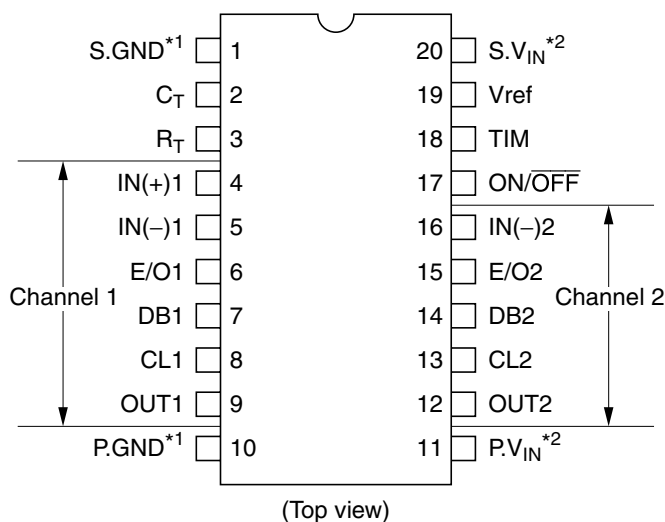
Note: The reference voltage 2.5 V is under the condition of $V_{IN} \geq 4.5$ V.

Ordering Information

Hitachi Control ICs for Chopper-Type DC/DC Converters

Channels	Product Number	Channel No.	Control Functions			Output Circuits	Overcurrent Protection
			Step-Up	Step-Down	Inverting		
Dual	HA17451	Ch 1	○	○	○	Open collector	SCP with timer (latch)
		Ch 2	○	○	○		
Single	HA16114	—	—	○	○	Totem pole power MOS FET driver	Pulse-by-pulse current limiter and intermittent operation by on/off timer
	HA16120	—	○	—	—		
Dual	HA16116	Ch 1	—	○	○		
		Ch 2	—	○	—		
	HA16121	Ch 1	—	○	○		
		Ch 2	○	—	—		

Pin Arrangement



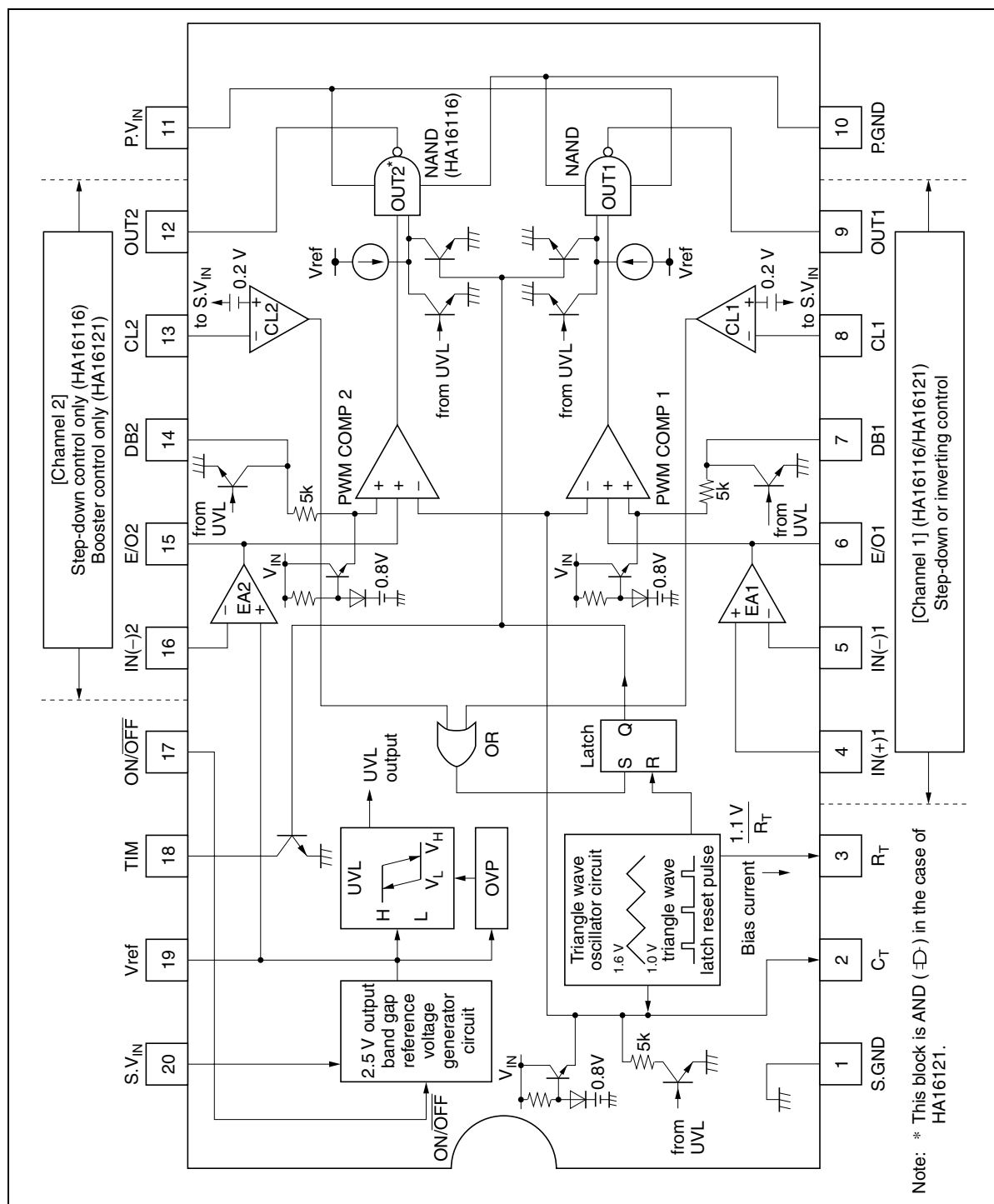
- Notes: 1. Pins S.GND (pin 1) and P.GND (pin 10) have no direct internal interconnection. Both pins must be connected to ground.
2. Pins S.V_{IN} (pin 20) and P.V_{IN} (pin 11) have no direct internal interconnection. Both pins must be connected to V_{IN}.

Pin Functions

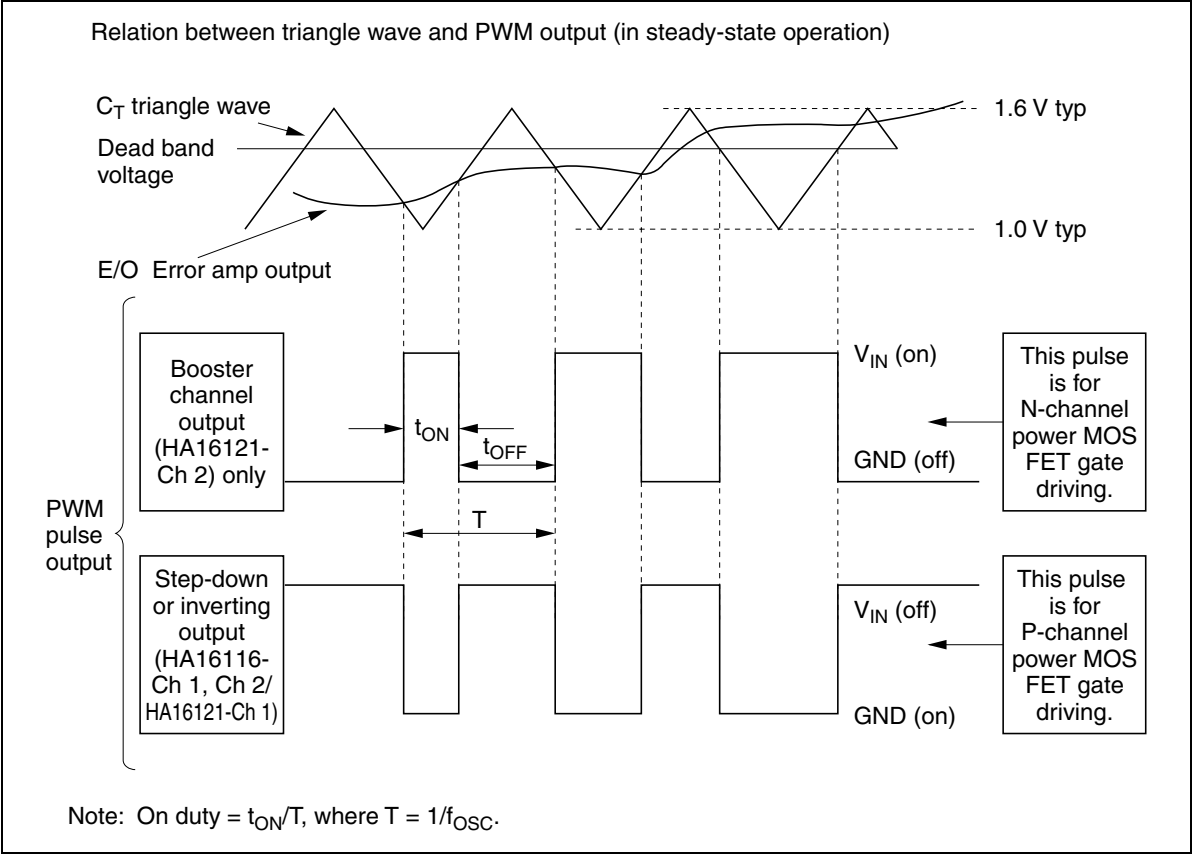
Pin No.	Symbol	Function	
1	S.GND	Signal circuitry* ¹ ground	
2	C _T	Timing capacitance (triangle wave oscillator output)	
3	R _T	Timing resistance (for bias current synchronization)	
4	IN(+) ₁	Error amp. noninverting input (1)	Channel 1
5	IN(-) ₁	Error amp. inverting input (1)	
6	E/O ₁	Error amp. output (1)	
7	DB ₁	Dead band timer off period adjustment input (1)	
8	CL ₁	Overcurrent detection input (1)	
9	OUT ₁	PWM pulse output (1)	
10	P.GND	Output stage* ¹ ground	
11	P.V _{IN}	Output stage* ¹ power supply input	
12	OUT ₂	PWM pulse output (2)	Channel 2
13	CL ₂	Overcurrent detection input (2)	
14	DB ₂	Dead band timer off period adjustment input (2)	
15	E/O ₂	Error amp. output (2)	
16	IN(-) ₂	Error amp. inverting input (2)* ²	
17	ON/OFF	IC on/off switch input (off when grounded)	
18	TIM	Setting of intermittent operation timing when overcurrent is detected (collector input of timer transistor)	
19	Vref	2.5 V reference voltage output	
20	S.V _{IN}	Signal circuitry* ¹ power supply input	

- Notes: 1. Here “output stage” refers to the power MOS FET driver circuits, and “signal circuitry” refers to all other circuits on the IC. Note that this IC is not protected against reverse insertion, which can cause breakdown of the IC between V_{IN} and GND. Be careful to insert the IC correctly.
2. Noninverting input of the channel 2 error amp is connected internally to Vref.

Block Diagram

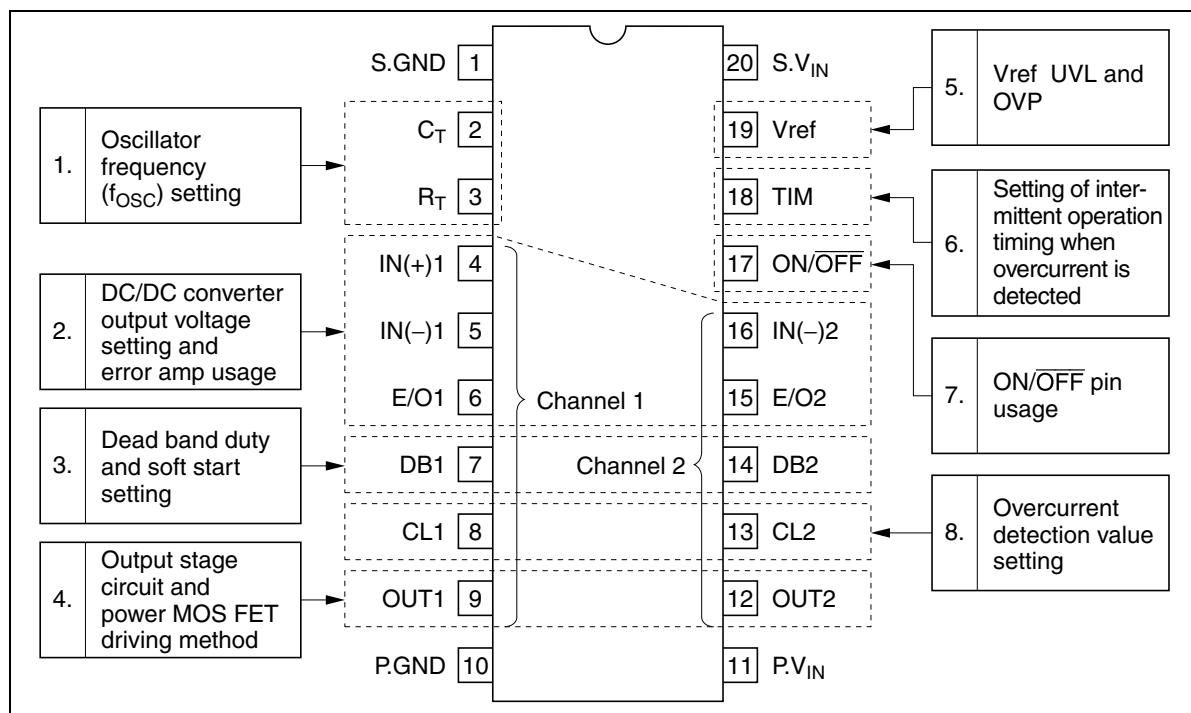


Function and Timing Chart



Determining External Component Constants (pin usage)

Constant settings are explained for the following items.



1. Oscillator Frequency (f_{osc}) Setting

Figure 1.1 shows an equivalent circuit for the triangle wave oscillator.

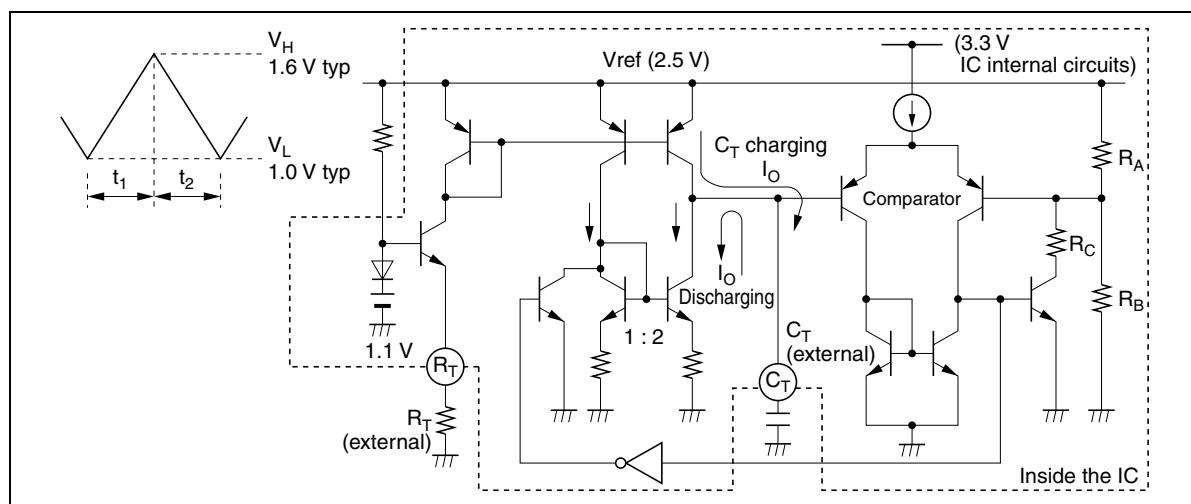


Figure 1.1 Equivalent Circuit for the Triangle Wave Oscillator

The triangle wave is a voltage waveform used as a reference in creating a PWM pulse. This block operates according to the following principles. A constant current I_o , determined by an external timing resistor R_T , is made to flow continuously to external timing capacitor C_T . When the C_T pin voltage exceeds the comparator threshold voltage V_H , the comparator output causes a switch to operate, discharging a current I_o from C_T . Next, when the C_T pin voltage drops below threshold voltage V_L , the comparator output again causes the switch to operate, stopping the I_o discharge. The triangle wave is generated by this repeated operation.

Note that $I_o = 1.1 \text{ V}/R_T$. Since the I_o current mirror circuit has a very limited current producing ability, R_T should be set to $\geq 5 \text{ k}\Omega$ ($I_o \geq 220 \text{ }\mu\text{A}$).

With this IC series, V_H and V_L of the triangle wave are fixed internally at about 1.6 V and 1.0 V by the internal resistors R_A , R_B , and R_C . The oscillator frequency can be calculated as follows.

$$f_{\text{OSC}} = \frac{1}{t_1 + t_2 + t_3}$$

Here,

$$t_1 = \frac{C_T \cdot (V_H - V_L)}{1.1 \text{ V}/R_T} = \frac{C_T R_T \cdot (V_H - V_L)}{1.1 \text{ V}}$$

$$t_2 = \frac{C_T \cdot (V_H - V_L)}{(2 - 1) \times 1.1 \text{ V}/R_T} = \frac{C_T R_T \cdot (V_H - V_L)}{1.1 \text{ V}} = t_1$$

$$V_H - V_L = 0.6 \text{ V}$$

$$t_1 = t_2 = \frac{0.6}{1.1} C_T R_T$$

$$t_3 \approx 0.8 \text{ }\mu\text{s} \text{ (comparator delay time in the oscillator)}$$

Accordingly,

$$f_{\text{OSC}} \approx \frac{1}{2t_1 + t_3} \approx \frac{1}{1.1 C_T R_T + 0.8 \text{ }\mu\text{s}} [\text{Hz}]$$

Note that the value of f_{OSC} may differ slightly from the above calculation depending on the amount of delay in the comparator circuit. Also, at high frequencies this comparator delay can cause triangle wave overshoot or undershoot, skewing the dead band threshold. Confirm the actual value in implementation and adjust the constants accordingly.

2. DC/DC Converter Output Voltage Setting and Error Amp Usage

2.1 Positive Voltage Booster ($V_o > V_{IN}$) or Step-Down ($V_{IN} > V_o > V_{ref}$)

$$\text{Use } V_o = \frac{R_1 + R_2}{R_2} \cdot V_{ref} \text{ (V)}$$

Booster output is possible only at channel 2 of HA16121. For step-down output, both channels of HA16116 or channel 1 of HA16121 are used.

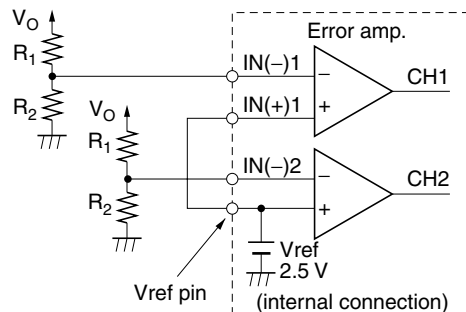


Figure 2.1

2.2 Negative Voltage ($V_o < V_{ref}$) for Inverting Output

$$\text{Use } V_o = -V_{ref} \cdot \left(\frac{R_1}{R_1 + R_2} \cdot \frac{R_3 + R_4}{R_3} - 1 \right) \text{ (V)}$$

Channel 1 is used for inverting output on both ICs.

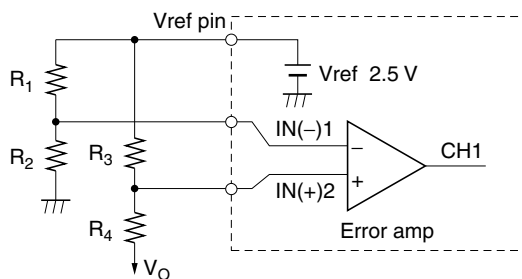


Figure 2.2 Inverting Output

2.3 Error Amplifier

Figure 2.3 shows an equivalent circuit of the error amplifier. The error amplifier on these ICs is configured of a simple NPN transistor differential input amplifier and the output circuit of a constant-current driver.

This amplifier features wide bandwidth ($f_T = 4$ MHz) with open loop gain kept to 50 dB, allowing stable feedback to be applied when the power supply is designed. Phase compensation is also easy.

Both HA16116 and HA16121 have a noninverting input (IN(+)) pin, in order to allow use of the channel 1 error amplifier for inverting control. The channel 2 error amplifier, on the other hand, is used for step-down control in HA16116 and booster control in HA16121; so the channel 2 noninverting input is connected internally to Vref.

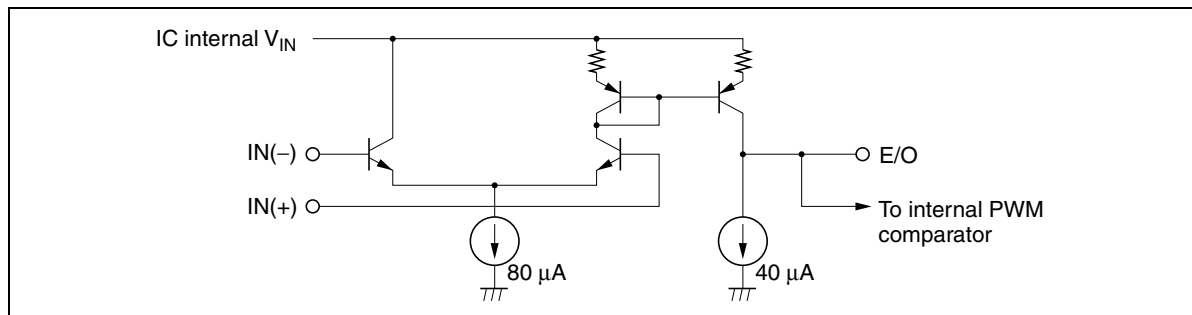


Figure 2.3 Error Amplifier Equivalent Circuit

3. Dead Band (DB) Duty and Soft Start Setting (common to both channels)

3.1 Dead Band Duty Setting

Dead band duty is set by adjusting the DB pin input voltage (V_{DB}). A convenient means of doing this is to connect two external resistors to the Vref of this IC so as to divide V_{DB} (see figure 3.1).

$$V_{DB} = V_{ref} \times \frac{R_2}{R_1 + R_2} \text{ (V)}$$

$$\text{Duty (DB)} = \frac{V_{TH} - V_{DB}}{V_{TH} - V_{TL}} \times 100 \text{ (\%)} \dots \text{ This applies when } V_{DB} > V_{TL}.$$

If $V_{DB} < V_{TL}$, there is no PWM output.

$$\text{Here, } T = \frac{1}{f_{OSC}}$$

Note: V_{TH} : 1.6 V (Typ)

V_{TL} : 1.0 V (Typ)

Vref is typically 2.5 V. Select R_1 and R_2 so that $1.0 \text{ V} \leq V_{DB} \leq 1.6 \text{ V}$.

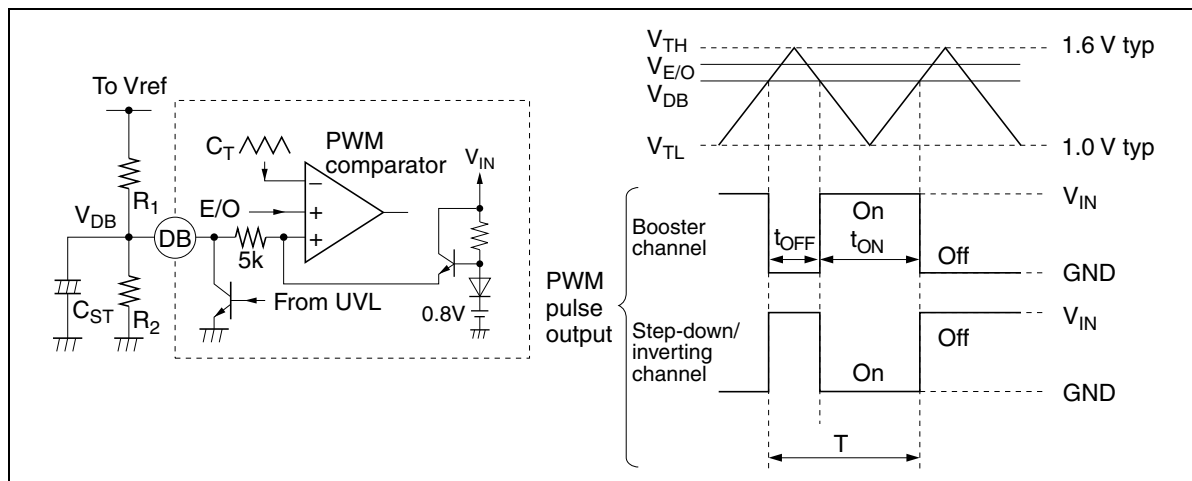


Figure 3.1 Dead Band Duty Setting

3.2 Soft Start (SST) Setting (each channel)

When the power is turned on, the soft start function gradually raises V_{DB} (refer to section 3.1), and the PWM output pulse width gradually widens. This function is realized by adding a capacitor C_{ST} to the DB pin. The function is realized as follows.

In the figure 3.2, the DB pin is clamped internally at approximately 0.8 V, which is 0.2 V lower than the triangle wave $V_{TL} = 1.0$ V typ.

t_A : Standby time until PWM pulse starts widening.

t_B : Time during which SST is in effect.

During soft start, the DB pin voltage in the figure below is as expressed in the following equation.

$$V_{SST} = V_{DB} \cdot \left(1 - e^{\frac{-t - t_{0.8}}{T}} \right), \quad t_{SST} = t_A + t_B$$

Here,

$$t_{0.8} = -T \ln \left(1 - \frac{0.8}{V_{DB}} \right), \quad T = C_{ST} \cdot (R_1 // R_2)$$

How to select values: If the soft start time t_{SST} is too short, the DC/DC converter output voltage will tend to overshoot. To prevent this, set t_{SST} to a few tens of ms or above.

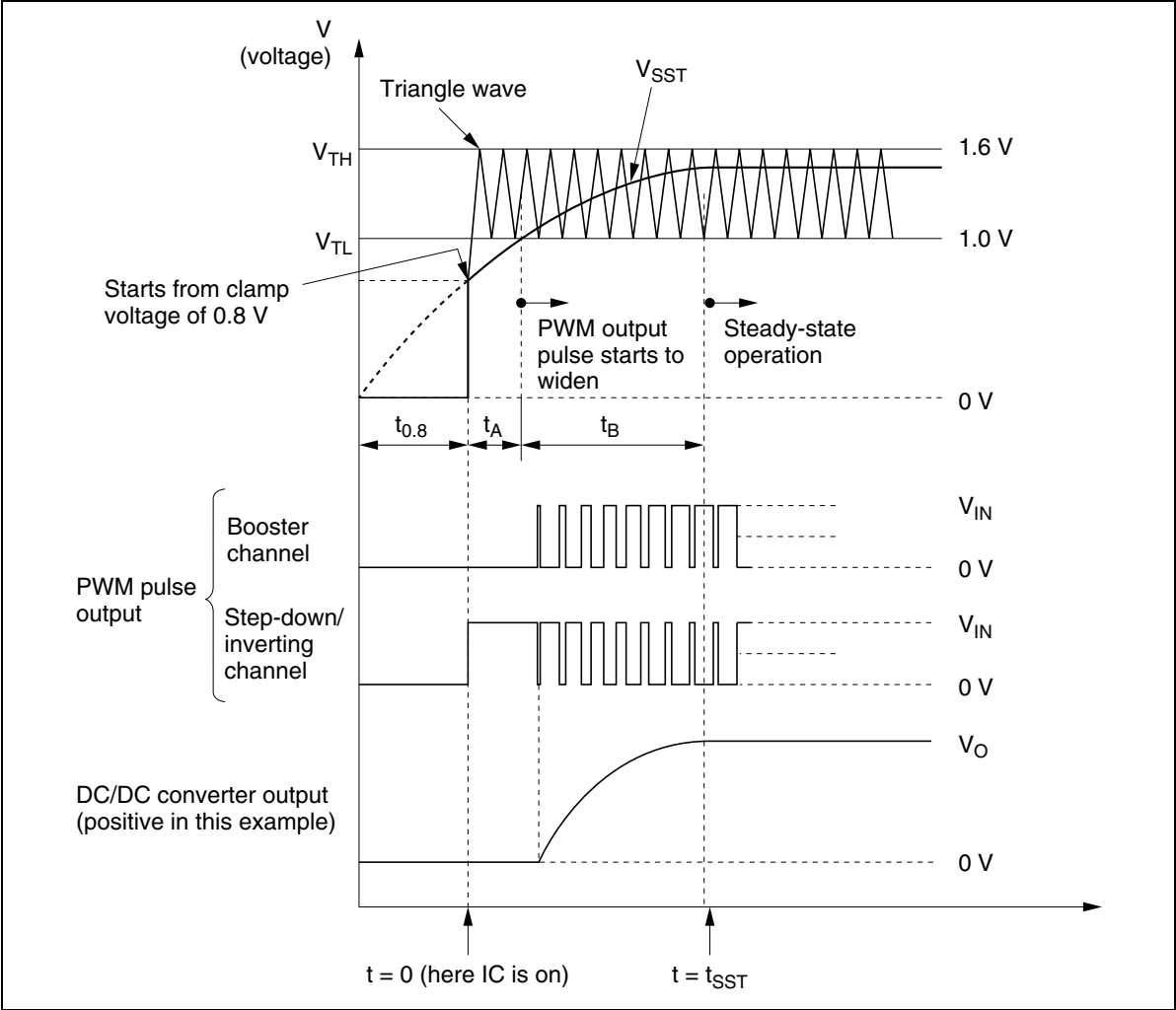


Figure 3.2 Soft Start (SST) Setting

4. Totem Pole Output Stage Circuit and Power MOS FET Driving Method

The output stage of this IC series is configured of totem pole circuits, allowing direct connection to a power MOS FET as an external switching device, so long as V_{IN} is below the gate breakdown voltage.

If there is a possibility that V_{IN} will exceed the gate breakdown voltage of the power MOS FET, a Zener diode circuit like that shown figure 4.1 or other protective measures should be used. The figure 4.1 shows an example using a P-channel power MOS FET.

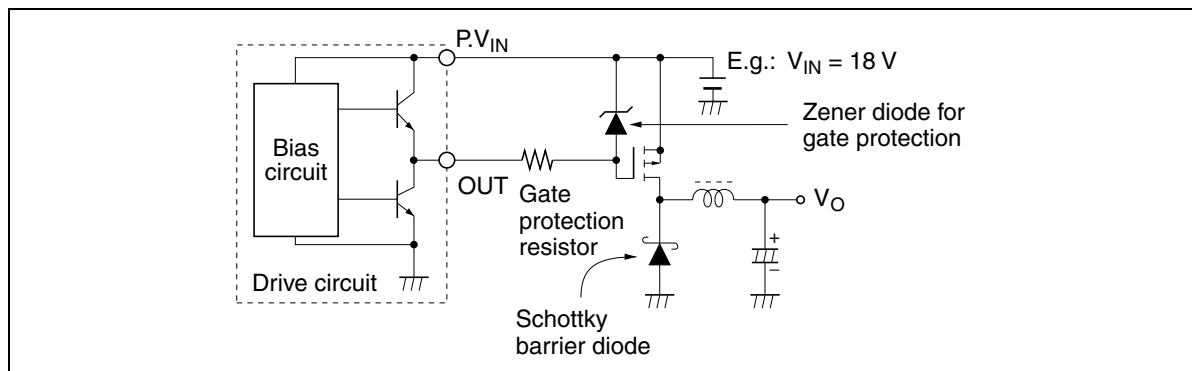


Figure 4.1 P-channel Power MOS FET (example)

5. Vref Undervoltage Error Prevention (UVL) and Overvoltage Protection (OVP) Functions

5.1 Operation Principles

The reference voltage circuit is equipped with UVL and OVP functions.

- UVL

In normal operation the Vref output voltage is fixed at 2.5 V. If V_{IN} is lower than normal, the UVL circuit detects the Vref output voltage with a hysteresis of 1.7 V and 2.0 V, and shuts off the PWM output if Vref falls below this level, in order to prevent malfunction.

- OVP

The OVP circuit protects the IC from inadvertent application of a high voltage from outside, such as if V_{IN} is shorted. A Zener diode (5.6 V) and resistor are used between Vref and GND for overvoltage detection. PWM output is shut off if Vref exceeds approximately 7.0 V.

Note that the PWM output pulse logic and the precision of the switching regulator output voltage are not guaranteed at an applied voltage of 2.5 V to 7 V.

5.2 Quick Shutoff

When the UVL circuit goes into operation, a sink transistor is switched on as in the figure below, drawing off the excess current. This transistor also functions when the IC is turned off, drawing off current from the C_T , E/O, and DB pins and enabling quick shutoff.

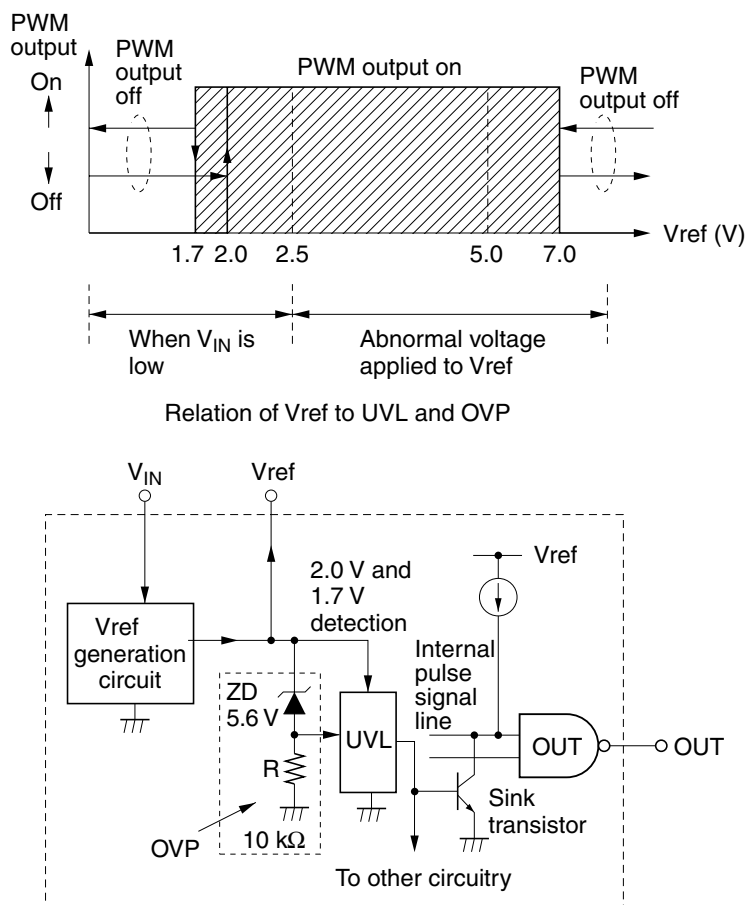


Figure 5.1 Quick Shutoff

6. Setting of Intermittent Operation Timing when Overcurrent is Detected

6.1 Operation Principles

The current limiter on this IC detects overcurrent in each output pulse, providing pulse-by-pulse overcurrent protection by limiting pulse output whenever an overcurrent is detected. If the overcurrent state continues, the TIM pin and ON/OFF pin can be used to operate the IC intermittently. As a result, a power supply with sharp vertical characteristics can be configured.

The ON/OFF timing for intermittent operation makes use of the hysteresis in the ON/OFF pin threshold voltage V_{ON} and V_{OFF} , such that $V_{ON} - V_{OFF} = V_{BE}$. Setting method is performed as described on the following pages. V_{BE} is based-emitter voltage of internal transistor.

Note: When an overcurrent is detected in one channel of this IC but not the other, the pulse-by-pulse current limiter still goes into operation on both channels. Also, when the intermittent operation feature is not used, the TIM pin should be set to open state and the ON/OFF pin pulled up to high level (above V_{ON}).

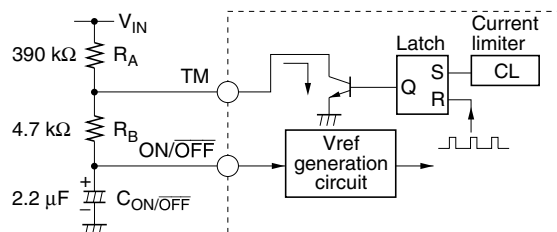
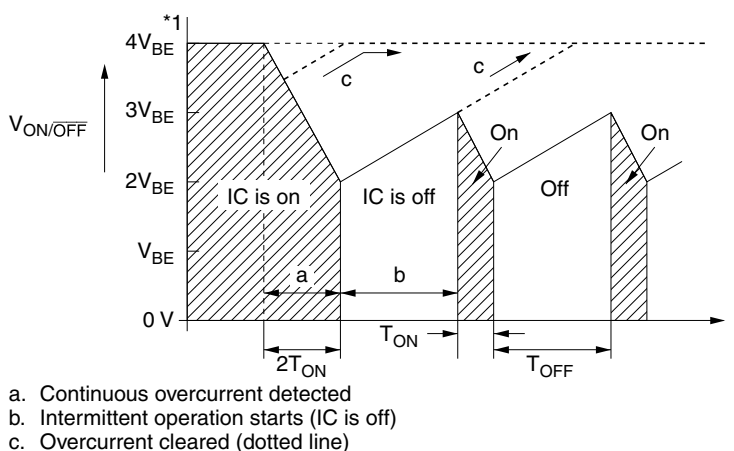


Figure 6.1 Connection Diagram (example)

6.2 Intermittent Operation Timing Chart ($V_{ON/OFF}$ only)



Note: 1. V_{BE} is the base-emitter voltage in transistors on the IC, and is approximately 0.7 V (see the figure 7.1).

For details, see the overall waveform timing diagram.

Figure 6.2 Intermittent Operation Timing Chart

6.3 Calculating Intermittent Operation Timing

Intermittent operation timing is calculated as follows.

(1) T_{ON} time (the time until the IC is shut off when continuous overcurrent occurs)

$$T_{ON} = C_{ON/OFF} \times R_B \times \ln \left(\frac{3V_{BE}}{2V_{BE}} \right) \times \left(\frac{1}{1 - \text{On duty}^*} \right)$$

$$= C_{ON/OFF} \times R_B \times \ln 1.5 \times \left(\frac{1}{1 - \text{On duty}^*} \right) \approx 0.4 \times C_{ON/OFF} \times R_B \times \left(\frac{1}{1 - \text{On duty}^*} \right)$$

(2) T_{OFF} time (when the IC is off, the time until it next goes on)

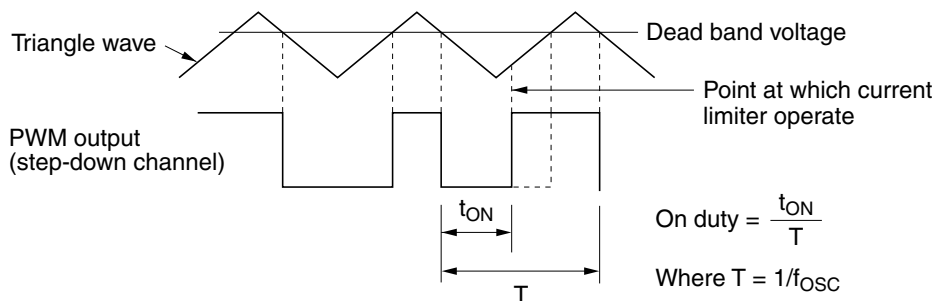
$$T_{OFF} = C_{ON/OFF} \times (R_A + R_B) \times \ln \left(\frac{V_{IN} - 2V_{BE}}{V_{IN} - 3V_{BE}} \right)$$

Where, $V_{BE} \approx 0.7 \text{ V}$

Note: 1. On duty is the percent of time the IC is on during one PWM cycle when the pulse-by-pulse current limiter is operating.

From the first equation (1) above, it is seen that the shorter the time T_{ON} when the pulse-by-pulse current limiter goes into effect (resulting in a larger overload), the smaller the value T_{ON} becomes.

As seen in the second equation (2), T_{OFF} is a function of V_{IN} . Further, according to this setting, when V_{IN} is switched on, the IC goes on only after T_{OFF} has elapsed.



Note: On duty is the percent of time the IC is on during one PWM cycle when the pulse-by-pulse current limiter is operating.

Figure 6.3

6.4 Examples of Intermittent Operation Timing (calculated values)

(1) T_{ON}

$$T_{ON} = T_1 \times C_{ON/\overline{OFF}} \times R_B$$

Here, coefficient

$$T_1 = 0.4 \times \frac{1}{1 - \text{On duty}}$$

from section 6.3 (1) previously.

Example: If $C_{ON/\overline{OFF}} = 2.2 \mu\text{F}$,
 $R_B = 4.7 \text{ k}\Omega$, and the on duty
of the current limiter is 75%,
then $T_{ON} = 16 \text{ ms}$.

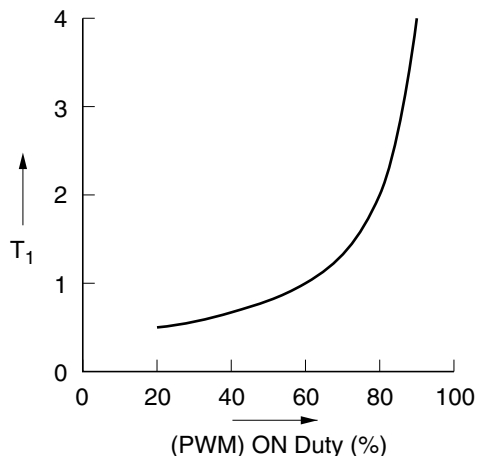


Figure 6.4 Examples of Intermittent Operation Timing (1)

(2) T_{OFF}

$$T_{OFF} = T_2 \times C_{ON/\overline{OFF}} \times (R_A + R_B)$$

Here, coefficient

$$T_2 = \ln \frac{V_{IN} - 2V_{BE}}{V_{IN} - 3V_{BE}}$$

from section 6.3 (2) previously.

Example: If $C_{ON/\overline{OFF}} = 2.2 \mu\text{F}$, $R_B = 4.7 \text{ k}\Omega$,
 $R_A = 390 \text{ k}\Omega$, $V_{IN} = 12 \text{ V}$,
then $T_{OFF} = 60 \text{ ms}$.

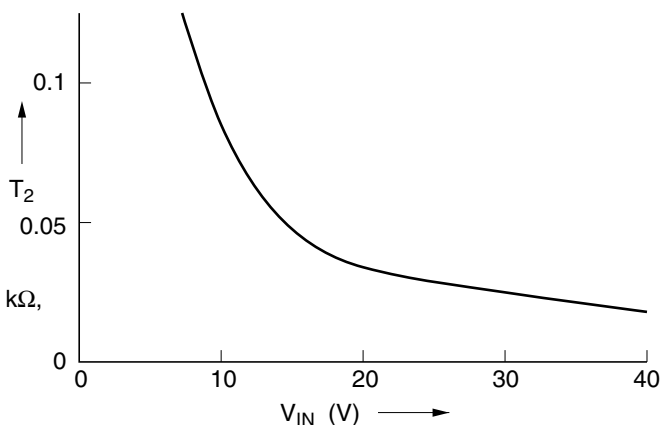


Figure 6.5 Examples of Intermittent Operation Timing (2)

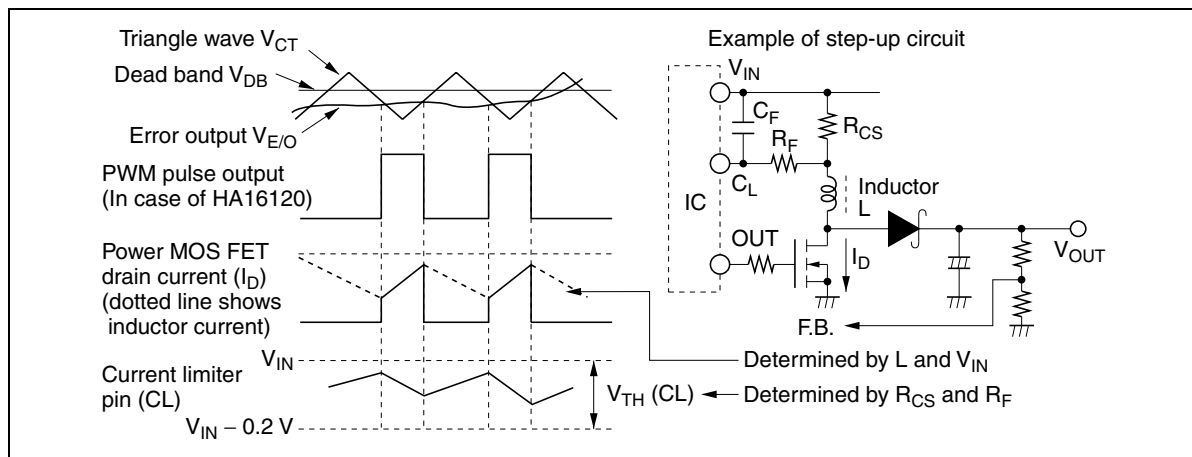


Figure 6.6

7. ON/OFF Pin Usage

7.1 IC Shutoff by the ON/OFF Pin

As shown in the figure 7.1, these ICs can be turned off safely by lowering the voltage at the ON/OFF pin to below $2V_{BE}$. This feature is used to conserve the power in the power supply system. In off state the IC current consumption (I_{OFF}) is 10 μA (Max) for HA16116 and 150 μA (Max) for HA16121.

The ON/OFF pin can also be used to drive logic ICs such as TTL or CMOS with a sink current of 50 μA (Typ) at an applied voltage of 5 V. When it is desired to employ this feature along with intermittent operation, an open collector or open drain logic IC should be used.

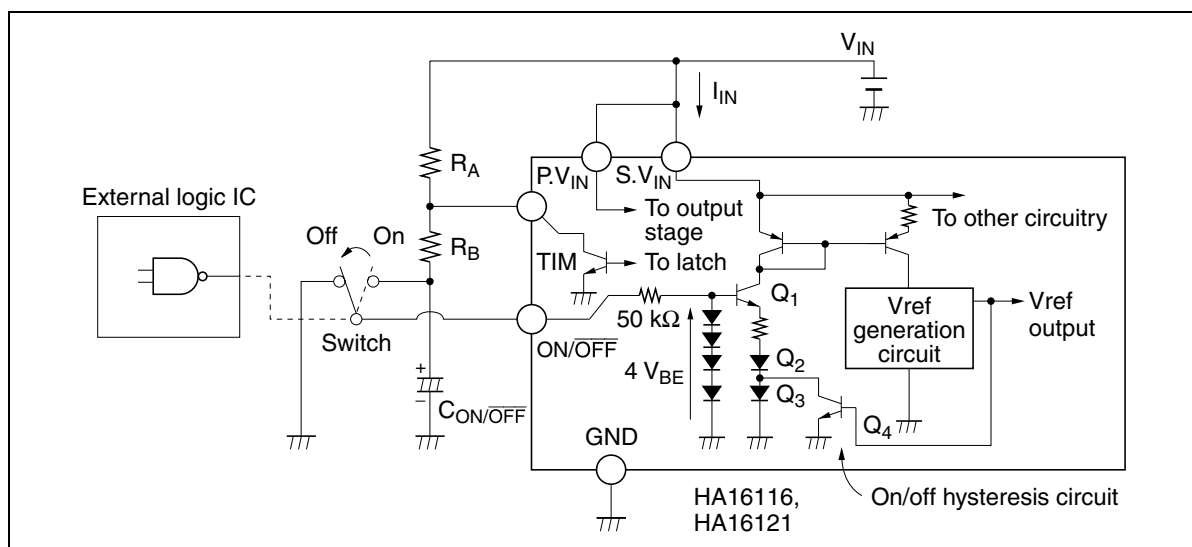


Figure 7.1 IC Shutoff by the ON/OFF Pin

7.2 Adjusting UVL Voltage (when intermittent operation is not used)

The UVL voltage setting in this IC series can be adjusted externally as shown below.

Using the relationships shown in the figure, the UVL voltage in relation to V_{IN} can be adjusted by changing the relative values of V_{TH} and V_{TL} .

When the IC is operating, transistor Q_4 is off, so $V_{ON} = 3V_{BE} \approx 2.1$ V. Accordingly, by connecting resistors R_C and R_D , the voltage at which UVL is cancelled is as follows.

$$V_{IN} = 2.1 \text{ V} \times \frac{R_C + R_D}{R_D}$$

This V_{IN} is simply the supply voltage at which the UVL stops functioning, so in this state V_{ref} is still below 2.5 V. In order to restore V_{ref} to 2.5 V, a V_{IN} of approximately 4.3 V should be applied.

With this IC series, $V_{ON/OFF}$ makes use of the V_{BE} of internal transistors, so when designing a power supply system it should be noted that V_{ON} has a temperature dependency of around $-6 \text{ mV}/^\circ\text{C}$.

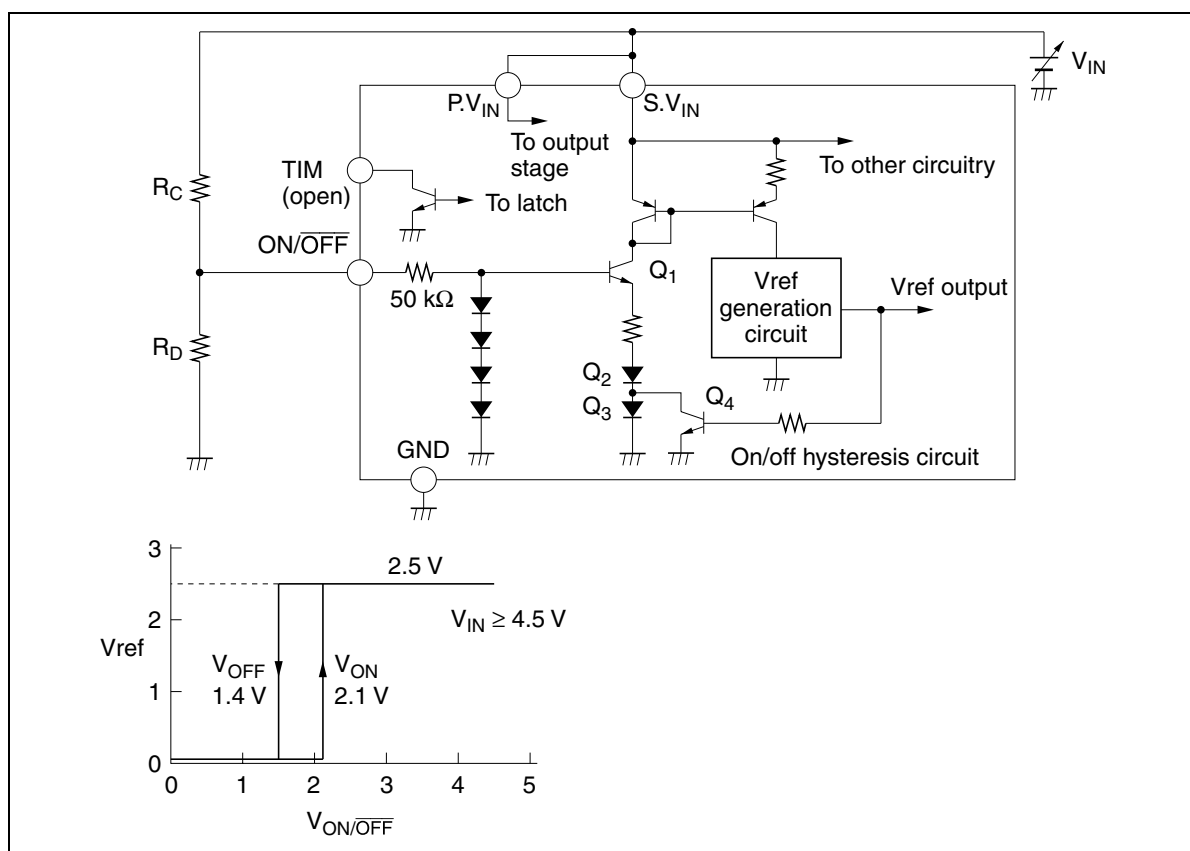


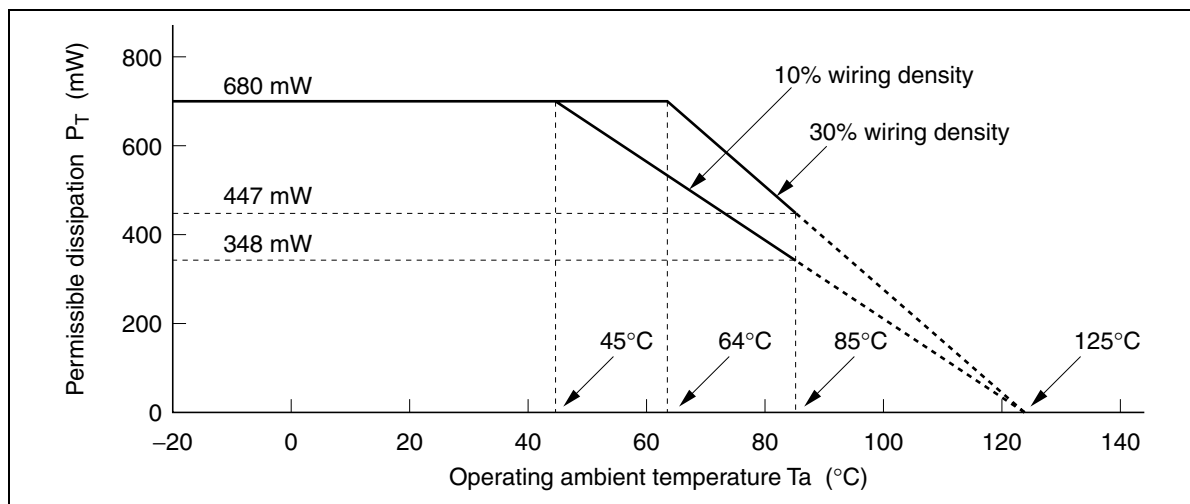
Figure 7.2 Adjusting UVL Voltage

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating		Unit
		HA16116FP, HA16121FP	HA16116FPJ, HA16121FPJ	
Supply voltage	V_{IN}	40	40	V
Output current (DC)	I_O	±0.1	±0.1	A
Output current (peak)	$I_{O \text{ peak}}$	±1.0	±1.0	A
Current limiter pin voltage	V_{CL}	V_{IN}	V_{IN}	V
Error amp input voltage	V_{IEA}	V_{IN}	V_{IN}	V
E/O input voltage	$V_{IE/O}$	Vref	Vref	V
RT pin source current	I_{RT}	500	500	μA
TIM pin sink current	I_{TM}	20	20	mA
Power dissipation*1	P_T	680*1,*2	680*1,*2	mW
Operation temperature range	Topr	−20 to +85	−40 to +85	°C
Junction temperature	TjMax	125	125	°C
Storage temperature range	Tstg	−55 to +125	−55 to +125	°C

- Note: 1. This value is based on actual measurements on a 40 × 40 × 1.6 mm glass epoxy circuit board. At a wiring density of 10%, it is the permissible value up to Ta = 45°C, but at higher temperatures this value should be derated by 8.3 mW/°C. At a wiring density of 30% it is the permissible value up to Ta = 64°C, but at higher temperatures it should be derated by 11.1 mW/°C.
2. For the DILP package.
This value applies up to Ta = 45°C; at temperatures above this, 8.3 mW/°C derating should be applied.



Electrical Characteristics

(Ta = 25°C, V_{IN} = 12 V, f_{OSC} = 300 kHz)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Reference voltage block	Output voltage	V _{ref}	2.45	2.50	2.55	V	I _O = 1 mA
	Line regulation	Line	—	30	60	mV	4.5 V ≤ V _{IN} ≤ 40 V
	Load regulation	Load	—	30	60	mV	0 ≤ I _O ≤ 10 mA
	Output shorting current	I _{OS}	10	25	—	mA	V _{ref} = 0 V
	V _{ref} OVP voltage	V _{rovp}	6.2	6.8	7.0	V	
	Output voltage temperature dependence	ΔV _{ref} /ΔTa	—	100	—	ppm/°C	
Triangle wave oscillator block	Maximum oscillator frequency	f _{OSCmax}	600	—	—	kHz	
	Minimum oscillator frequency	f _{OSCmin}	—	—	1	Hz	
	Oscillator frequency input voltage stability	Δf _{OSC} /ΔV _{IN}	—	±1	±3	%	4.5 V ≤ V _{IN} ≤ 40 V
	Oscillator frequency temperature stability	Δf _{OSC} /ΔTa	—	±5	—	%	−20°C ≤ Ta ≤ 85°C
	Oscillator frequency	f _{OSC}	270	300	330	kHz	C _T = 220 pF, R _T = 10 kΩ)
Dead band adjust block	Low-level threshold voltage	V _{TLDB}	0.87	0.97	1.07	V	Output on duty 0%
	High-level threshold voltage	V _{THDB}	1.48	1.65	1.82	V	Output on duty 100%
	Threshold differential voltage	ΔV _{TDB}	0.55	0.65	0.75	V	ΔV _{TH} = V _{TH} − V _{TL}
	Output source current	I _{Osource (DB)}	100	150	200	μA	DB pin = 0 V
PWM comparator block	Low-level threshold voltage	V _{TLCMP}	0.87	0.97	1.07	V	Output on duty = 0%
	High-level threshold voltage	V _{THCMP}	1.48	1.65	1.82	V	Output on duty = 100%
	Threshold differential voltage	ΔV _{TCMP}	0.55	0.65	0.75	V	ΔV _{TH} = V _{TH} − V _{TL}
	Dead band precision	DBdev	−5	0	+5	%	Deviation when V _{EO} = (V _{TL} + V _{TH})/2, duty = 50 %

Electrical Characteristics (cont.)

(Ta = 25°C, V_{IN} = 12 V, f_{OSC} = 300 kHz)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Error amp block	Input offset voltage	V _{IOEA}	—	2	10	mV	
	Input bias current	I _{BEA}	—	0.8	2	μA	
	Output sink current	I _{Osink (EA)}	28	40	52	μA	In open loop, V _I = 3 V, V _O = 2 V
	Output source current	I _{Osource (EA)}	28	40	52	μA	In open loop, V _I = 2 V, V _O = 1 V
	Voltage gain	A _V	40	50	—	dB	f = 10 kHz
	Unity gain band-width	BW	3	4	—	MHz	
	High-level output voltage	V _{OHEA}	2.2	3.0	—	V	I _O = 10 μA
	Low-level output voltage	V _{OLEA}	—	0.2	0.5	V	I _O = 10 μA
Overcurrent detection block	Threshold voltage	V _{TCL}	V _{IN} −0.22	V _{IN} −0.2	V _{IN} −0.18	V	
	CL bias current	I _{BCL}	150	200	250	μA	C _L = V _{IN}
	Operating time	t _{OFFCL}	—	200	300	ns	C _L = V _{IN} −0.3 V
			—	500	600	ns	Applies only to ch 2 of HA16121
Output stage	Output low voltage	V _{OL1}	—	0.7	2.2	V	I _{Osink} = 10 mA Applies only to HA16116
			—	1.6	1.9	V	I _{Osink} = 10 mA Applies only to HA16121
			—	1.0	1.3	V	I _{Osink} = 0 mA Applies only to HA16121
	Off state low voltage	V _{OL2}	—	1.6	1.9	V	I _{Osink} = 1 mA ON/OFF pin = 0 V Applies only to ch 2 of HA16121
			—	1.0	1.3	V	I _{Osink} = 0 mA ON/OFF = 0 V Applies only to ch 2 of HA16121
	Output high voltage	V _{OH1}	V _{IN} −1.9	V _{IN} −1.6	—	V	I _{Osource} = 10 mA
			V _{IN} −1.3	V _{IN} −1.0	—	V	I _{Osource} = 0 A
	Off state high voltage	V _{OH2}	V _{IN} −1.9	V _{IN} −1.6	—	V	I _{Osource} = 1 mA ON/OFF pin = 0 V
			V _{IN} −1.3	V _{IN} −1.0	—	V	I _{Osource} = 0 A ON/OFF pin = 0 V
	Rise time	t _r	—	70	130	ns	C _L = 1000 pF (to V _{IN}) *1, *2
	Fall time	t _f	—	70	130	ns	C _L = 1000 pF (to V _{IN}) *1, *2

Electrical Characteristics (cont.)

(Ta = 25°C, V_{IN} = 12 V, f_{OSC} = 300 kHz)

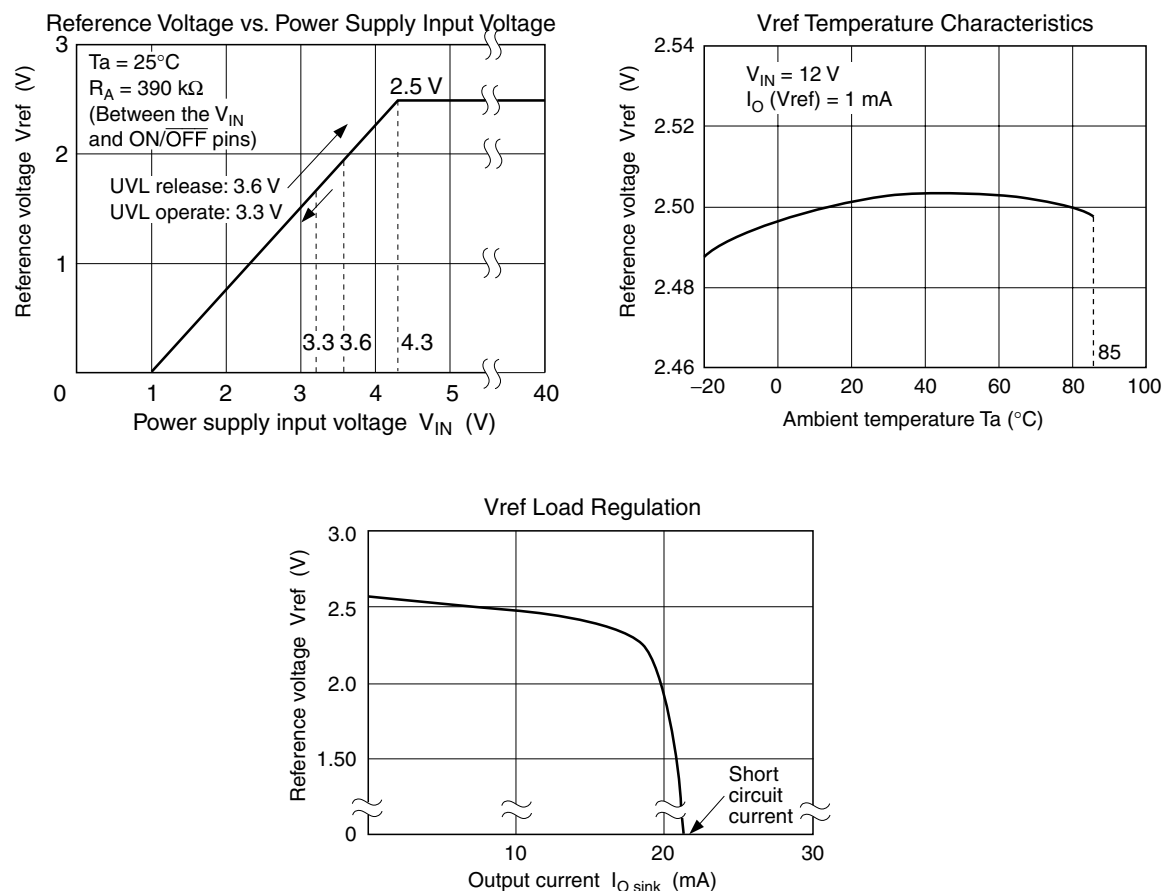
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
UVL block	V _{IN} high-level threshold voltage	V _{TUH1}	3.3	3.6	3.9	V	
	V _{IN} low-level threshold voltage	V _{TUL1}	3.0	3.3	3.6	V	
	V _{IN} threshold differential voltage	ΔV _{TU1}	0.1	0.3	0.5	V	ΔV _{TU1} = V _{TUH1} – V _{TUL1}
	Vref high-level threshold voltage	V _{TUH2}	1.7	2.0	2.3	V	
	Vref low-level threshold voltage	V _{TUL2}	1.4	1.7	2.0	V	
	Vref threshold differential voltage	ΔV _{TU2}	0.1	0.3	0.5	V	ΔV _{TU2} = V _{TUH2} – V _{TUL2}
ON/OFF block	ON/OFF pin sink current	I _{ON/OFF}	—	35	50	μA	ON/OFF pin = 5 V
	IC on-state voltage	V _{ON}	1.8	2.1	2.4	V	
	IC off-state voltage	V _{OFF}	1.1	1.4	1.7	V	
	ON/OFF threshold differential voltage	ΔV _{ON/OFF}	0.5	0.7	0.9	V	
TIM block	TIM pin sink current in steady state	I _{TIM1}	0	—	10	μA	CL pin = V _{IN} , V _{TIM} = 0.3 V
	TIM pin sink current at overcurrent detection	I _{TIM2}	10	15	20	mA	CL pin = V _{IN} – 0.3 V V _{TIM} = 0.3 V
Common block	Operating current	I _{IN}	6.0	8.5	11.1	mA	C _L = 0 pF (to V _{IN}) *1, *2
			8.5	12.1	15.7	mA	C _L = 500 pF (to V _{IN}) *1, *2
			11.0	15.7	20.5	mA	C _L = 1000 pF (to V _{IN}) *1, *2
	Off current	I _{OFF}	0	—	10	μA	HA16116FP ON/OFF
			0	120	150	μA	HA16121FP pin = 0 V

Notes: 1. C_L is load capacitor for Power MOS FET's gate, and C_L = 1000 pF to GND in the case of HA16121 – ch 2.

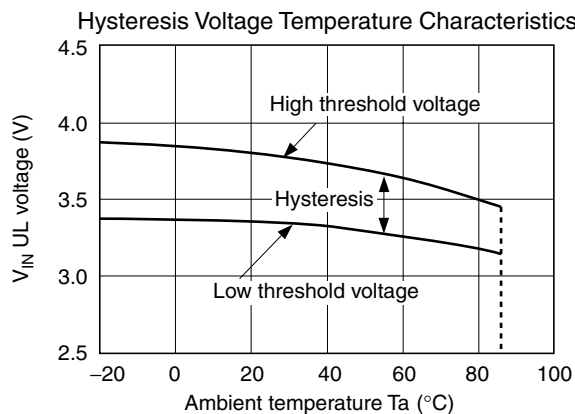
2. C_L in channel 2 of HA16121 is connected to GND.

Characteristic Curves

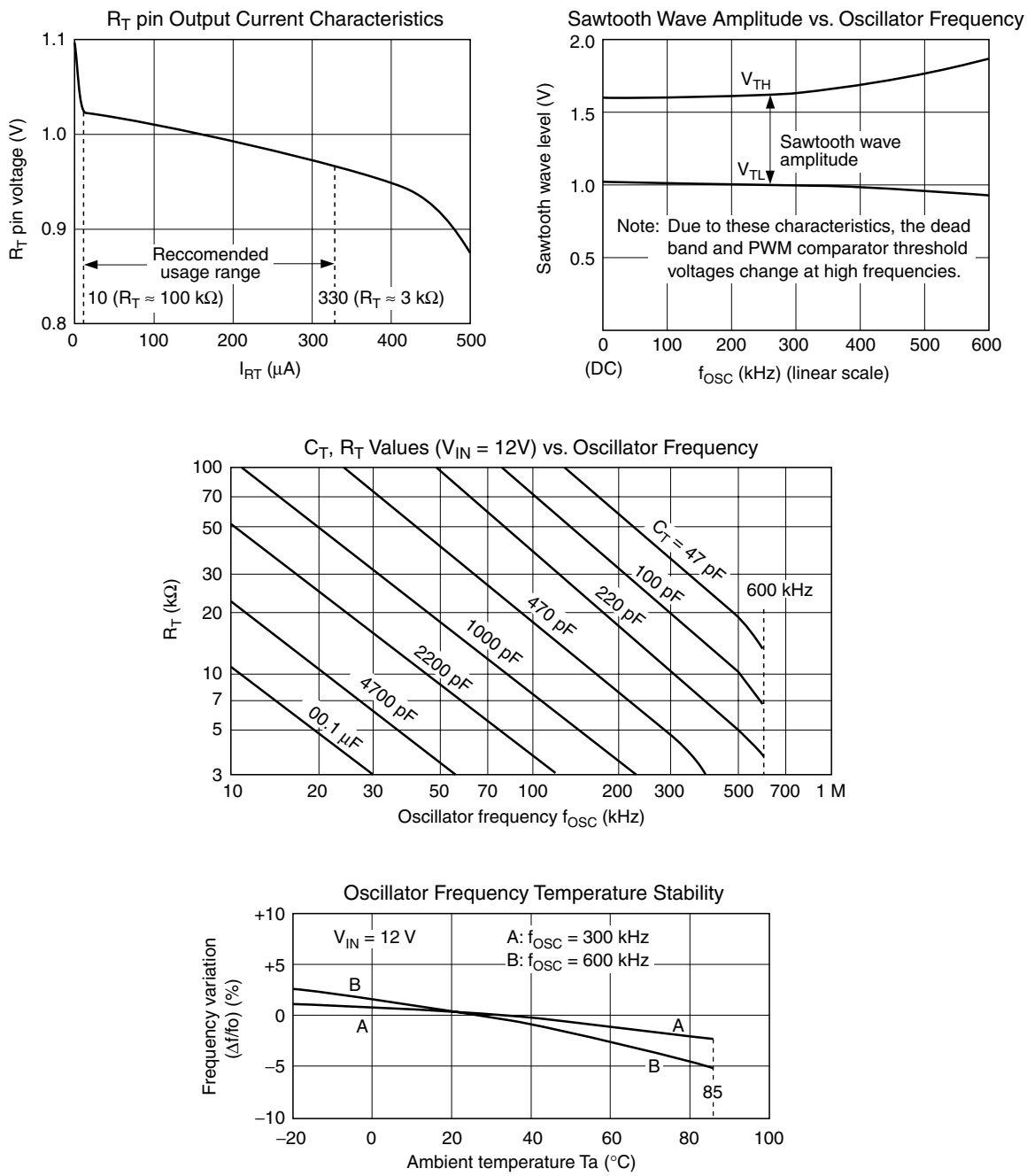
- Reference Voltage Block (Vref)



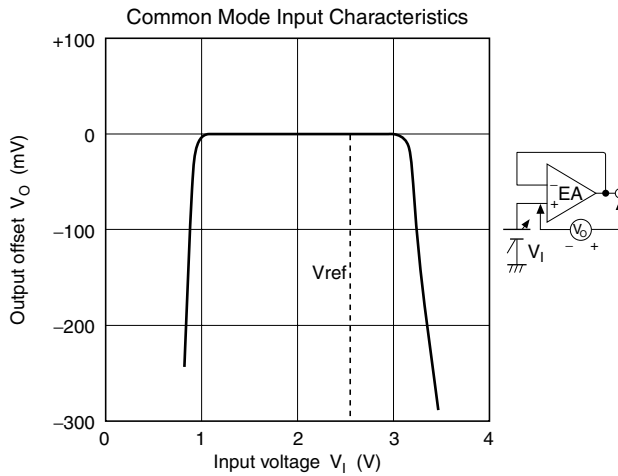
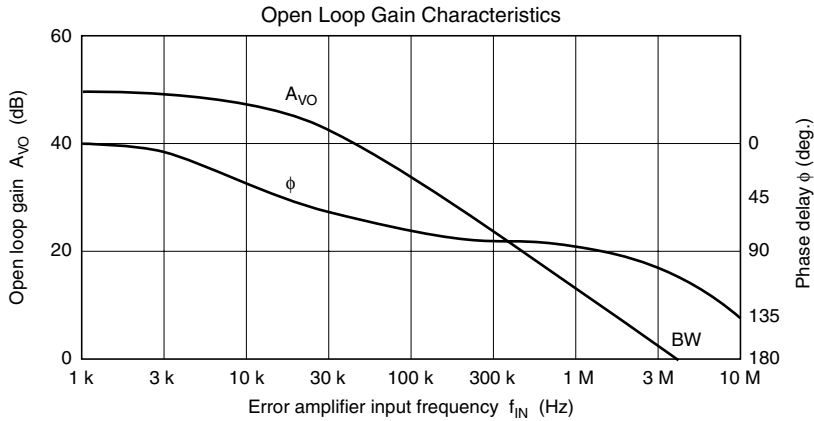
- UVL (Low Input Voltage Malfunction Prevention) Block



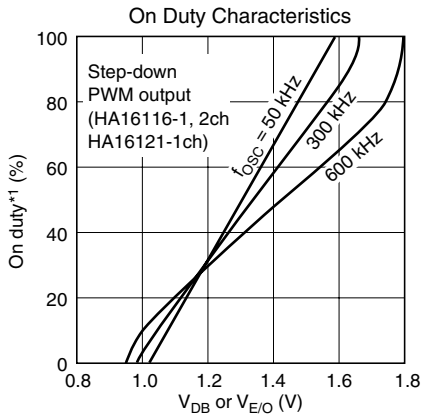
• Triangle Wave Oscillator Block



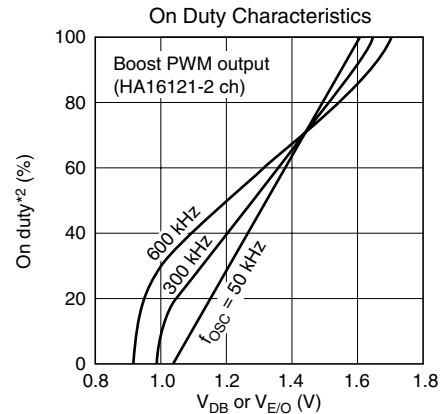
- Error Amplifier Block



- On Duty Characteristics

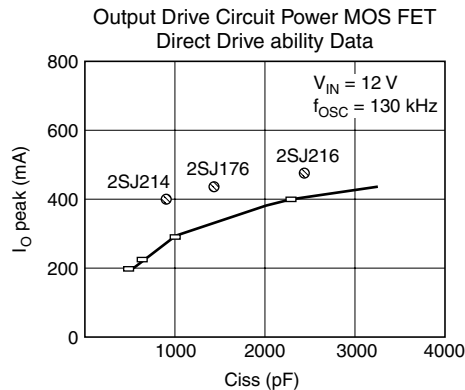
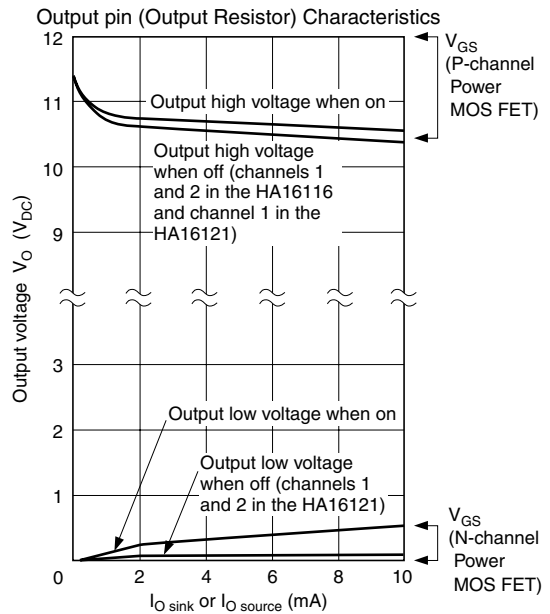
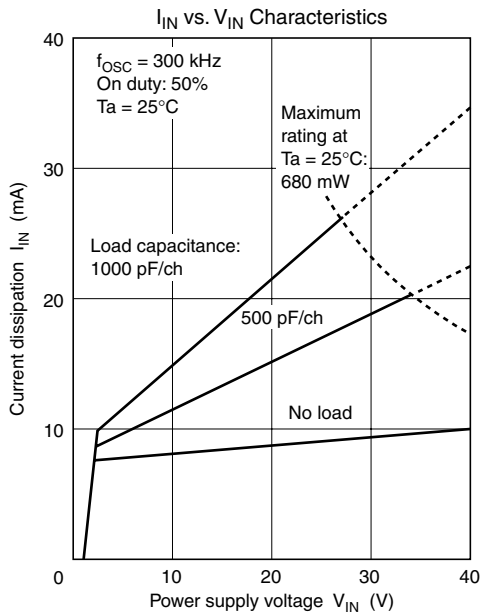
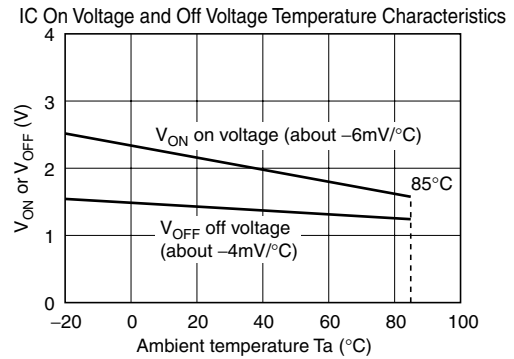
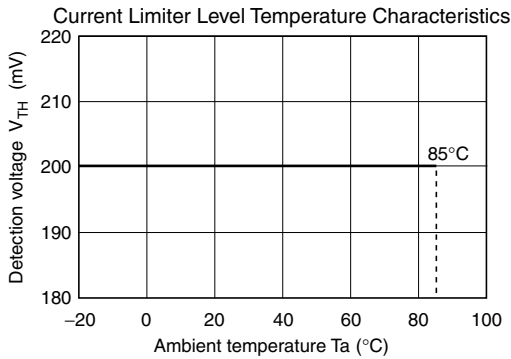


Notes: 1. The percentage of a single timing cycle during which the output is low.

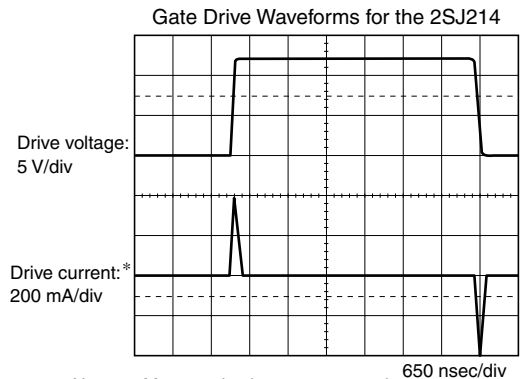


2. The percentage of a single timing cycle during which the output is high.

• Other Characteristics



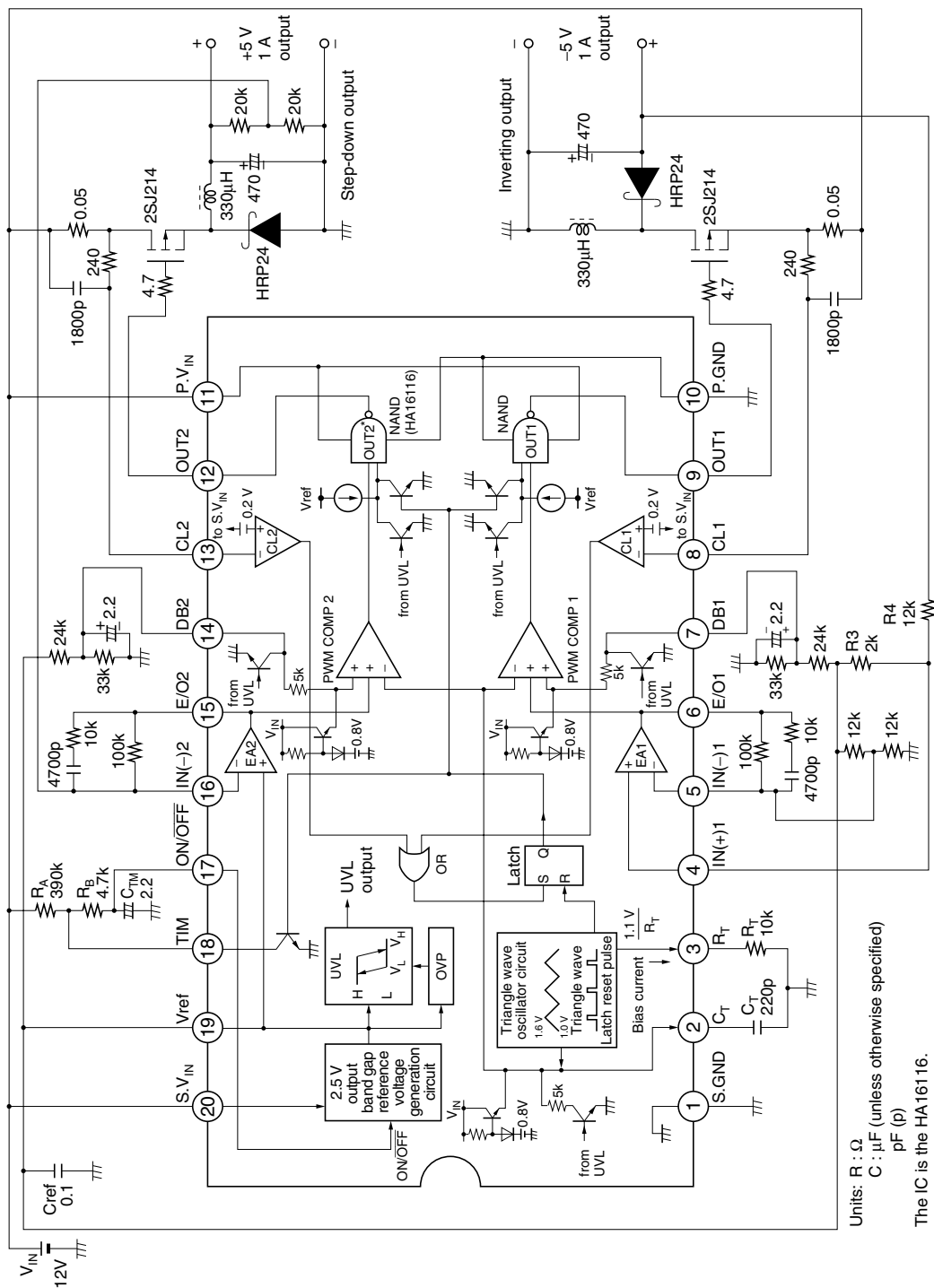
Note: The solid line is data measured with discrete capacitances (for each channel of HA16116).



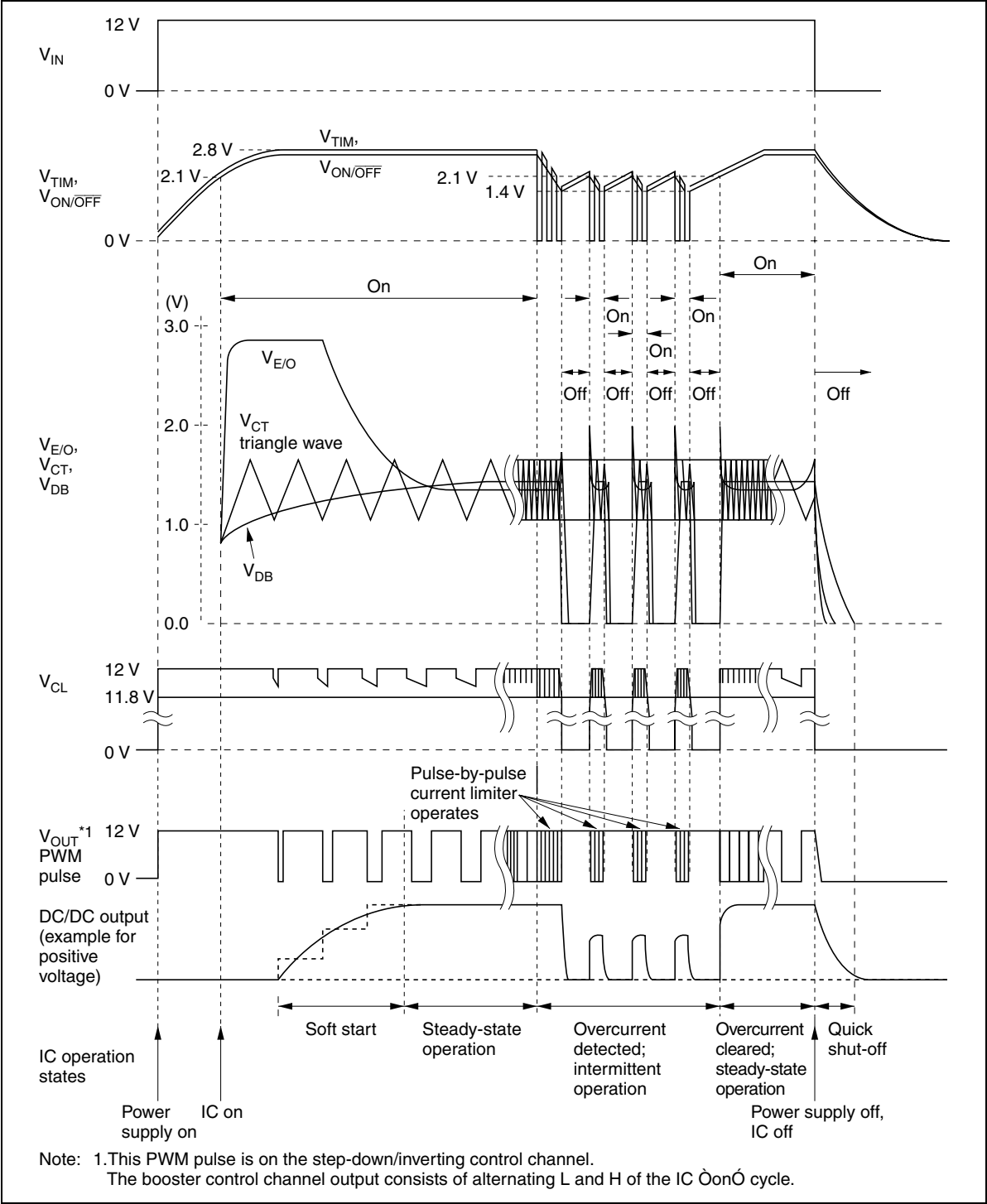
Note: * Measured using a current probe.
(The boost channel (channel 2 in the HA16121) load is with respect to ground, and has almost identical characteristics.)

Application Examples (1)

HA16116FP is used in a ± 5 V output power supply, with a +12 V input.

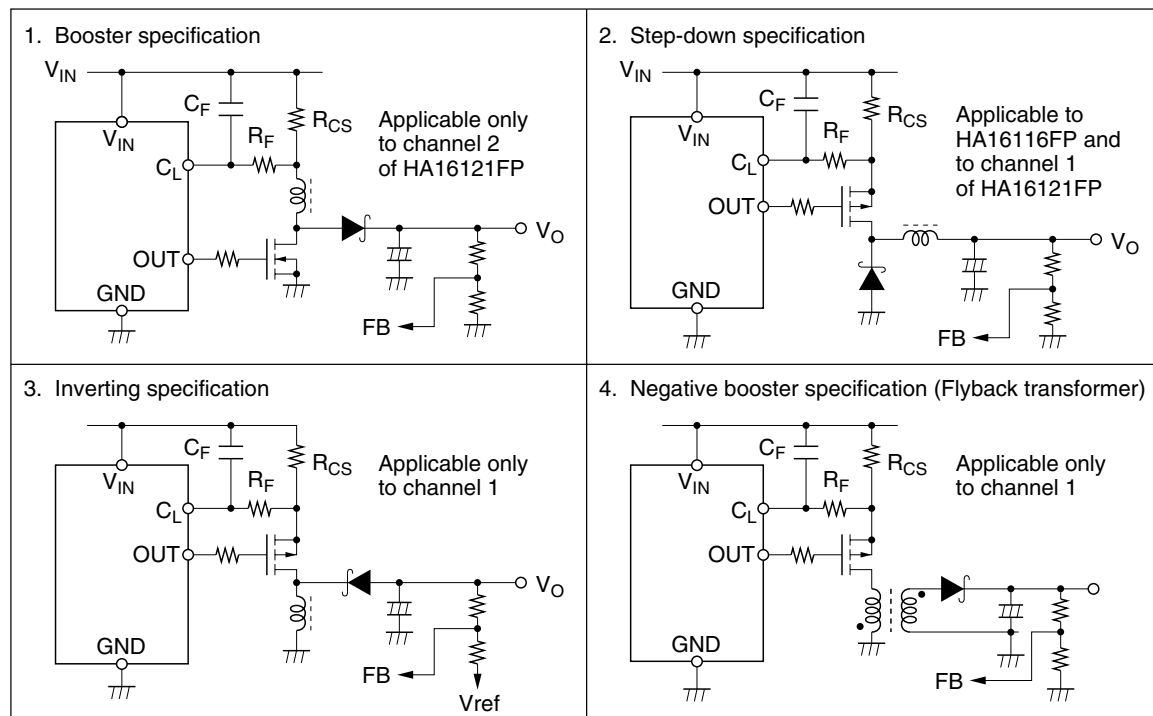


Overall Waveform Timing Diagram (for Application Examples (1))

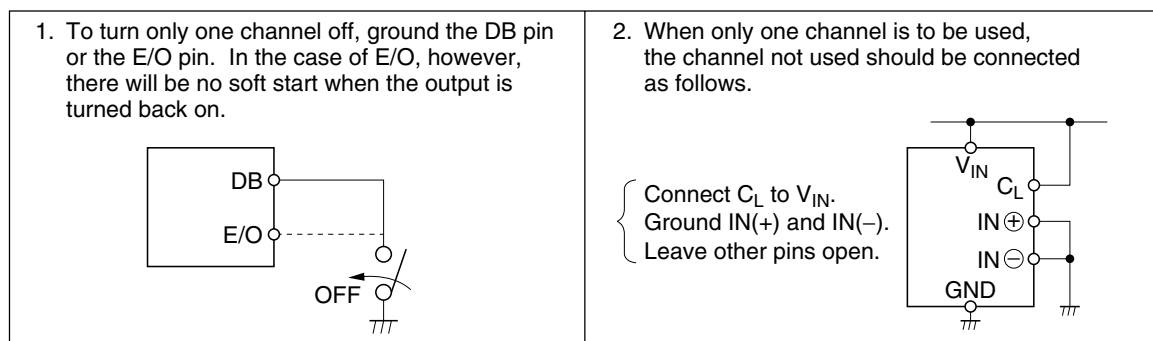


Application Examples (2) (Some Pointers on Use)

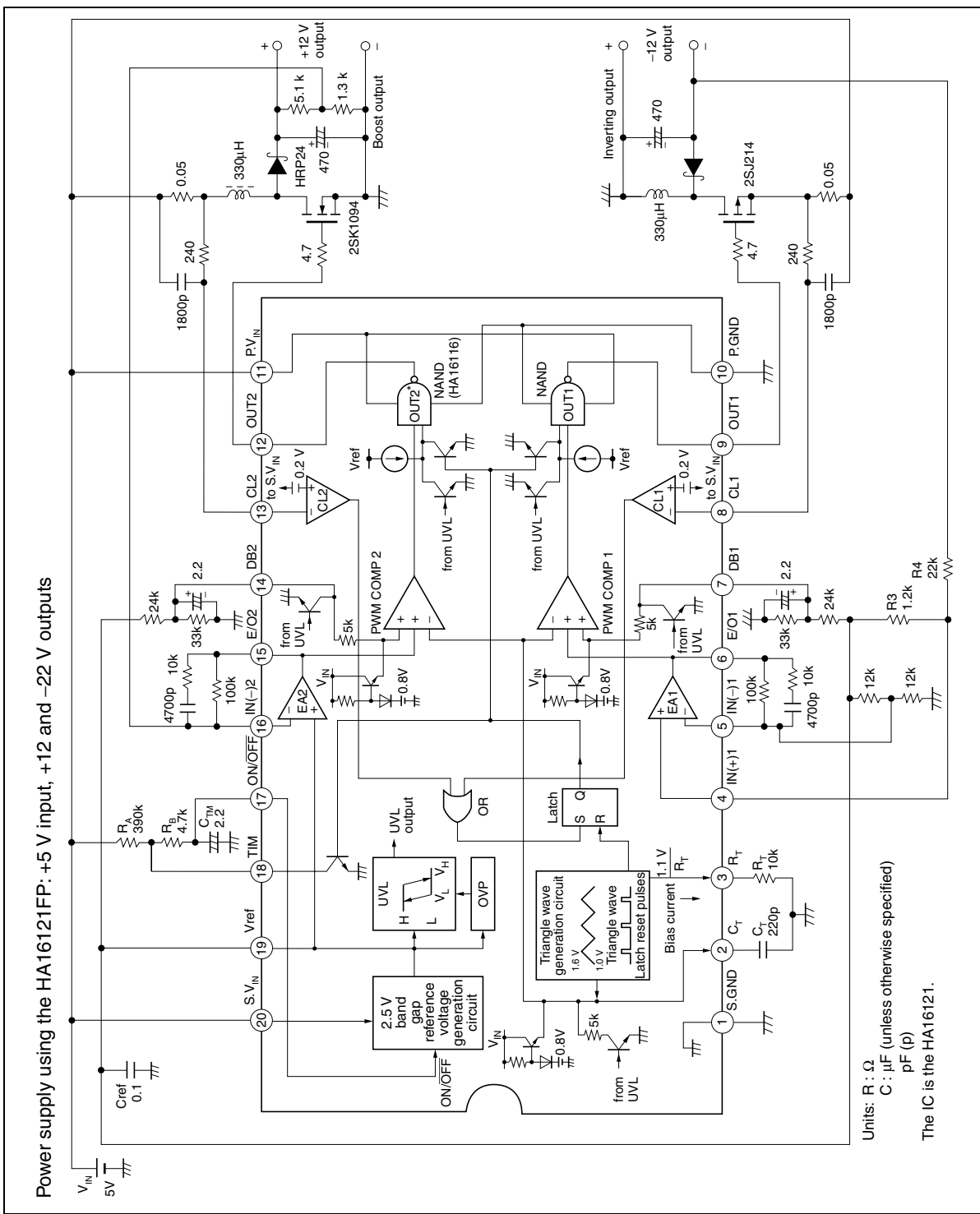
1. Inductor, Power MOS FET, and Diode Connections



2. Turning Output On and Off while the IC is On

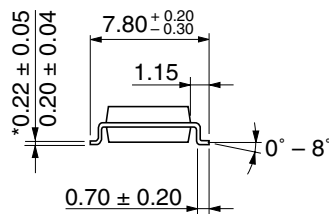
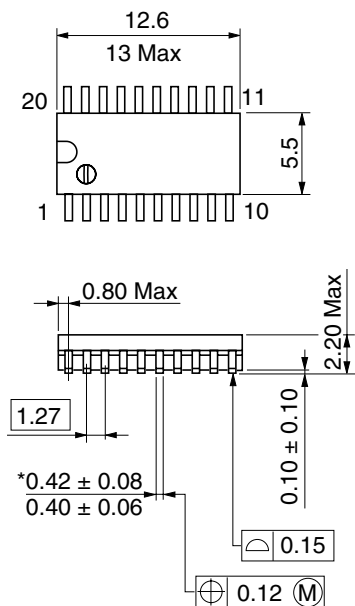


Application Examples (3)



Package Dimensions

As of January, 2002
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

Disclaimer

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

Sales Offices

HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL <http://www.hitachisemiconductor.com/>

For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe Ltd.
Electronic Components Group
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585200

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen
Postfach 201, D-85619 Feldkirchen
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00
Singapore 049318
Tel: <65>-538-6533/538-8577
Fax: <65>-538-6933/538-3877
URL: <http://semiconductor.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road
Hung-Kuo Building
Taipei (105), Taiwan
Tel: <886>-(2)-2718-3666
Fax: <886>-(2)-2718-8180
Telex: 23222 HAS-TP
URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon Hong Kong
Tel: <852>-(2)-735-9218
Fax: <852>-(2)-730-0281
URL: <http://semiconductor.hitachi.com.hk>

Copyright © Hitachi, Ltd., 2001. All rights reserved. Printed in Japan.
Colophon 5.0