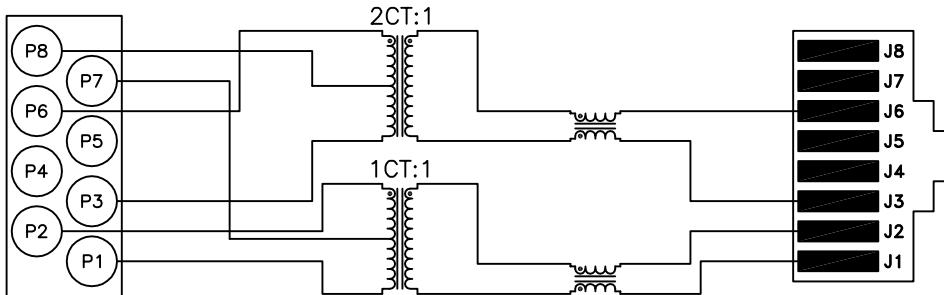
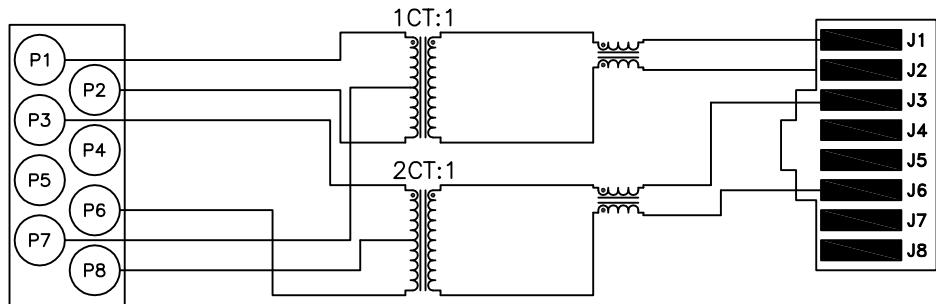


## LOWER ROW



## UPPER ROW



### NOTES:

1.0 PINS P4 AND P5 ARE OMITED.

### ELECTRICAL SPECIFICATIONS:

1.0 TURNS RATIO:  $(P_2 - P_7 - P_1) : (J_2 - J_1)$  : 1CT : 1  $\pm$  3%  
 $(P_3 - P_8 - P_6) : (J_3 - J_6)$  : 2CT : 1  $\pm$  3%

2.0 INDUCTANCE:  $(P_6 - P_3)$  : 140  $\mu$ H MIN. @ 0.01V, 10KHz  
 $(P_2 - P_1)$  : 140  $\mu$ H MIN. @ 0.01V, 10KHz

3.0 LEAKAGE INDUCTANCE: P6-P3 (WITH J6 AND J3 SHORT) : 1.0  $\mu$ H MAX. @ 1MHz  
P2-P1 (WITH J2 AND J1 SHORT) : 0.3  $\mu$ H MAX. @ 1MHz

4.0 INTERWINDING CAPACITANCE:  $(P_6, P_8, P_3)$  TO  $(J_6, J_3)$  : 12 pf MAX @ 1MHz  
 $(P_2, P_7, P_1)$  TO  $(J_2, J_1)$  : 12 pf MAX @ 1MHz

5.0 DC RESISTANCE:  $(J_6 - J_3) : (J_1 - J_2)$  : 1.0 ohms Max.  
 $(P_6 - P_3)$  : 1.0 ohms Max.  
 $(P_2 - P_1)$  : 0.6 ohms Max.

Bel Stewart Connector  
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717.234.7512

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<http://www.stewartconnector.com>

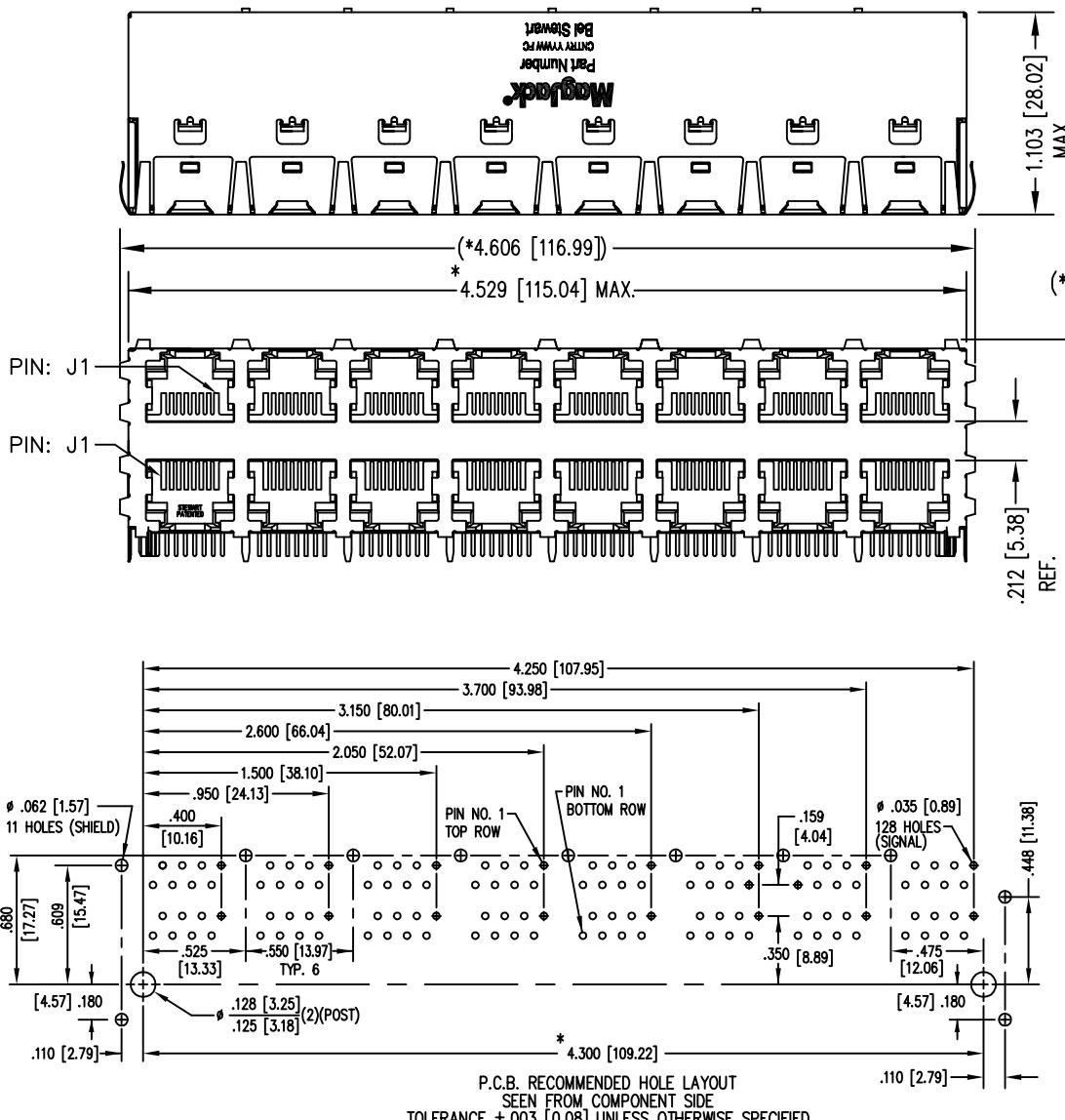
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SHEET  
1 OF 3

DRAWING NO.

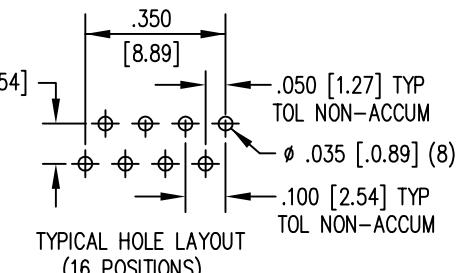
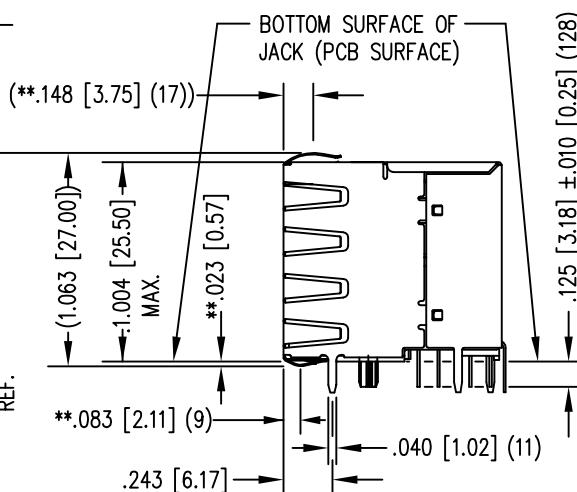
SI-30148 REV. 02

SHIELDING: "PG4-02" EMI-RFI 2 PIECE SHIELDED, ESD GROUNDED  
16 PORTS (8 OVER 8) STACKED JACK



NOTES:

- TOLERANCES COMPLY WITH F.C.C. DIMENSION REQUIREMENTS.
- DIMENSIONS SHOWN WITH "\*" TO BE CENTRAL ABOUT CENTER LINE.
- DIMENSIONS SHOWN ARE SUBJECT TO CHANGE WITHOUT NOTICE.
- PINS NOT ELECTRICALLY CONNECTED MAYBE OMITTED.  
SEE ELECTRICAL DRAWINGS FOR OMITTED PINS.
- 50 MICRO-INCH SELECTIVE GOLD PLATING
- WAVE SOLDER COMPATABLE - PREHEAT 125°C/90 SECS MAX.
- ALL POLYMERS FLAMMABILITY - UL94V0



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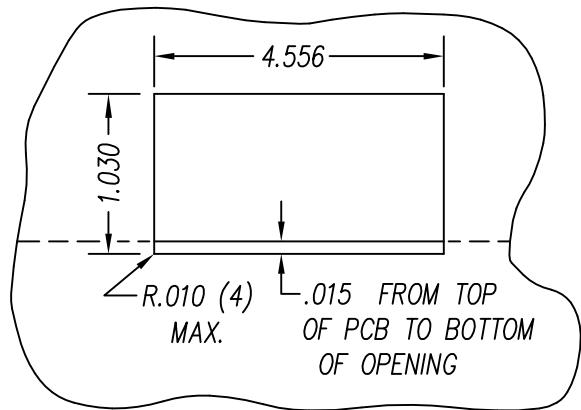
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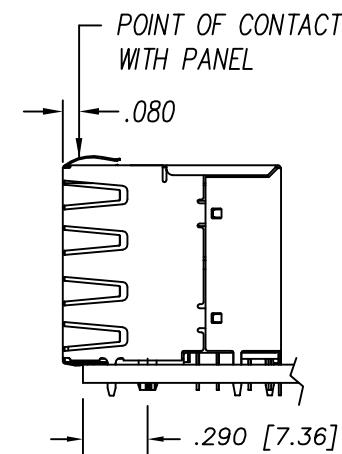
SHEET  
2 OF 3

DRAWING NO.

SI-30148 REV. 06



SUGGESTED PANEL OPENING  
(N.T.S.)



THE SUGGESTED PANEL OPENING IS INTENDED TO GIVE THE USER THE ABILITY TO HAVE REASONABLE JACK / PANEL CLEARANCES YET MAINTAIN RELIABLE GROUNDING CAPABILITY.

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SHEET  
3 OF 3

DRAWING NO.

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