

1-of-16 Decoder/Demultiplexer High-Performance Silicon-Gate CMOS

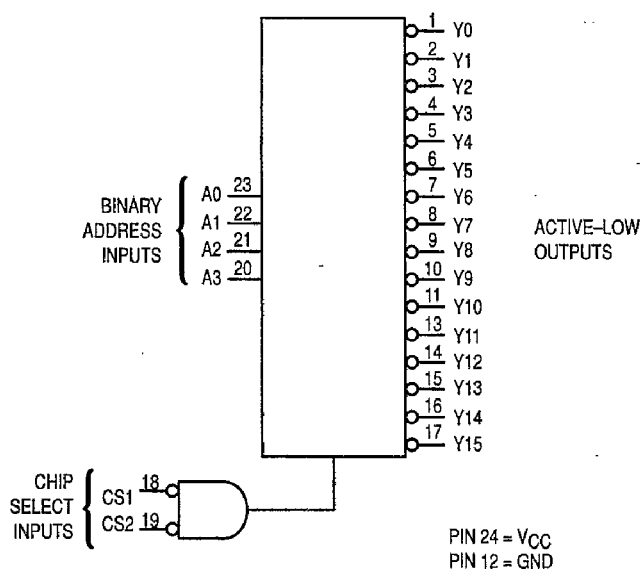
The MC54/74HC154 is identical in pinout to the LS154. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device, when enabled, selects one of 16 active-low outputs. Two active-low Chip Selects are provided to facilitate the chip-select, demultiplexing, and cascading functions. When either Chip Select is high, all outputs are high. The demultiplexing function is accomplished by using the Address inputs to select the desired device output. Then, while holding one chip select input low, data can be applied to the other chip select input (see Application Note).

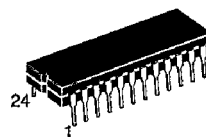
The HC154 is primarily used for memory address decoding and data routing applications.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 192 FETs or 48 Equivalent Gates

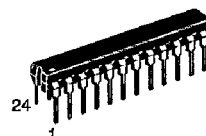
LOGIC DIAGRAM



MC54/74HC154



J SUFFIX
CERAMIC PACKAGE
CASE 758-02



N SUFFIX
PLASTIC PACKAGE
CASE 724-03



DW SUFFIX
SOIC PACKAGE
CASE 751E-04

ORDERING INFORMATION

MC54HCXXXJ	Ceramic
MC74HCXXXN	Plastic
MC74HCXXXDW	SOIC

PIN ASSIGNMENT

Y0	1	24	VCC
Y1	2	23	A0
Y2	3	22	A1
Y3	4	21	A2
Y4	5	20	A3
Y5	6	19	CS2
Y6	7	18	CS1
Y7	8	17	Y15
Y8	9	16	Y14
Y9	10	15	Y13
Y10	11	14	Y12
GND	12	13	Y11

3



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP or SOIC Package)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
Ceramic DIP: - 10 mW/°C from 100° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 2)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 8$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, CS to Output Y (Figures 2 and 3)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2.
- Information on typical parametric values can be found in Chapter 2.

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		80	

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2.

PIN DESCRIPTIONS**INPUTS****A0, A1, A2, A3 (Pins 23, 22, 21, 20)**

Address inputs. These inputs, when the 1-of-16 decoder is enabled, determine which of its sixteen active-low outputs is selected.

OUTPUTS**Y0 – Y15 (Pins 1 – 11, 13 – 17)**

Active-low outputs. These outputs assume a low level

when addressed and both chip-select inputs are active. These outputs remain high when not addressed or a chip-select input is high.

CONTROL INPUTS**CS1, CS2 (Pins 18, 19)**

Active-low chip-select inputs. With low levels on both of these inputs, the outputs of the decoder follow the Address inputs. A high level on either input forces all outputs high.

3**FUNCTION TABLE**

Inputs					Outputs																
CS1	CS2	A3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H
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L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
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L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	H	H	H	H	H	H												

H = High Level, L = Low Level, X = Don't Care

SWITCHING WAVEFORMS

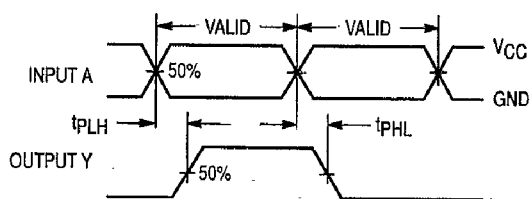


Figure 1.

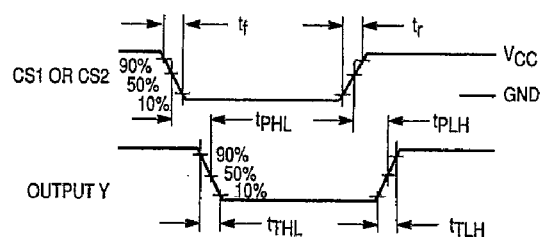
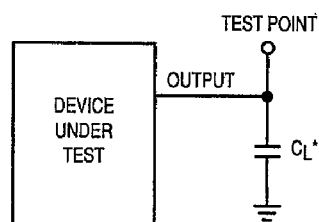


Figure 2.

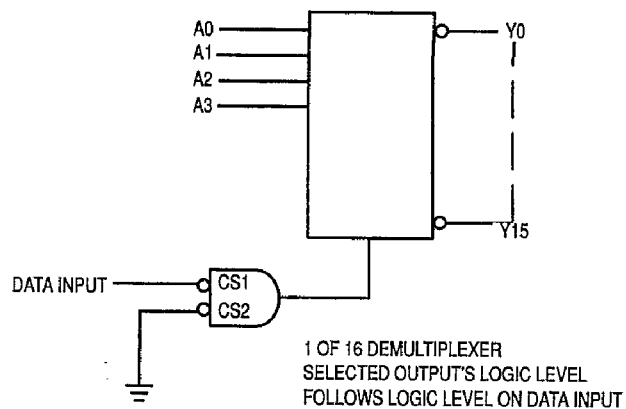
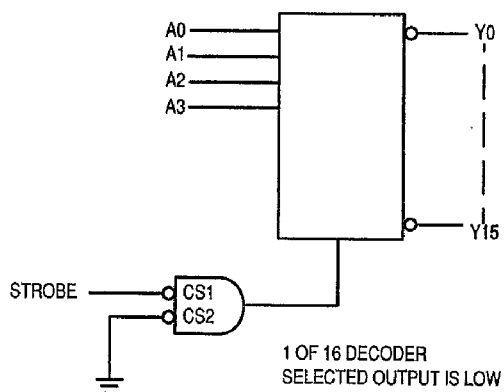


* Includes all probe and jig capacitance

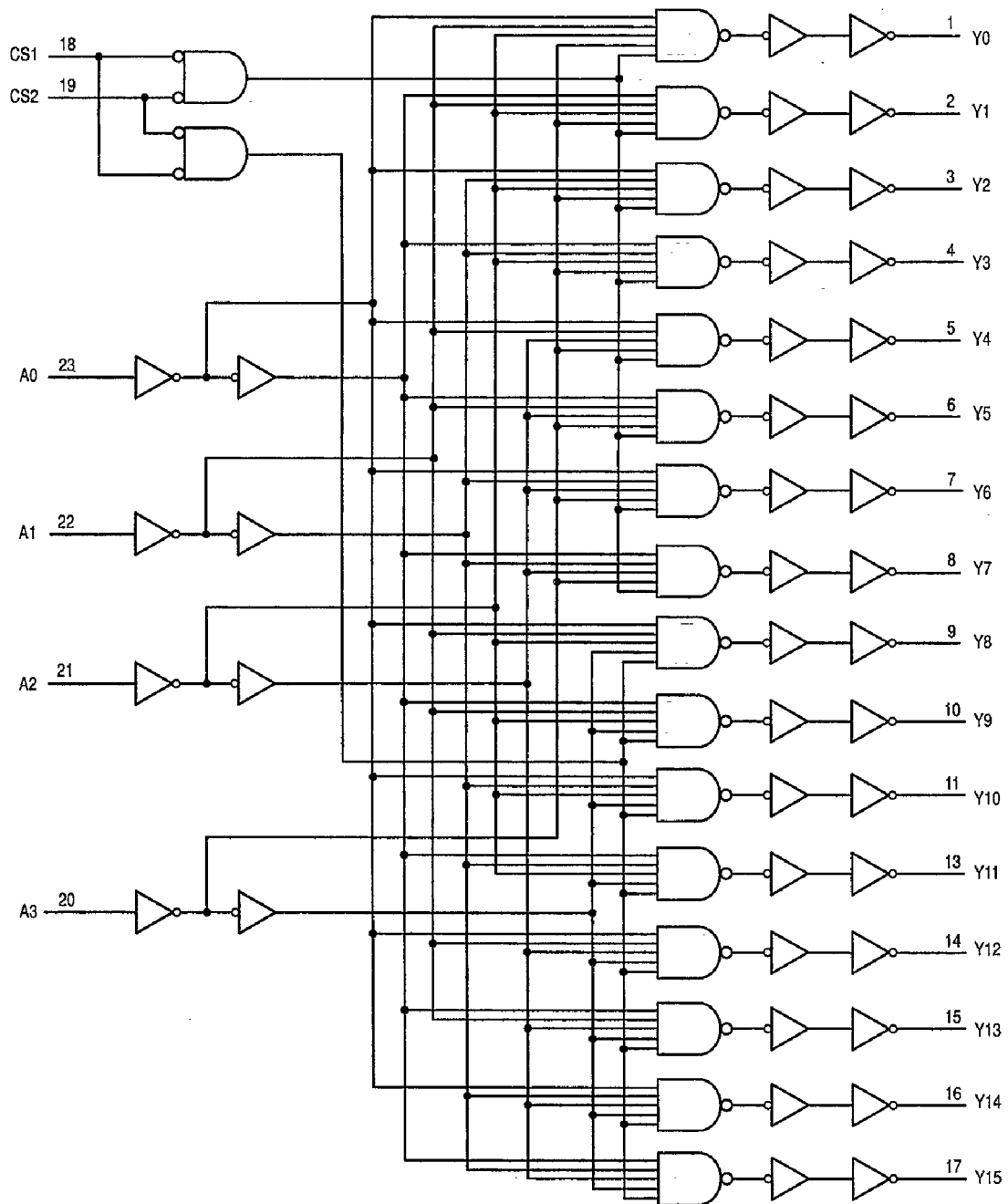
Figure 3. Test Circuit

3

TYPICAL APPLICATIONS



EXPANDED LOGIC DIAGRAM



3

Quad 2-Input Data Selectors/Multiplexers

High-Performance Silicon-Gate CMOS

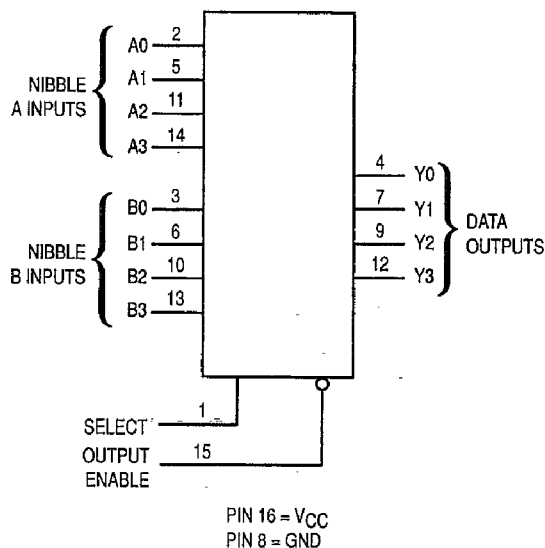
The MC54/74HC157A is identical in pinout to the LS157. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device routes 2 nibbles (A or B) to a single port (Y) as determined by the Select input. The data is presented at the outputs in noninverted form. A high level on the Output Enable input sets all four Y outputs to a low level.

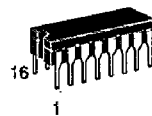
The HC157A is similar in function to the HC257 which has 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 82 FETs or 20.5 Equivalent Gates

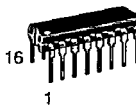
LOGIC DIAGRAM



MC54/74HC157A



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-08



D SUFFIX
SOIC PACKAGE
CASE 751B-05



DT SUFFIX
TSSOP PACKAGE
CASE 948F-01

ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXAD	SOIC
MC74HCXXXADT	TSSOP

PIN ASSIGNMENT

SELECT	1	16	V_{CC}
A0	2	15	OUTPUT ENABLE
B0	3	14	A3
Y0	4	13	B3
A1	5	12	Y3
B1	6	11	A2
Y1	7	10	B2
GND	8	9	Y2

FUNCTION TABLE

Inputs		Outputs Y0 - Y3
Output Enable	Select	
H	X	L
L	L	A0 - A3
L	H	B0 - B3

X = don't care
A0 - A3, B0 - B3 = the levels of the respective Data-Word Inputs.



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
Ceramic DIP: - 10 mW/°C from 100° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V 0 V _{CC} = 4.5 V 0 V _{CC} = 6.0 V 0	1000 500 400	ns

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 4)	2.0	105	130	160	ns
		4.5	21	26	32	
		6.0	18	22	27	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Select to Output Y (Figures 2 and 4)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2.

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	
		33	
			pF

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2.**PIN DESCRIPTIONS****INPUTS****A0, A1, A2, A3 (Pins 2, 5, 11, 14)**

Nibble A inputs. The data present on these pins is transferred to the outputs when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

B0, B1, B2, B3 (Pins 3, 6, 10, 13)

Nibble B inputs. The data present on these pins is transferred to the outputs when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

OUTPUTS**Y0, Y1, Y2, Y3 (Pins 4, 7, 9, 12)**

Data outputs. The selected input Nibble is presented at

these outputs when the Output Enable input is at a low level. The data present on these pins is in its noninverted form. For the Output Enable input at a high level, the outputs are at a low level.

CONTROL INPUTS**Select (Pin 1)**

Nibble select. This input determines the data word to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

Output Enable (Pin 15)

Output Enable input. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input sets all outputs to a low level.

SWITCHING WAVEFORMS

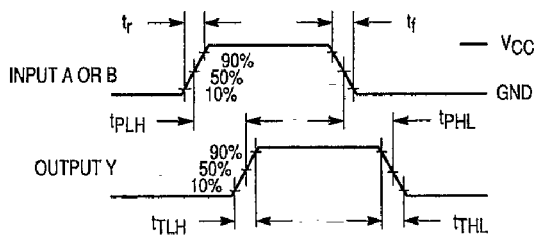


Figure 1. HC157A

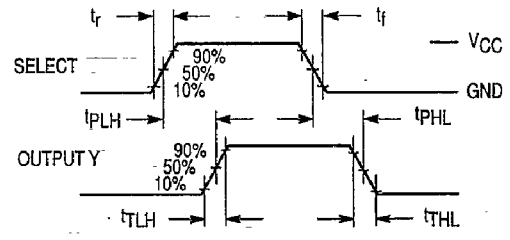


Figure 2. Y versus Select, Noninverted

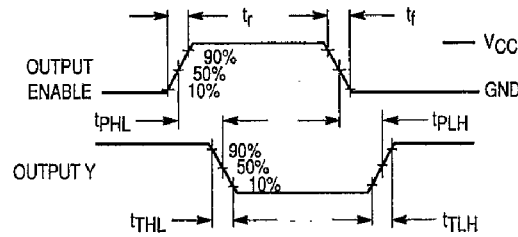
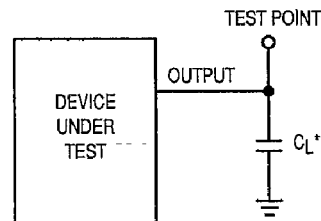


Figure 3. HC157A



* Includes all probe and jig capacitance

Figure 4. Test Circuit

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EXPANDED LOGIC DIAGRAM

