

**STRUCTURE** 

Silicon Monolithic Integrated Circuit

NAME OF PRODUCT

DC-AC Inverter Control IC

**TYPE** 

BD9887FS

**FUNCTION** 

- 36V High voltage process
- 1ch control with Full-Bridge
- · Lamp current and voltage sense feed back control
- · Sequencing easily achieved with Soft Start Control
- · Short circuit protection with Timer Latch
- Under Voltage Lock Out
- · Mode-selectable the operating or stand-by mode by stand-by pin
- · Synchronous operating the other BD9887FS IC's
- · BURST mode controlled by PWM and DC input
- · Output liner Control by external DC voltage

### ○Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage	Vcc	36	٧
BST pin	BST	40	V
SW pin	SW	36	V
BST-SW voltage difference	BST-SW	7	V
Operating Temperature Range	Topr	<b>-40∼+85</b>	°C
Storage Temperature Range	Tstg	-55~+125	°C
Maximum Junction Temperature	Tjmax	+150	°C
Power Dissipation	Pd	760*	mW

<sup>\*</sup>Pd derate at 6.08mW/℃ for temperature above Ta = 25℃ (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

### Operating condition

Parameter	Symbol	Limits	Unit
Supply voltage	VCC	6.5~30.0	٧
BST voltage	BST	4.0~36.0	٧
BST-SW voltage difference	BST-SW	4.0~6.0	٧
CT oscillation frequency	fCT	60~180	kHz
BCT oscillation frequency	fBCT	0.05~1.00	kHz

#### Status of this document

The Japanese version of this document is the official specification.

Please use the translation version of this document as a reference to expedite understanding of the official version. If these are any uncertainty in translation version of this document, official version takes priority.



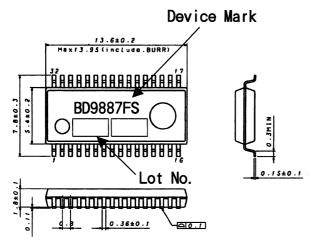
OElectric Characteristics (Ta=25°C, VCC=24V)

lectric Characteristics (Ta=	Symbol		Limits		Unit	Conditions
	- Cymbo.	MIN.	TYP.	MAX.		- GOIGITT GIS
((WHOLE DEVICE))	1 11		10.0	10.0		L VCT O EV
Operating current Stand-by current	lcc1		10.0	18.0 30.0	mA μA	VCT=0.5V
((STAND BY CONTROL))	1002		13.0	30.0	μ	<u> </u>
Stand-by voltage H	VstH	1.4	I – I	VCC	V	System ON
Stand-by voltage L	VstL	-0.3		0.8	v	System OFF
((UMLO BLOCK)))						
Operating voltage (VCC)	VuvloH	5.7	6.0	6.3	٧	
Shut down voltage (VCC)	VuvloL	5.4	5.7	6.0	٧	
Hesteresis width (VCC)	⊿VCC_Vuvlo	0.22	0.29	0.36	٧	<u> </u>
Operating voltage (UVLO)	Vuvlo1 Vuvlo2	2.10	2.16	2.22	V	
Shut down voltage (UVLO) Hesteresis width (UVLO)	ΔVuvio	0.074	0.098	2.321 0.122	<del>l v</del>	
((REG BLOCK))	1 244410 1	0.074	0.030	0.122	1 *	<u> </u>
REG output voltage	VREG	5.68	5.80	5.92	l v	VCC>7.0V
EG source current	IREG	20.0	-	-	mA	
/REF input voltage range	VREFIN	0.60	_	1.60	٧	No effect at VREF>1.25
((OSC BLOCK))						
Active edge setting current	lact	1.35/RT	1.5/RT	1.65/RT	V	
Negative edge setting current	Ineg	lact×8	lact×10	lact×12	٧	107 100111
OSC Max voltage	VoscH	1.8	2.0	2.2	V	fCT=120kHz
OSC Min voltage ①	VoscL1	0.32	0.63	0.94	V	fCT=50kHz
OSC Miin voltage ②	VoscL2	0.22	0.44	0.66	٧	fCT=120kHz
Soft start current	ISS	0.7	1.4	2.1	μA	
SRT ON resistance	RSRT		150	300	Ω	
((BOSC BLOCK))						
BOSC Max voltage	VBCTH	1.94	2.00	2.06	٧	fBCT=0.3kHz
BOSC Min voltage	VBCTL	0.40	0.50	0.60	٧	fBCT=0. 3kHz
BOSC constant current	IBCT	1.35/BRT	1.5/BRT	1.65/BRT	A	VBCT=0, 2V
BOSC frequency	fBCT	291	300	309	Hz	BRT=33k Ω BCT=0.048 μF
((FEED BACK BLOCK))					<u> </u>	
	VIS①	1.225	1,250	1.275	V	
IS threshold voltage 1	+		<del> </del>			
IS threshold voltage 2	VIS2	_	VREFIN	VIS①	٧	VREF applying voltage
VS threshold voltage	Vvs	1.225	1.250	1.275	\ v	
IS source current 1	1181	1	_	0.9	μA	DUTY=2.0V
IS source current 2	1182	35.6	57.0	78.4	μA	DUTY=0V IS=0.5V
VS source current	IVS			0.9	μA	
FB over voltage detect voltage	Vovf	2.2	2.5	2.8	V	10001115
IS COMP detect voltage ① IS COMP detect voltage ②	VISCOMP① VISCOMP②	0.893	0.92 VREFIN×0.74	0.947	V V	VREFIN≥1.25V
((DUTY BLOCK))	VISCOMF		VNEFINAU.74	<del>-</del>		VREFIN<1.25V
High voltage	VDUTY-0UTH	2.8	3.1	3.4	T v	<del></del>
Low voitage	VDUTY-OUTL			0.5	i v	
DUTY-OUT sink resistance						
	RDUTY-OUTSink	-	150	300	Ω	
DUTY-OUT source resistance	RDUTY-OUTSink RDUTY-OUTSource	-	150 200	400	Ω	<u> </u>
DUTY-OUT source resistance ((OUTPUT BLOCK))						
((OUTPUT BLOCK)) LN output sink resistance	RDUTY-OUTSource RsinkLN		1.5	3.0	Ω	
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance	RDUTY-OUTSource  RsinkLN RsourceLN	-	200 1.5 5.0	3. 0 10. 0	Ω Ω Ω	
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output sink resistance	RDUTY-OUTSource  RsinkLN  RsourceLN  RsinkHN	- - -	1.5 5.0 2.5	3. 0 10. 0 5. 0	Ω Ω Ω Ω	VBST-VSW=5.0V
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output sink resistance HN output source resistance	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN	- - - -	1.5 5.0 2.5 5.0	3. 0 10. 0 5. 0 10. 0	Ω Ω Ω Ω Ω	VBST-VSW=5.0V
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output sink resistance HN output source resistance MAX DUTY	RDUTY-OUTSource  RsinkLN  RsourceLN  RsinkHN  RsourceHN  MAX DUTY	- - - - - 44	200 1.5 5.0 2.5 5.0 46.5	3. 0 10. 0 5. 0 10. 0 49	Ω Ω Ω Ω Ω	VBST-VSW=5.0V FOUT=60kHz
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output sink resistance HN output source resistance MAX DUTY OFF period ①	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF①	- - - - - 44	1.5 5.0 2.5 5.0 46.5	3. 0 10. 0 5. 0 10. 0 49 200	Ω Ω Ω Ω Ω Ω Ω % ns	VBST-VSW=5.0V FOUT=60kHz SW>4.0V
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output sink resistance HN output source resistance MAX DUTY	RDUTY-OUTSource  RsinkLN  RsourceLN  RsinkHN  RsourceHN  MAX DUTY	- - - - - 44	200 1.5 5.0 2.5 5.0 46.5	400 3.0 10.0 5.0 10.0 49 200 310	Ω Ω Ω Ω Ω Ω Ω Ω Ν % ns ns	VBST-VSW=5.0V FOUT=60kHz SW>4.0V SW<2.0V
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output sink resistance HN output source resistance MAX DUTY OFF period ① OFF period ②	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF②	- - - - 44 - 150	1.5 5.0 2.5 5.0 46.5 120 230	3. 0 10. 0 5. 0 10. 0 49 200	Ω Ω Ω Ω Ω Ω Ω % ns	VBST-VSW=5.0V FOUT=60kHz SW>4.0V
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output sink resistance HN output source resistance MAX DUTY OFF period ① OFF period ② Drive output frequency	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF②	- - - - 44 - 150	1.5 5.0 2.5 5.0 46.5 120 230	400 3.0 10.0 5.0 10.0 49 200 310	Ω Ω Ω Ω Ω Ω Ω Ω Ν % ns ns	VBST-VSW=5.0V FOUT=60kHz SW>4.0V SW<2.0V
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output sink resistance HN output source resistance MAX DUTY OFF period ① OFF period ② Drive output frequency ((TIMER LATCH BLOCK)) Timer Latch setting voltage	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT	- - - - 44 - 150 58.5	200  1.5 5.0 2.5 5.0 46.5 120 230 60.0	3.0 10.0 5.0 10.0 49 200 310 61.5	Ω Ω Ω Ω Ω % ns ns kHz	VBST-VSM=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ.CT=430pF
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output sink resistance HN output source resistance MAX DUTY OFF period ① OFF period ② Drive output frequency ((TIMER LATCH BLOCK))	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT	- - - - - 44 - 150 58.5	200 1.5 5.0 2.5 5.0 46.5 120 230 60.0	3.0 10.0 5.0 10.0 49 200 310 61.5	Ω Ω Ω Ω Ω % ns ns kHz	VBST-VSM=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ CT=430pF  except for under voltage detecting
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output sink resistance HN output source resistance MAX DUTY OFF period ① OFF period ② Drive output frequency ((TIMER LATCH BLOCK)) Timer Latch setting voltage	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT	- - - - 44 - 150 58.5	200  1.5 5.0 2.5 5.0 46.5 120 230 60.0	3.0 10.0 5.0 10.0 49 200 310 61.5	Ω Ω Ω Ω Ω % ns ns kHz	VBST-VSW=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ、CT=430pF  except for under voltage detecting only under
((OUTPUT BLOCK)) LN output sink resistance LN output sink resistance HN output sink resistance HN output sink resistance MAX DUTY OFF period ① OFF period ② Drive output frequency ((TIMER LATCH BLOCK)) Timer Latch setting voltage Timer Latch setting current ①	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT  VCP	- - - - - 44 - 150 58.5	200  1.5 5.0 2.5 5.0 46.5 120 230 60.0	400 3.0 10.0 5.0 10.0 49 200 310 61.5 2.06 0.79	Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω	VBST-VSM=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ CT=430pF  except for under voltage detecting
((OUTPUT BLOCK)) LN output sink resistance LN output sink resistance HN output sink resistance HN output source resistance MAX DUTY OFF period ① DFT period ② DFT period ② ((TIMER LATCH BLOCK)) Timer Latch setting voltage Timer Latch setting current ① Timer Latch setting current ② ((COMP CLOCK))	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT  VCP ICP1 ICP2	- - - - 44 - 150 58.5 1.94 0.53	200  1.5 5.0 2.5 5.0 46.5 120 230 60.0  2.0 0.66 6.22	400  3.0  10.0  5.0  10.0  49  200  310  61.5  2.06  0.79	Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω	VBST-VSW=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ、CT=430pF  except for under voltage detecting only under voltage detecting
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output source resistance HN output source resistance HN output source resistance MAX DUTY OFF period ① OFF period ② Drive output frequency ((TIMER LATCH BLOCK)) Timer Latch setting voltage Timer Latch setting current ① Timer Latch setting current ② ((COMP CLOCK)) COMP1 over voltage detect voltage	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT  VCP ICP1 ICP2  VCOMPH	- - - - 44 - 150 58.5 1.94 0.53 4.98	200  1.5 5.0 2.5 5.0 46.5 120 230 60.0  2.0 0.66 6.22	400  3.0  10.0  5.0  10.0  49  200  310  61.5  2.06  0.79  7.46	Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω	VBST-VSM=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ.CT=430pF  except for under voltage detecting only under voltage detecting VSS>2.2V
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output source resistance HN output source resistance HN output source resistance MAX DUTY OFF period ① OFF period ② Drive output frequency ((TIMER LATCH BLOCK)) Timer Latch setting voltage Timer Latch setting current ① Timer Latch setting current ② ((COMP CLOCK)) COMPI over voltage detect voltage COMP2 over voltage detect voltage	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT  VCP ICP1 ICP2  VCOMPH VCMOP2_H	- - - - 44 - 150 58.5 1.94 0.53 4.98	200  1.5 5.0 2.5 5.0 46.5 120 230 60.0  2.0 0.66 6.22	400  3.0  10.0  5.0  10.0  49  200  310  61.5  2.06  0.79  7.46	Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ν Ν Ν Ν Ν Ν Ν Ν Ν	VBST-VSM=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ.CT=430pF  except for under voltage detecting only under voltage detecting VSS>2.2V VSS>2.2V
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output source resistance HN output source resistance HN output source resistance MAX DUTY OFF period ① OFF period ② Drive output frequency ((TIMER LATCH BLOCK)) Timer Latch setting voltage Timer Latch setting current ① Timer Latch setting current ② ((COMP CLOCK)) COMP1 over voltage detect voltage	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT  VCP ICP1 ICP2  VCOMPH VCMOP2_H VCOMP_L_1	- - - - 44 - 150 58.5 1.94 0.53 4.98	200  1.5 5.0 2.5 5.0 46.5 120 230 60.0  2.0 0.66 6.22	400  3. 0  10. 0  5. 0  10. 0  49  200  310  61. 5  2. 06  0. 79  7. 46  2. 510  2. 510  1. 275	Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω	VBST-VSW=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ, CT=430pF  except for under voltage detecting only under voltage detecting VSS>2.2V VSS>2.2V VSS>2.2V
((OUTPUT BLOCK)) LN output sink resistance LN output sink resistance HN output sink resistance HN output sink resistance HN output sink resistance MAX DUTY  OFF period ①  OFF period ②  Drive output frequency  ((TIMER LATCH BLOCK)) Timer Latch setting voltage  Timer Latch setting current ①  Timer Latch setting current ②  ((COMP1 over voltage detect voltage  COMP2 over voltage detect voltage  COMP2 under voltage detect voltage	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT  VCP ICP1 ICP2  VCOMPH VCMOP2_H		200  1.5 5.0 2.5 5.0 46.5 120 230 60.0  2.0 0.66 6.22	400  3.0  10.0  5.0  10.0  49  200  310  61.5  2.06  0.79  7.46	Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ν Ν Ν Ν Ν Ν Ν Ν Ν	VBST-VSM=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ.CT=430pF  except for under voltage detecting only under voltage detecting VSS>2.2V VSS>2.2V
((OUTPUT BLOCK))  LN output sink resistance LN output sink resistance HN output source resistance HN output source resistance HN output source resistance MAX DUTY OFF period ① Drive output frequency ((TIMER LATCH BLOCK)) Timer Latch setting voltage Timer Latch setting current ①  ((COMP CLOCK)) COMP1 over voltage detect voltage COMP2 under voltage detect voltage ① COMP2 under voltage detect voltage ② (((Synchronous Block)) High voltage	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT  VCP ICP1 ICP2  VCOMPH VCMOP2_H VCOMP_L_1		200  1.5 5.0 2.5 5.0 46.5 120 230 60.0  2.0 0.66 6.22	400  3. 0  10. 0  5. 0  10. 0  49  200  310  61. 5  2. 06  0. 79  7. 46  2. 510  2. 510  1. 275	Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω	VBST-VSW=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ, CT=430pF  except for under voltage detecting only under voltage detecting VSS>2.2V VSS>2.2V VSS>2.2V
((OUTPUT BLOCK)) LN output sink resistance LN output source resistance HN output source resistance HN output source resistance HN output source resistance MAX DUTY OFF period ① OFF period ② Drive output frequency ((TIMER LATCH BLOCK)) Timer Latch setting voltage Timer Latch setting current ①  Timer Latch setting current ② ((COMP CLOCK)) COMP1 over voltage detect voltage COMP2 under voltage detect voltage (((Synchronous Block)) High voltage Low voltage	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT  VCP ICP1 ICP2  VCOMPH VCMOP2_H VCOMP_L_1 VCOMP_L_2  VCT_SYNCH VCT_SYNCL		200  1.5 5.0 2.5 5.0 46.5 120 230 60.0  2.0 0.66 6.22  2.485 2.485 1.25 0.625	3.0 10.0 5.0 10.0 49 200 310 61.5 2.06 0.79 7.46 2.510 2.510 1.275 0.644 3.4 0.5	Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω	VBST-VSW=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ, CT=430pF  except for under voltage detecting only under voltage detecting VSS>2.2V VSS>2.2V VSS>2.2V
((OUTPUT BLOCK)) LN output sink resistance LN output sink resistance HN output sink resistance HN output sink resistance HN output sink resistance MAX DUTY OFF period ① OFF period ② Drive output frequency ((TIMER LATCH BLOCK)) Timer Latch setting voltage Timer Latch setting current ① Timer Latch setting current ② ((COMP1 over voltage detect voltage COMP2 under voltage detect voltage COMP2 under voltage detect voltage ② ((Synchronous Block)) High voltage Low voltage Low voltage Low voltage CT_SYNC sink resistance	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT  VCP ICP1 ICP2  VCOMPH VCMOP2_H VCOMP_L_1 VCOMP_L_2  VCT_SYNCH VCT_SYNCL RCT_SYNC_SYNC		200  1.5 5.0 2.5 5.0 46.5 120 230 60.0  2.0 0.66 6.22  2.485 2.485 1.25 0.625	3.0 10.0 5.0 10.0 49 200 310 61.5 2.06 0.79 7.46 2.510 2.510 1.275 0.644 3.4 0.5 300	Ω Ω Ω Ω Ω Ω Ω Ω Ν πs ns kHz V μA ν ν ν ν ν ν	VBST-VSW=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ, CT=430pF  except for under voltage detecting only under voltage detecting VSS>2.2V VSS>2.2V VSS>2.2V
((OUTPUT BLOCK)) LN output sink resistance LN output sink resistance HN output sink resistance HN output sink resistance HN output source resistance MAX DUTY OFF period ① OFF period ② Drive output frequency ((TIMER LATCH BLOCK)) Timer Latch setting voltage Timer Latch setting current ② ((COMP1 over voltage detect voltage COMP2 over voltage detect voltage COMP2 under voltage detect voltage ② ((Synchronous Block)) High voltage Low voltage CT_SYNC source resistance CT_SYNC source resistance	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT  VCP ICP1 ICP2  VCMIPH VCMOP2_H VCMOP2_L VCOMP_L_1 VCT_SYNCL RCT_SYNC_SOURCE		200  1.5 5.0 2.5 5.0 46.5 120 230 60.0  2.0 0.66 6.22  2.485 1.25 0.625  3.1 - 150 370	400  3. 0  10. 0  5. 0  10. 0  49  200  310  61. 5  2. 06  0. 79  7. 46  2. 510  2. 510  1. 275  0. 644  3. 4  0. 5  300  740	Ω Ω Ω Ω Ω Ω Ω Ω Ν πs ns ns ν ν ν ν ν ν ν Ω Ω	VBST-VSW=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ、CT=430pF  except for under voltage detecting only under voltage detecting VSS>2.2V VSS>2.2V VSS>2.2V VSS<2.2V
((OUTPUT BLOCK)) LN output sink resistance LN output sink resistance HN output sink resistance HN output sink resistance HN output sink resistance MAX DUTY OFF period ① OFF period ② Drive output frequency ((TIMER LATCH BLOCK)) Timer Latch setting voltage Timer Latch setting current ① Timer Latch setting current ② ((COMP1 over voltage detect voltage COMP2 under voltage detect voltage COMP2 under voltage detect voltage ② ((Synchronous Block)) High voltage Low voltage Low voltage Low voltage CT_SYNC sink resistance	RDUTY-OUTSource  RsinkLN RsourceLN RsinkHN RsourceHN MAX DUTY TOFF① TOFF② fCT  VCP ICP1 ICP2  VCOMPH VCMOP2_H VCOMP_L_1 VCOMP_L_2  VCT_SYNCH VCT_SYNCL RCT_SYNC_SYNC		200  1.5 5.0 2.5 5.0 46.5 120 230 60.0  2.0 0.66 6.22  2.485 2.485 1.25 0.625	3.0 10.0 5.0 10.0 49 200 310 61.5 2.06 0.79 7.46 2.510 2.510 1.275 0.644 3.4 0.5 300	Ω Ω Ω Ω Ω Ω Ω Ω Ν πs ns kHz V μA ν ν ν ν ν ν	VBST-VSW=5.0V FOUT=60kHz SW>4.0V SW<2.0V RT=15kΩ, CT=430pF  except for under voltage detecting only under voltage detecting VSS>2.2V VSS>2.2V VSS>2.2V

(This product is not designed to be radiation-resistant.)

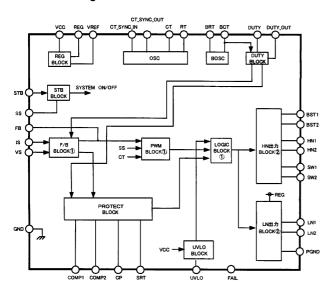


# OPackage Dimensions



SSOP-A32 (unit:mm)

## OBlock Diagram



# **OPin Description**

1 PGND Ground for FET driver  2 LN2 NMOS FET driver  3 HN2 NMOS FET driver  4 SW2 Lower rail voltage for HN2 output  5 BST2 Boot-Strap input for HN2 output  6 CT_SYNC_IN CT synchronous signal input pin  7 CT_SYNC_OUT CT synchronous signal output pin  8 SRT External resistor from SRT to RT for adjusting the triangle oscillator  9 RT External resistor from SRT to RT for adjusting the triangle oscillator  10 CT External capacitor from CT to GND for adjusting the triangle oscillator  11 GND GROUND  12 BCT External capacitor from BCT to GND for adjusting the BURST triangle oscillator  13 BRT External resistor from BRT to RND for adjusting the BURST triangle oscillator  14 DUTY Control PWM mode and BURST mode  15 DUTY_OUT BURST signal output pin  16 STB Stand-by switch  17 CP External capacitor from CP to GND for Timer Latch  18 FAIL COMP2 under voltage protect clock output  19 VREF Reference voltage input pin for Error amplifier ①  20 VS Error amplifier input ②  21 IS Error amplifier input ②  22 FB Error amplifier input ①  23 SS External capacitor from SS to GND for Soft Start Control  24 COMP2 Under, over voltage detect pin  25 COMP1 Over voltage detect pin  26 VCC Supply voltage input  27 UVLO External Under Voltage Lock Out  28 REG Internal regulator output  29 BST1 Boot-Strap input for HN1 output  30 SW1 Lower rail voltage for HN1 output  31 HN1 NMOS FET driver	PIN No.	PIN NAME	FUNCTION
A SW2 Lower rail voltage for HN2 output  BST2 Boot-Strap input for HN2 output  CT_SYNC_IN CT synchronous signal input pin  CT_SYNC_OUT CT synchronous signal output pin  External resistor from SRT to RT for adjusting the triangle oscillator  RT External resistor from SRT to RT for adjusting the triangle oscillator  CT External capacitor from CT to GND for adjusting the triangle oscillator  RRT External capacitor from BCT to GND for adjusting the triangle oscillator  RROND GROUND  External capacitor from BCT to GND for adjusting the BURST triangle oscillator  External resistor from BRT to GND for adjusting the BURST triangle oscillator  External resistor from BRT to GND for adjusting the BURST triangle oscillator  DUTY Control PMM mode and BURST mode  DUTY_OUT BURST signal output pin  STB Stand-by switch  CP External capacitor from CP to GND for Timer Latch  External capacitor from CP to GND for Timer Latch  RAIL COMP2 under voltage protect clock output Reference voltage input pin for Error amplifier ①  VS Error amplifier input ②  SE FRO External capacitor from SS to GND for Soft Start Control  Under, over voltage detect pin  COMP1 Under, over voltage detect pin  COMP1 Over voltage detect pin  COMP1 Over voltage input  External regulator output  REG Internal regulator output  REG Internal regulator output  NULO External under Voltage for HN1 output  NUCO SWI Lower rail voltage for HN1 output	1	PGND	Ground for FET drivers
SW2 Lower rail voltage for HN2 output  BST2 Boot-Strap input for HN2 output  CT_SYNC_IN CT synchronous signal input pin  CT_SYNC_OUT CT synchronous signal output pin  RRT External resistor from SRT to RT for adjusting the triangle oscillator  External resistor from SRT to RT for adjusting the triangle oscillator  CT External capacitor from CT to GND for adjusting the triangle oscillator  RRD GROUND  BCT External capacitor from BCT to GND for adjusting the BURST triangle oscillator  External resistor from BRT to GND for adjusting the BURST triangle oscillator  External resistor from BRT to GND for adjusting the BURST triangle oscillator  DUTY Control PWM mode and BURST mode  DUTY_OUT BURST signal output pin  STB Stand-by switch  CP External capacitor from CP to GND for Timer Latch  FAIL COMP2 under voltage protect clock output  Reference voltage input pin for Error amplifier ①  VS Error amplifier input ②  SS External capacitor from SS to GND for Soft Start Control  Under, over voltage detect pin  COMP2 Under, over voltage detect pin  COMP1 Under, over voltage Lock Out  REG Internal regulator output  REG Internal regulator output  REG Internal regulator output  REG Internal regulator output  NEC REG Internal regulator output	2	LN2	NMOS FET driver
BST2 Boot-Strap input for HN2 output  CT_SYNC_IN CT synchronous signal input pin  CT_SYNC_OUT CT synchronous signal output pin  RRT External resistor from SRT to RT for adjusting the triangle oscillator  External resistor from SRT to RT for adjusting the triangle oscillator  CT External capacitor from CT to GND for adjusting the triangle oscillator  RROD GROUND  BCT External capacitor from BCT to GND for adjusting the BURST triangle oscillator  External resistor from BRT to GND for adjusting the BURST triangle oscillator  External resistor from BRT to GND for adjusting the BURST triangle oscillator  DUTY Control PWM mode and BURST mode  DUTY_OUT BURST signal output pin  STB Stand-by switch  CP External capacitor from CP to GND for Timer Latch  Reference voltage input pin for Error amplifier ①  VREF Reference voltage input pin for Error amplifier ①  VS Error amplifier input ②  IS Error amplifier output  External capacitor from SS to GND for Soft Start Control  COMP2 Under, over voltage detect pin  COMP1 Over voltage detect pin  COMP2 Under, over voltage Lock Out  REG Internal regulator output  NIMOS FET driver	3	HN2	NMOS FET driver
6 CT_SYNC_IN CT synchronous signal input pin 7 CT_SYNC_OUT CT synchronous signal output pin 8 SRT External resistor from SRT to RT for adjusting the triangle oscillator 9 RT External resistor from SRT to RT for adjusting the triangle oscillator 10 CT External capacitor from CT to GND for adjusting the triangle oscillator 11 GND GROUND 12 BCT External capacitor from BCT to GND for adjusting the BURST triangle oscillator 13 BRT External resistor from BRT to GND for adjusting the BURST triangle oscillator 14 DUTY Control PWM mode and BURST mode 15 DUTY_OUT BURST signal output pin 16 STB Stand-by switch 17 CP External capacitor from CP to GND for Timer Latch 18 FAIL COMP2 under voltage protect clock output 19 VREF Reference voltage input pin for Error amplifier ① 20 VS Error amplifier input ② 21 IS Error amplifier input ② 22 FB Error amplifier output 23 SS External capacitor from SS to GND for Soft Start Control 24 COMP2 Under, over voltage detect pin 25 COMP1 Over voltage detect pin 26 VCC Supply voltage input 27 UVLO External Under Voltage Lock Out 28 REG Internal regulator output 29 BST1 Boot-Strap input for HN1 output 30 SW1 Lower rail voltage for HN1 output 31 HN1 NMOS FET driver	4	SW2	Lower rail voltage for HN2 output
TCT_SYNC_OUT CT synchronous signal output pin  External resistor from SRT to RT for adjusting the triangle oscillator  PRT External resistor from SRT to RT for adjusting the triangle oscillator  CCT External capacitor from CT to GND for adjusting the triangle oscillator  RROD GROUND  BCT External capacitor from BCT to GND for adjusting the triangle oscillator  RROD GROUND  BCT External capacitor from BCT to GND for adjusting the BURST triangle oscillator  BCT External resistor from BRT to GND for adjusting the BURST triangle oscillator  DUTY Control PWM mode and BURST mode  DUTY_OUT BURST signal output pin  STB Stand-by switch  CP External capacitor from CP to GND for Timer Latch  Reference voltage input pin for Error amplifier ①  VREF Reference voltage input pin for Error amplifier ①  VS Error amplifier input ②  SET Error amplifier output  SS External capacitor from SS to GND for Soft Start Control  COMP2 Under, over voltage detect pin  COMP1 Over voltage detect pin  COMP2 Under, over voltage lock Out  REG Internal regulator output  BST1 Boot-Strap input for HN1 output  NMOS FET driver	5	BST2	Boot-Strap input for HN2 output
8 SRT External resistor from SRT to RT for adjusting the triangle oscillator 9 RT External resistor from SRT to RT for adjusting the triangle oscillator 10 CT External capacitor from CT to GND for adjusting the triangle oscillator 11 GND GROUND 12 BCT External capacitor from BCT to GND for adjusting the BURST triangle oscillator 13 BRT External resistor from BRT to GND for adjusting the BURST triangle oscillator 14 DUTY Control PWM mode and BURST mode 15 DUTY_OUT BURST signal output pin 16 STB Stand-by switch 17 CP External capacitor from CP to GND for Timer Latch 18 FAIL COMP2 under voltage protect clock output 19 VREF Reference voltage input pin for Error amplifier ① 20 VS Error amplifier input ② 21 IS Error amplifier input ① 22 FB Error amplifier output 23 SS External capacitor from SS to GND for Soft Start Control 24 COMP2 Under, over voltage detect pin 25 COMP1 Over voltage detect pin 26 VCC Supply voltage input 27 UVLO External Under Voltage Lock Out 28 REG Internal regulator output 29 BST1 Boot-Strap input for HN1 output 30 SW1 Lower rail voltage for HN1 output 31 HN1 NMOS FET driver	6	CT_SYNC_IN	CT synchronous signal input pin
the triangle oscillator  RT External resistor from SRT to RT for adjusting the triangle oscillator  External capacitor from CT to GND for adjusting the triangle oscillator  RND GROUND  External capacitor from BCT to GND for adjusting the BURST triangle oscillator  External resistor from BRT to GND for adjusting the BURST triangle oscillator  External resistor from BRT to GND for adjusting the BURST triangle oscillator  DUTY Control PWM mode and BURST mode  DUTY_OUT BURST signal output pin  STB Stand-by switch  CP External capacitor from CP to GND for Timer Latch  FAIL COMP2 under voltage protect clock output  Reference voltage input pin for Error amplifier ①  VREF Reference voltage input pin for Error amplifier ①  VS Error amplifier input ②  IS Error amplifier output  SS External capacitor from SS to GND for Soft Start Control  Under, over voltage detect pin  COMP2 Under, over voltage lock Out  REG Internal regulator output  REG Internal regulator output  SWI External Under Voltage Lock Out  REG Internal regulator output  NMOS FET driver	7	CT_SYNC_OUT	CT synchronous signal output pin
the triangle oscillator  CT External capacitor from CT to GND for adjusting the triangle oscillator  GND GROUND  External capacitor from BCT to GND for adjusting the BURST triangle oscillator  BRT External resistor from BRT to GND for adjusting the BURST triangle oscillator  Control PWMM mode and BURST mode  DUTY_OUT BURST signal output pin  BRT Stand-by switch  CP External capacitor from CP to GND for Timer Latch  FAIL COMP2 under voltage protect clock output  Reference voltage input pin for Error amplifier ①  VREF Reference voltage input pin for Error amplifier input ②  Error amplifier input ②  FB Error amplifier output  COMP2 Under, over voltage detect pin  COMP2 Under, over voltage detect pin  COMP1 Over voltage input  External lunder Voltage Lock Out  REG Internal regulator output  BOTT OND TOTAL OUTPUT  COMP1 BURST signal output pin for Error amplifier input ②  External capacitor from SS to GND for Soft Start Control  COMP1 Over voltage detect pin  COMP1 Over voltage detect pin  COMP1 Over voltage input  COMP1 Over voltage input  COMP1 Over voltage input  COMP1 Over voltage input  COMP1 Over voltage for HN1 output  COMP1 Over rail voltage for HN1 output  COMP1 Ower rail voltage for HN1 output  COMP1 Ower rail voltage for HN1 output	8	SRT	
adjusting the triangle oscillator    GROUND	9	RT	
External capacitor from BCT to GND for adjusting the BURST triangle oscillator  External resistor from BRT to GND for adjusting the BURST triangle oscillator  DUTY Control PWM mode and BURST mode  BURST signal output pin  BURST signal output pin  BURST signal output pin  CP External capacitor from CP to GND for Timer Latch  External capacitor from CP to GND for Timer Latch  Reference voltage input pin for Error amplifier input ©  STB Error amplifier input ©  External capacitor from SS to GND for Soft Start Control  COMP2 Under, over voltage detect pin  COMP2 Under, over voltage detect pin  COMP1 Over voltage input  External Under Voltage Lock Out  REG Internal regulator output  External regulator output  SS REG Internal regulator output  BOTT TO GND for Soft Start Control  COMP1 Over voltage detect pin  COMP2 Under, over voltage detect pin  COMP1 Over voltage input  External Under Voltage Lock Out  External regulator output  SS REG Internal regulator output  BOTT UVLO External Voltage for HN1 output  NOW SET driver	10	СТ	
adjusting the BURST triangle oscillator  External resistor from BRT to GND for adjusting the BURST triangle oscillator  DUTY Control PWM mode and BURST mode  BURST signal output pin  BURST signal output pin  BURST signal output pin  CP External capacitor from CP to GND for Timer Latch  FAIL COMP2 under voltage protect clock output  Reference voltage input pin for Error amplifier ①  VREF Reference voltage input pin for Error amplifier input ②  IS Error amplifier input ②  FB Error amplifier output  SS External capacitor from SS to GND for Soft Start Control  COMP2 Under, over voltage detect pin  COMP1 Over voltage detect pin  COMP1 Over voltage input  External Under Voltage Lock Out  REG Internal regulator output  SS BST1 Boot-Strap input for HN1 output  NMOS FET driver	11	GND	GROUND
adjusting the BURST triangle oscillator  DUTY Control PWM mode and BURST mode  BURST signal output pin  BURST signal output pin  STB Stand-by switch  CP External capacitor from CP to GND for Timer Latch  Reference voltage protect clock output  VREF Reference voltage input pin for Error amplifier ①  VS Error amplifier input ②  IS Error amplifier output  External capacitor from SS to GND for Soft Start Control  COMP2 Under, over voltage detect pin  COMP1 Over voltage detect pin  COMP1 Over voltage input  REG Internal regulator output  BST1 Boot-Strap input for HN1 output  NMOS FET driver	12	ВСТ	adjusting the BURST triangle oscillator
DUTY_OUT BURST signal output pin  STB Stand-by switch  CP External capacitor from CP to GND for Timer Latch  FAIL COMP2 under voltage protect clock output  Perference voltage input pin for Error amplifier ①  VREF Reference voltage input pin for Error amplifier ①  VS Error amplifier input ②  IS Error amplifier output  External capacitor from SS to GND for Soft Start Control  Under, over voltage detect pin  COMP1 Over voltage detect pin  COMP1 Over voltage input  REG Internal regulator output  BST1 Boot-Strap input for HN1 output  NMOS FET driver	13	BRT	
STB Stand-by switch  CP External capacitor from CP to GND for Timer Latch  FAIL COMP2 under voltage protect clock output  Perference voltage input pin for Error amplifier ①  VREF Reference voltage input pin for Error amplifier ①  VS Error amplifier input ②  IS Error amplifier output  FB Error amplifier output  SS External capacitor from SS to GND for Soft Start Control  COMP2 Under, over voltage detect pin  COMP1 Over voltage detect pin  VCC Supply voltage input  External Under Voltage Lock Out  REG Internal regulator output  SST1 Boot-Strap input for HN1 output  NMOS FET driver	14	DUTY	Control PWM mode and BURST mode
External capacitor from CP to GND for Timer Latch  18 FAIL COMP2 under voltage protect clock output  19 VREF Reference voltage input pin for Error amplifier ①  20 VS Error amplifier input ②  21 IS Error amplifier input ①  22 FB Error amplifier output  23 SS External capacitor from SS to GND for Soft Start Control  24 COMP2 Under, over voltage detect pin  25 COMP1 Over voltage detect pin  26 VCC Supply voltage input  27 UVLO External Under Voltage Lock Out  28 REG Internal regulator output  29 BST1 Boot-Strap input for HN1 output  30 SW1 Lower rail voltage for HN1 output  31 HN1 NMOS FET driver	15	DUTY_OUT	BURST signal output pin
Latch  18 FAIL COMP2 under voltage protect clock output  19 VREF Reference voltage input pin for Error amplifier ①  20 VS Error amplifier input ②  21 IS Error amplifier input ①  22 FB Error amplifier output  23 SS External capacitor from SS to GND for Soft Start Control  24 COMP2 Under, over voltage detect pin  25 COMP1 Over voltage detect pin  26 VCC Supply voltage input  27 UVLO External Under Voltage Lock Out  28 REG Internal regulator output  29 BST1 Boot-Strap input for HN1 output  30 SW1 Lower rail voltage for HN1 output  31 HN1 NMOS FET driver	16	STB	Stand-by switch
19 VREF Reference voltage input pin for Error amplifier ① 20 VS Error amplifier input ② 21 IS Error amplifier input ① 22 FB Error amplifier output 23 SS External capacitor from SS to GND for Soft Start Control 24 COMP2 Under, over voltage detect pin 25 COMP1 Over voltage detect pin 26 VCC Supply voltage input 27 UVLO External Under Voltage Lock Out 28 REG Internal regulator output 29 BST1 Boot-Strap input for HN1 output 30 SW1 Lower rail voltage for HN1 output 31 HN1 NMOS FET driver	17	СР	l
amplifier ①  WS Error amplifier input ②  IS Error amplifier input ①  Error amplifier output  Error amplifier output  SS External capacitor from SS to GND for Soft Start Control  Under, over voltage detect pin  COMP1 Over voltage detect pin  COMP1 Over voltage input  WLO External Under Voltage Lock Out  REG Internal regulator output  BST1 Boot-Strap input for HN1 output  WHO SET driver	18	FAIL	COMP2 under voltage protect clock output
21 IS Error amplifier input ① 22 FB Error amplifier output 23 SS External capacitor from SS to GND for Soft Start Control 24 COMP2 Under, over voltage detect pin 25 COMP1 Over voltage detect pin 26 VCC Supply voltage input 27 UVLO External Under Voltage Lock Out 28 REG Internal regulator output 29 BST1 Boot-Strap input for HN1 output 30 SW1 Lower rail voltage for HN1 output 31 HN1 NMOS FET driver	19	VREF	
22 FB Error amplifier output  23 SS External capacitor from SS to GND for Soft Start Control  24 COMP2 Under, over voltage detect pin  25 COMP1 Over voltage detect pin  26 VCC Supply voltage input  27 UVLO External Under Voltage Lock Out  28 REG Internal regulator output  29 BST1 Boot-Strap input for HN1 output  30 SW1 Lower rail voltage for HN1 output  31 HN1 NMOS FET driver	20	VS	Error amplifier input ②
SS External capacitor from SS to GND for Soft Start Control  Under, over voltage detect pin  COMP1 Over voltage detect pin  COMP1 Over voltage detect pin  VCC Supply voltage input  VVLO External Under Voltage Lock Out  REG Internal regulator output  BST1 Boot-Strap input for HN1 output  SW1 Lower rail voltage for HN1 output  HN1 NMOS FET driver	21	IS	Error amplifier input ①
Start Control  COMP2 Under, over voltage detect pin  COMP1 Over voltage detect pin  COMP1 Over voltage detect pin  VCC Supply voltage input  VCC Supply voltage input  External Under Voltage Lock Out  REG Internal regulator output  BST1 Boot-Strap input for HN1 output  SW1 Lower rail voltage for HN1 output  HN1 NMOS FET driver	22	FB	Error amplifier output
25 COMP1 Over voltage detect pin 26 VCC Supply voltage input 27 UVLO External Under Voltage Lock Out 28 REG Internal regulator output 29 BST1 Boot-Strap input for HN1 output 30 SW1 Lower rail voltage for HN1 output 31 HN1 NMOS FET driver	23	SS	1
26 VCC Supply voltage input 27 UVLO External Under Voltage Lock Out 28 REG Internal regulator output 29 BST1 Boot-Strap input for HN1 output 30 SW1 Lower rail voltage for HN1 output 31 HN1 NMOS FET driver	24	COMP2	Under, over voltage detect pin
27 UVLO External Under Voltage Lock Out  28 REG Internal regulator output  29 BST1 Boot-Strap input for HN1 output  30 SW1 Lower rail voltage for HN1 output  31 HN1 NMOS FET driver	25	COMP1	Over voltage detect pin
28 REG Internal regulator output 29 BST1 Boot-Strap input for HN1 output 30 SW1 Lower rail voltage for HN1 output 31 HN1 NMOS FET driver	26	VCC	Supply voltage input
29 BST1 Boot-Strap input for HN1 output 30 SW1 Lower rail voltage for HN1 output 31 HN1 NMOS FET driver	27	UVL0	External Under Voltage Lock Out
30 SW1 Lower rail voltage for HN1 output 31 HN1 NMOS FET driver	28	REG	Internal regulator output
31 HN1 NMOS FET driver	29	BST1	Boot-Strap input for HN1 output
	30	SW1	Lower rail voltage for HN1 output
32 LN1 NMOS FET driver	31	HN1	NMOS FET driver
	32	LN1	NMOS FET driver



ONOTE FOR USE

- 1. When designing the external circuit, including adequate margins for variation between external devices and IC. Use adequate margins for steady state and transient characteristics.
- 2. The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however the variation will be small.
- 3. Mounting failures, such as misdirection or miscounts, may harm the device.
- 4. A strong electromagnetic field may cause the IC to malfunction.
- 5. The GND pin should be the location within  $\pm 0.3V$  compared with the PGND pin.
- 6. BD9887FS incorporate a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation of the thermal shutdown circuit is assumed.
- 7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
- 8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
- 9. On operating Slow Start Control (SS is less than 2.2V), It does not operate Timer Latch.
- 1 0. By STB voltage, BD9887FS are changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state  $(0.8 \sim 1.4 \text{V})$ .
- 1 1. The pin connected a connector need to connect to the resistor for electrical surge destruction. This IC is a monolithic IC which (as shown is Fig-1) has P<sup>+</sup> substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows.
  - O(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)
  - O(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.

- 1 2. This IC is a monolithic IC which (as shown is Fig-1)has P<sup>+</sup> substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,
  - $\bigcirc$  (When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)
  - O(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.

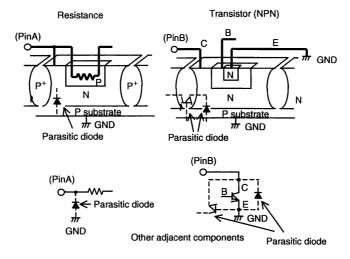


Fig-1 Simplified structure of a Bipolar IC

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