- Member of the Texas Instruments Widebus™ Family
- Undershoot Protection for Off-Isolation on A and B Ports Up To –2 V
- B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot-Plugging
- Supports PCI Hot Plug
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I_{CC} = 3 μA Max)
- V_{CC} Operating Range From 4 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

DGG, DGV, OR DL PACKAGE
(TOP VIEW)

BIASV	1	56	1$\overline{OE}$
1A1	2	55	2$\overline{OE}$
1A2	3	54	1B1
1A3	4	53	1B2
1A4	5	52	1B3
1A5	6	51	1B4
1A6	7	50	1B5
GND	8	49	GND
1A7	9	48	1B6
1A8	10	47	1B7
1A9	11	46	1B8
1A10	12	45	1B9
1A11	13	44	1B10
1A12	14	43	1B11
2A1	15	42	1B12
2A2	16	41	2B1
V_{CC}	17	40	2B2
2A3	18	39	2B3
GND	19	38	GND
2A4	20	37	2B4
2A5	21	36	2B5
2A6	22	35	2B6
2A7	23	34	2B7
2A8	24	33	2B8
2A9	25	32	2B9
2A10	26	31	2B10
2A11	27	30	2B11
2A12	28	29	2B12

description/ordering information

The SN74CBT16811C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16811C provides protection for undershoot up to –2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

Copyright © 2003, Texas Instruments Incorporated

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

1

description/ordering information (continued)

The SN74CBT16811C is organized as two 12-bit bus switches with separate output-enable (1$\overline{\text{OE}}$, 2$\overline{\text{OE}}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{\text{OE}}$ is low, the associated 12-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{\text{OE}}$ is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. The B port is precharged to BIASV through the equivalent of a 10-kΩ resistor when $\overline{\text{OE}}$ is high, or if the device is powered down (V_{CC} = 0 V).

During insertion (or removal) of a card into (or from) an active bus, the card's output voltage may be close to GND. When the connector pins make contact, the card's parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method will ensure that any glitch produced by insertion (or removal) of the card will not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube	SN74CBT16811CDL	CBT16811C
		Tape and reel	SN74CBT16811CDLR	
	TSSOP – DGG	Tube	SN74CBT16811CDGG	CBT16811C
		Tape and reel	SN74CBT16811CDGGR	
	TVSOP – DGV	Tape and reel	SN74CBT16811CDGVR	CY811C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 12-bit bus switch)

INPUT $\overline{\text{OE}}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV

![Texas Instruments logo]

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

logic diagram (positive logic)
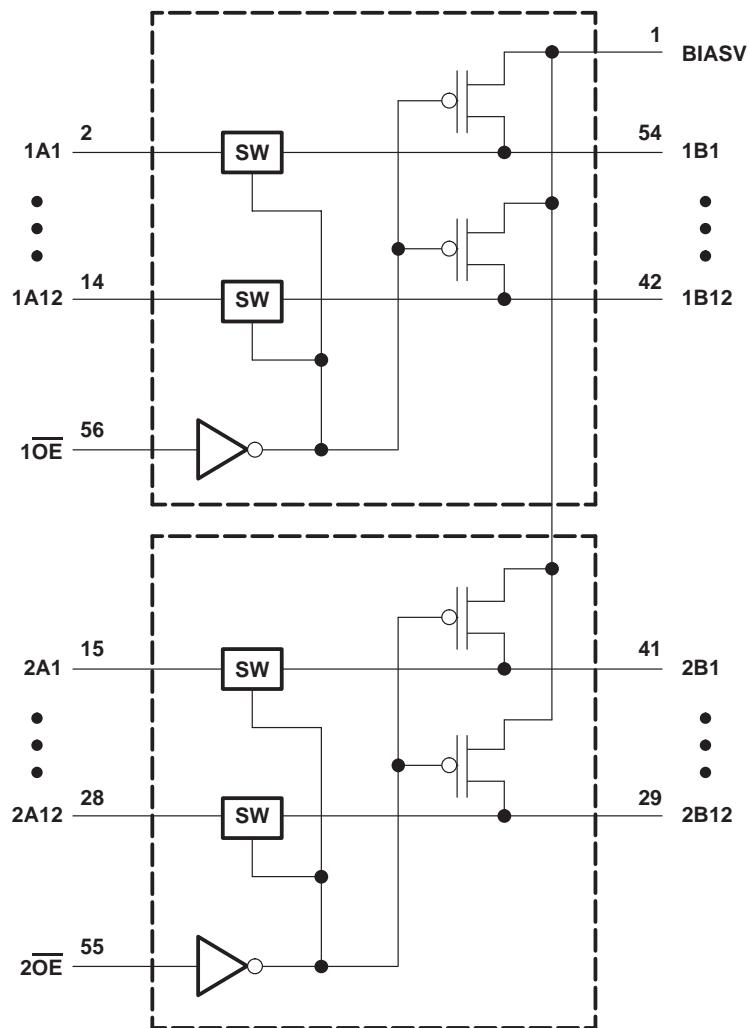
simplified schematic, each FET switch (SW)
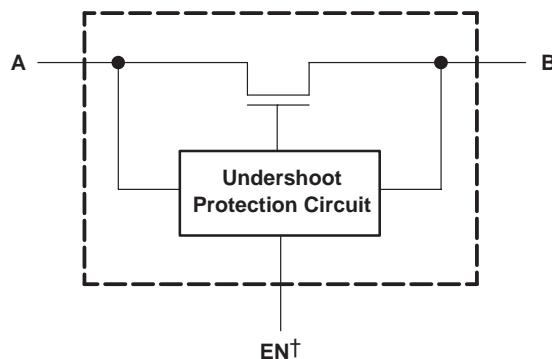
† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Bias supply voltage range, BIASV . . . . –0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . –0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . –0.5 V to 7 V
Control input clamp current, I_{IK} (V_{IN} < 0) . . . . –50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0) . . . . –50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . ±128 mA
Continuous current through V_{CC} or GND terminals . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DGG package . . . . 64°C/W
DGV package . . . . 48°C/W
DL package . . . . 56°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Bias supply voltage	0	V_{CC}	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	–40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. BIASV is a supply voltage, not a control input.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = –18 mA				–1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ –50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			–2	V
$V_{O(USP)}$[‡]		V_{CC} = BIASV = 5 V,	I_I = –10 mA, V_{IN} = V_{CC} or GND,	Switch OFF	3			V
V_O	B port	V_{CC} = 0 V,	BIASV = V_X,	I_O = 0	V_X–0.1		V_X	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	µA
I_O	B port	V_{CC} = 4.5 V,	BIASV = 2.4 V, V_O = 0,	Switch OFF, V_{IN} = V_{CC} or GND		0.25		mA
I_{OZ}[§]		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	µA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	µA
ΔI_{CC}[¶]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0					4.5	pF
$C_{io(OFF)}$	A port	$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND			5.5	pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND			15.5	pF
r_{on}[#]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = –15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = –15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
[‡] $V_{O(USP)}$ = A-port undershoot static protection.
[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.
[¶] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}[‖]		A or B	B or A		0.24		0.15	ns
t_{PZH}	BIASV = GND	$\overline{OE}$	A or B		6.5	1.5	6	ns
t_{PZL}	BIASV = 3 V				6.5	1.5	6	
t_{PHZ}	BIASV = GND	$\overline{OE}$	A or B		6.5	1.5	6	ns
t_{PLZ}	BIASV = 3 V				6.5	1.5	6	

[‖] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION
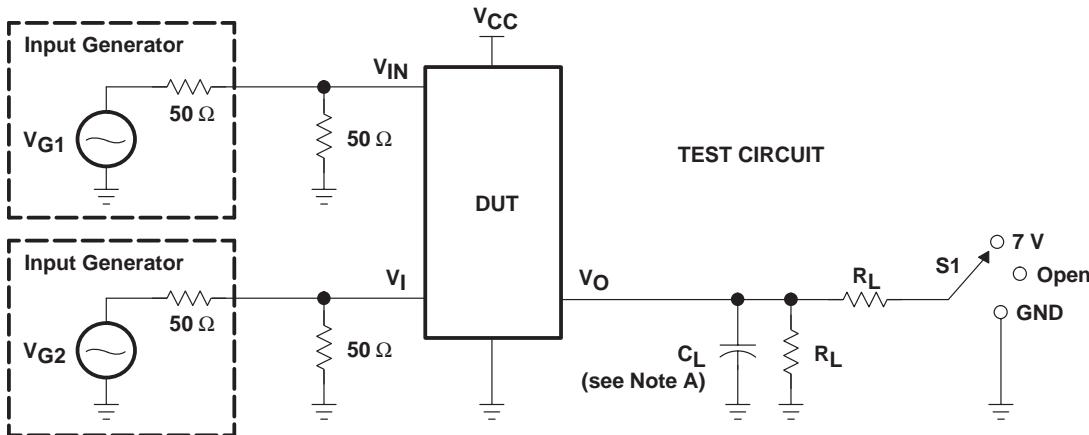
TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V $\pm$ 0.5 V	Open	500 Ω	V_{CC} or GND	50 pF	
	4 V	Open	500 Ω	V_{CC} or GND	50 pF	
t_{PLZ}/t_{PZL}	5 V $\pm$ 0.5 V	7 V	500 Ω	GND	50 pF	0.3 V
	4 V	7 V	500 Ω	GND	50 pF	0.3 V
t_{PHZ}/t_{PZH}	5 V $\pm$ 0.5 V	Open	500 Ω	V_{CC}	50 pF	0.3 V
	4 V	Open	500 Ω	V_{CC}	50 pF	0.3 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)
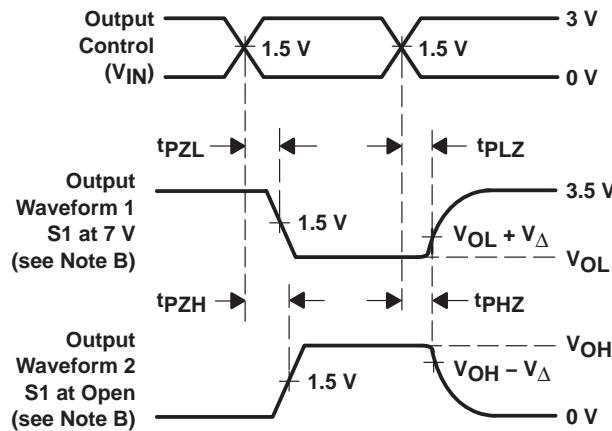
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Test Circuit and Voltage Waveforms

![Texas Instruments logo]
TEXAS
INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74CBT16811CDGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT16811CDGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16811CDGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16811CDGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16811CDLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16811CDLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN
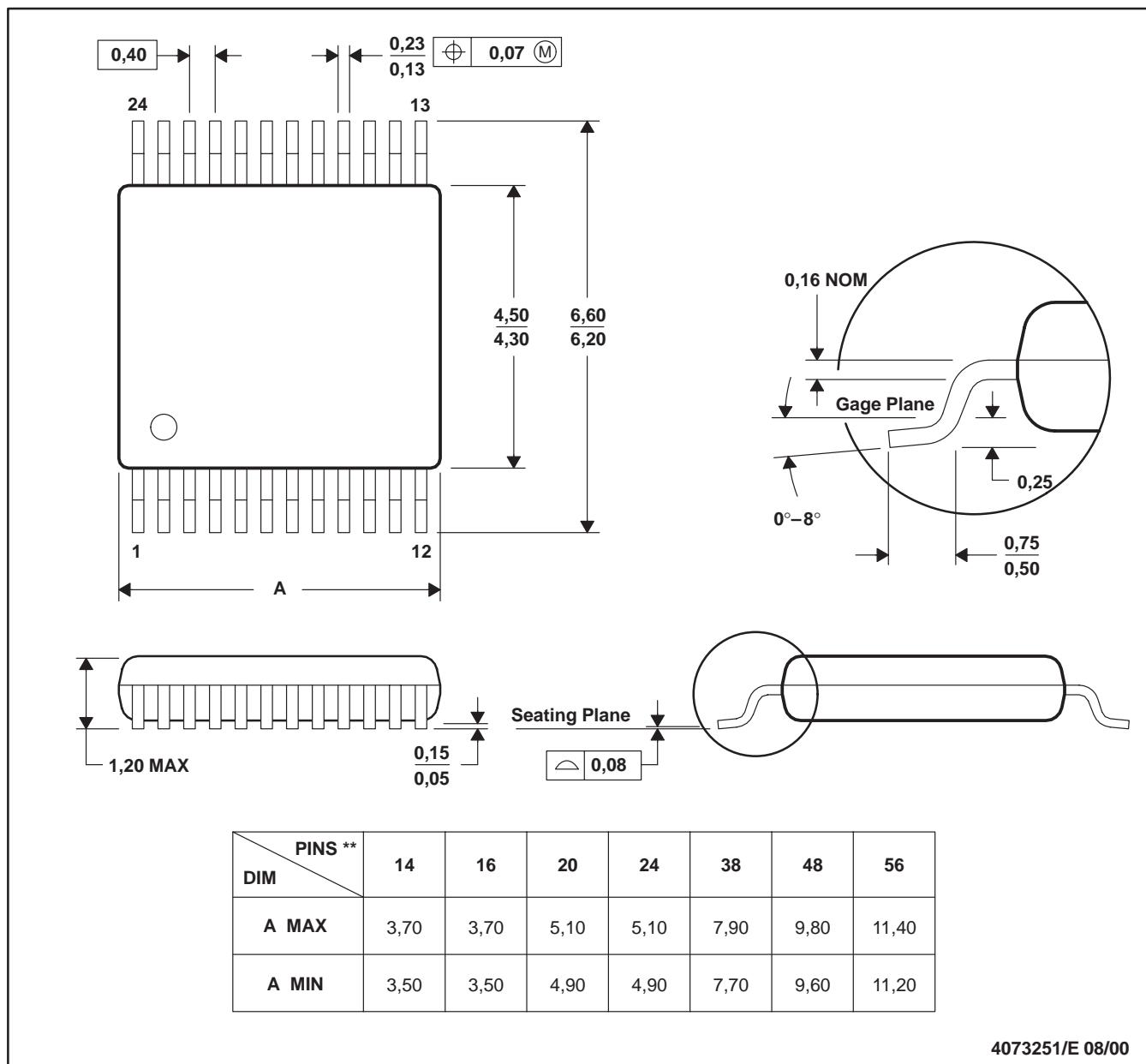
| PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
             B. This drawing is subject to change without notice.
             C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
             D. Falls within JEDEC: 24/48 Pins – MO-153
                                    14/16/20/56 Pins – MO-194

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

DL (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

	PINS **	28	48	56
DIM				
A MAX		0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN		0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01
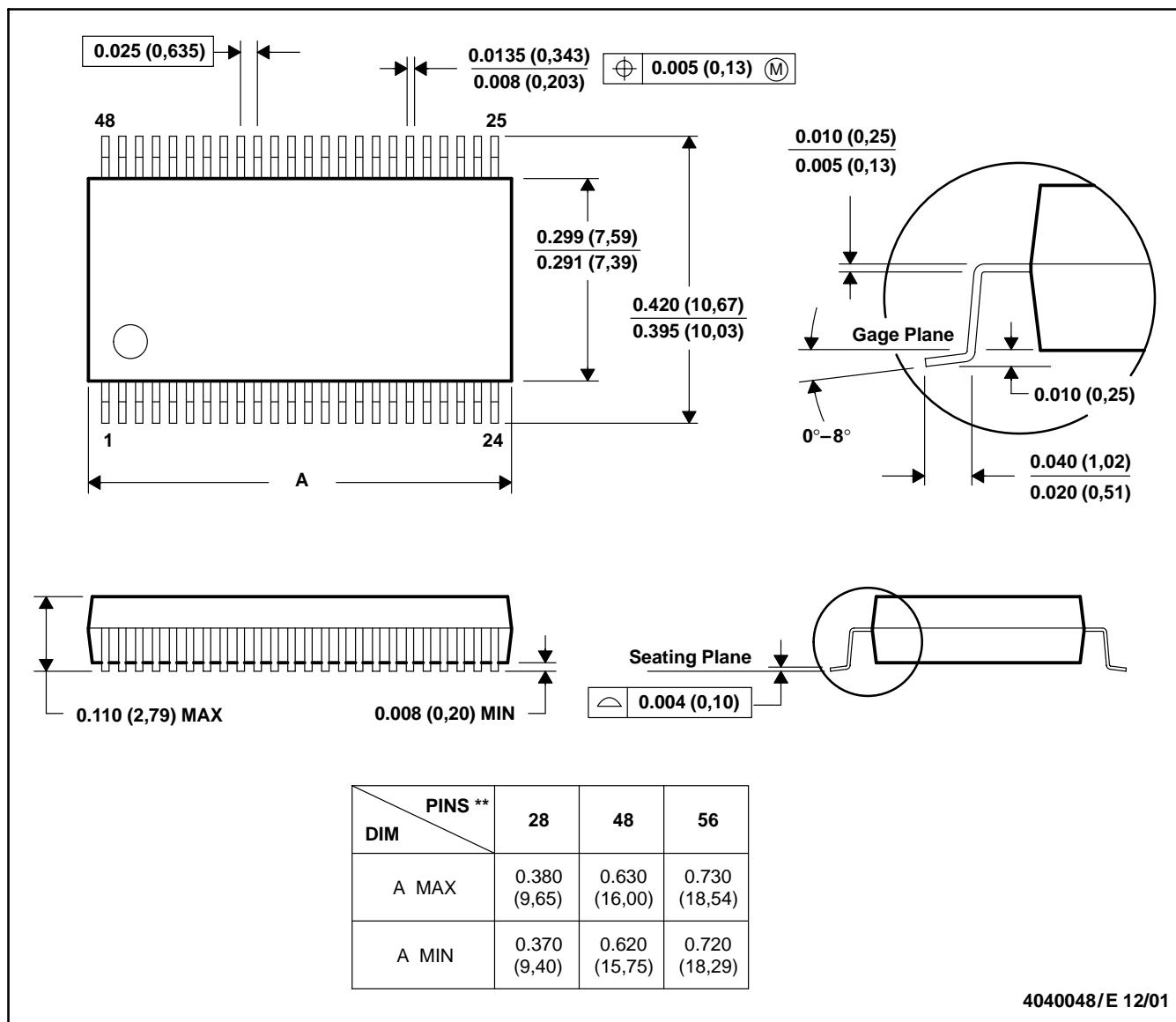
NOTES: A. All linear dimensions are in inches (millimeters).
       B. This drawing is subject to change without notice.
       C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
       D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**
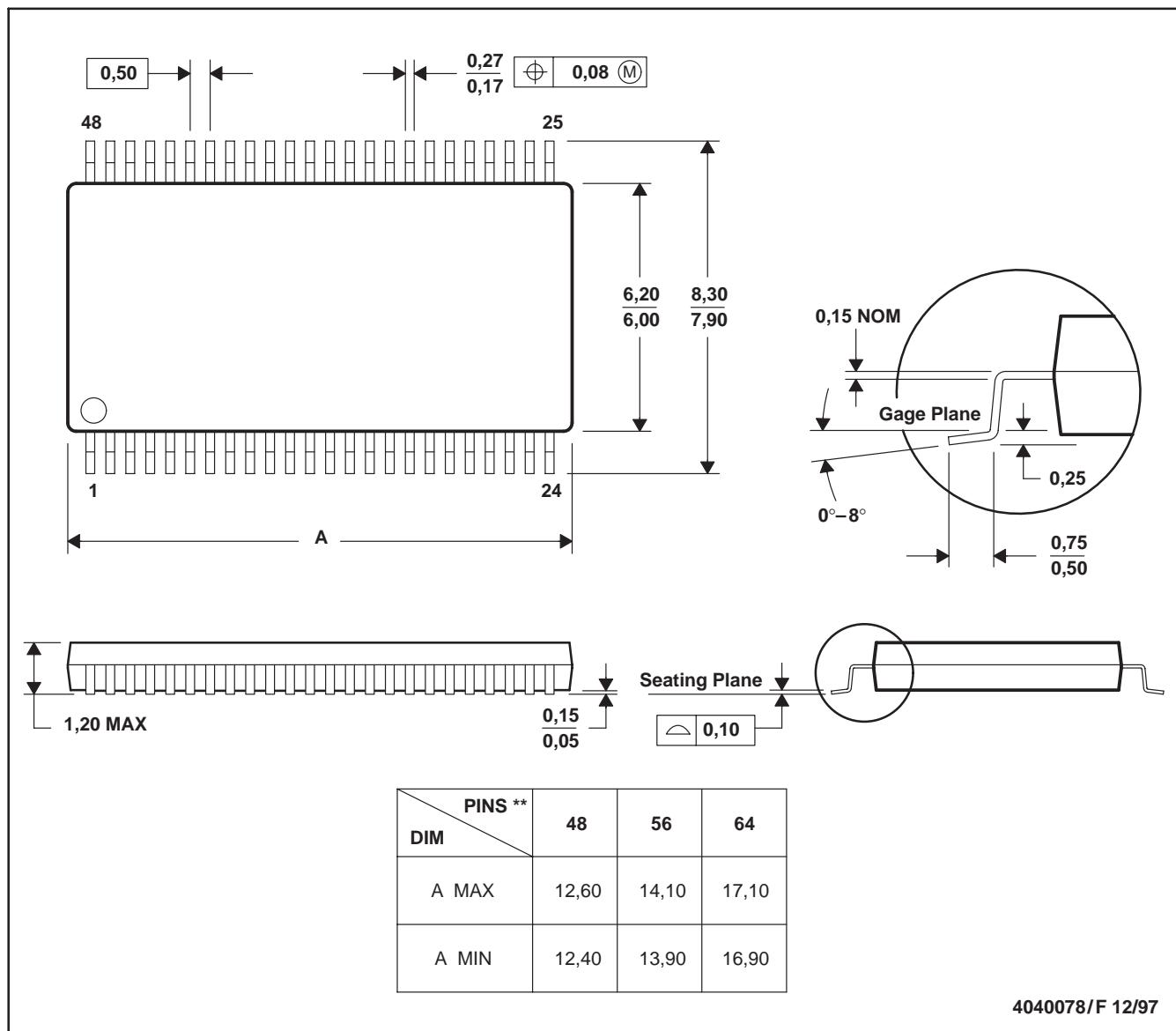
48 PINS SHOWN

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold protrusion not to exceed 0,15.
   D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
                     Post Office Box 655303 Dallas, Texas 75265