

# Ultra-Small, Rail-to-Rail I/O with Disable, Single-/Dual-Supply, Low-Power Op Amps

## General Description

The MAX4245/MAX4246/MAX4247 family of low-cost op amps offer rail-to-rail inputs and outputs, draw only 320 $\mu$ A of quiescent current, and operate from a single +2.5V to +5.5V supply. For additional power conservation, the MAX4245/MAX4247 offer a low-power shutdown mode that reduces supply current to 50nA, and puts the amplifiers' outputs in a high-impedance state. These devices are unity-gain stable with a 1MHz gain-bandwidth product driving capacitive loads up to 470pF.

The MAX4245/MAX4246/MAX4247 family is specified from -40°C to +125°C, making them suitable for use in a variety of harsh environments, such as automotive applications. The MAX4245 single amplifier is available in ultra-small 6-pin SC70 and space-saving 6-pin SOT23 packages. The MAX4246 dual amplifier is available in 8-pin SOT23, SO, and  $\mu$ MAX® packages. The MAX4247 dual amplifier comes in a tiny 10-pin  $\mu$ MAX package.

## Applications

Portable Communications  
Single-Supply Zero-Crossing Detectors  
Instruments and Terminals  
Electronic Ignition Modules  
Infrared Receivers  
Sensor-Signal Detection

## Features

- ◆ Rail-to-Rail Input and Output Voltage Swing
- ◆ 50nA (max) Shutdown Mode (MAX4245/MAX4247)
- ◆ 320 $\mu$ A (typ) Quiescent Current Per Amplifier
- ◆ Single +2.5V to +5.5V Supply Voltage Range
- ◆ 110dB Open-Loop Gain with 2k $\Omega$  Load
- ◆ 0.01% THD with 100k $\Omega$  Load
- ◆ Unity-Gain Stable up to C<sub>LOAD</sub> = 470pF
- ◆ No Phase Inversion for Overdriven Inputs
- ◆ Available in Space-Saving Packages  
6-Pin SC70 or 6-Pin SOT23 (MAX4245)  
8-Pin SOT23/SO or 8-Pin  $\mu$ MAX (MAX4246)  
10-Pin  $\mu$ MAX (MAX4247)

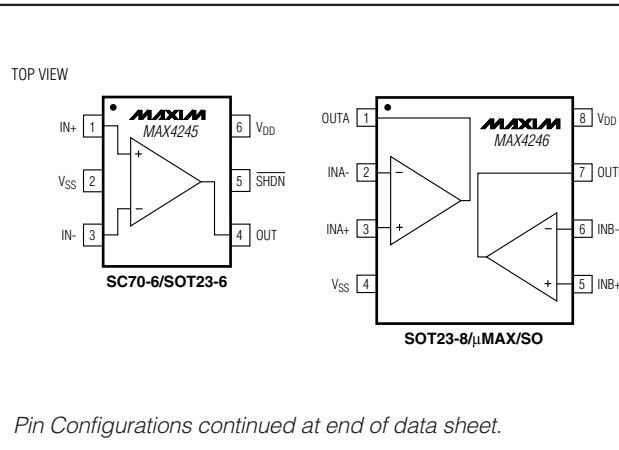
## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
<b>MAX4245AXT-T</b>	-40°C to +125°C	6 SC70-6	AAZ
MAX4245AUT-T	-40°C to +125°C	6 SOT23-6	AAUB
<b>MAX4246AKA-T</b>	-40°C to +125°C	8 SOT23-8	AAIN
MAX4246ASA	-40°C to +125°C	8 SO	—
MAX4246AUA	-40°C to +125°C	8 $\mu$ MAX	—
<b>MAX4247AUB</b>	-40°C to +125°C	10 $\mu$ MAX	—

## Selector Guide

PART	AMPLIFIERS PER PACKAGE	SHUTDOWN MODE
MAX4245AXT-T	1	Yes
MAX4245AUT-T	1	Yes
MAX4246AKA-T	2	No
MAX4246ASA	2	No
MAX4246AUA	2	No
MAX4247AUB	2	Yes

## Pin Configurations



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## ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V <sub>DD</sub> to V <sub>SS</sub> )	-0.3V to +6V
All Other Pins	(V <sub>SS</sub> - 0.3V) to (V <sub>DD</sub> + 0.3V)
Output Short-Circuit Duration (OUT shorted to V <sub>SS</sub> or V <sub>DD</sub> )	Continuous
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
6-Pin SC70 (derate 3.1mW/°C above +70°C)	245mW
6-Pin SOT23 (derate 8.7mW/°C above +70°C)	695mW
8-Pin SO (derate 5.9mW/°C above +70°C)	471mW

8-Pin SOT23 (derate 9.1mW/°C above +70°C)	727mW
8-Pin μMAX (derate 4.5mW/°C above +70°C)	362mW
10-Pin μMAX (derate 5.6mW/°C above +70°C)	444mW
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +2.7V, V<sub>SS</sub> = 0V, V<sub>CM</sub> = 0V, V<sub>OUT</sub> = V<sub>DD</sub> / 2, R<sub>L</sub> connected from OUT to V<sub>DD</sub> / 2,  $\overline{\text{SHDN}_-}$  = V<sub>DD</sub> (MAX4245/MAX4247 only), T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V <sub>DD</sub>	Inferred from PSRR test	2.5	5.5	5.5	V
Supply Current (Per Amplifier)	I <sub>DD</sub>	V <sub>DD</sub> = +2.7V	320	650	650	μA
		V <sub>DD</sub> = +5.5V	375	700	700	
Supply Current in Shutdown	I $\overline{\text{SHDN}_-}$	$\overline{\text{SHDN}_-}$ = V <sub>SS</sub> (Note 2)	0.05	0.5	0.5	μA
Input Offset Voltage	V <sub>OS</sub>	V <sub>SS</sub> - 0.1V ≤ V <sub>CM</sub> ≤ V <sub>DD</sub> + 0.1V	±0.4	±1.5	±1.5	mV
Input Bias Current	I <sub>B</sub>	V <sub>SS</sub> - 0.1V ≤ V <sub>CM</sub> ≤ V <sub>DD</sub> + 0.1V	±10	±50	±50	nA
Input Offset Current	I <sub>OS</sub>	V <sub>SS</sub> - 0.1V ≤ V <sub>CM</sub> ≤ V <sub>DD</sub> + 0.1V	±1	±6	±6	nA
Input Resistance	R <sub>IN</sub>	V <sub>IN+</sub> - V <sub>IN-</sub>   ≤ 10mV	4000		4000	kΩ
Input Common-Mode Voltage Range	V <sub>CM</sub>	Inferred from CMRR test	V <sub>SS</sub> - 0.1	V <sub>DD</sub> + 0.1	V <sub>DD</sub> + 0.1	V
Common-Mode Rejection Ratio	CMRR	V <sub>SS</sub> - 0.1V ≤ V <sub>CM</sub> ≤ V <sub>DD</sub> + 0.1V	65	80	80	dB
Power-Supply Rejection Ratio	PSRR	2.5V ≤ V <sub>DD</sub> ≤ 5.5V	75	90	90	dB
Large-Signal Voltage Gain	A <sub>V</sub>	V <sub>SS</sub> + 0.05V ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> - 0.05V, R <sub>L</sub> = 100kΩ	120	120	120	dB
		V <sub>SS</sub> + 0.2V ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> - 0.2V, R <sub>L</sub> = 2kΩ	95	110	110	
Output Voltage Swing High	V <sub>OH</sub>	Specified as V <sub>DD</sub> - V <sub>OUT</sub>	R <sub>L</sub> = 100kΩ	1	1	mV
			R <sub>L</sub> = 2kΩ	35	60	
Output Voltage Swing Low	V <sub>OL</sub>	Specified as V <sub>OUT</sub> - V <sub>SS</sub>	R <sub>L</sub> = 100kΩ	1	1	mV
			R <sub>L</sub> = 2kΩ	30	60	
Output Short-Circuit Current	I <sub>OUT(SC)</sub>	V <sub>DD</sub> = +5.0V	Sourcing	11	11	mA
			Sinking	30	30	
Output Leakage Current in Shutdown	I <sub>OUT(SH)</sub>	Device in Shutdown Mode ( $\overline{\text{SHDN}_-}$ = V <sub>SS</sub> ), V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> (Note 2)	±0.01	±0.5	±0.5	μA
SHDN <sub>-</sub> Logic Low	V <sub>IL</sub>	(Note 2)		0.3 × V <sub>DD</sub>	0.3 × V <sub>DD</sub>	V
SHDN <sub>-</sub> Logic High	V <sub>IH</sub>	(Note 2)		0.7 × V <sub>DD</sub>	0.7 × V <sub>DD</sub>	V
SHDN <sub>-</sub> Input Current	I <sub>L/IH</sub>	V <sub>SS</sub> ≤ $\overline{\text{SHDN}_-}$ ≤ V <sub>DD</sub> (Note 2)	0.5	50	50	nA

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +2.7V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = V_{DD} / 2$ ,  $R_L$  connected from OUT to  $V_{DD} / 2$ ,  $\overline{SHDN}_- = V_{DD}$  (MAX4245/MAX4247 only),  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBW			1.0		MHz
Phase Margin	$\phi_M$			70		degrees
Gain Margin	$G_M$			20		dB
Slew Rate	SR			0.4		V/ $\mu$ s
Input Voltage-Noise Density	$e_n$	$f = 10\text{kHz}$		52		nV/ $\sqrt{\text{Hz}}$
Input Current-Noise Density	$i_n$	$f = 10\text{kHz}$		0.1		pA/ $\sqrt{\text{Hz}}$
Capacitive-Load Stability	$C_{LOAD}$	$A_V = 1$ (Note 3)			470	pF
Shutdown Delay Time	$t_{(SH)}$	(Note 2)		3		$\mu$ s
Enable Delay Time	$t_{(EN)}$	(Note 2)		4		$\mu$ s
Power-On Time	$t_{ON}$			4		$\mu$ s
Input Capacitance	$C_{IN}$			2.5		pF
Total Harmonic Distortion	THD	$f = 10\text{kHz}$ , $V_{OUT} = 2\text{Vp-p}$ , $A_V = +1$ , $V_{DD} = +5.0V$ , Load = $100\text{k}\Omega$ to $V_{DD}/2$		0.01		%
Settling Time to 0.01%	$t_s$	$V_{OUT} = 4\text{V}$ step, $V_{DD} = +5.0V$ , $A_V = +1$		10		$\mu$ s

## ELECTRICAL CHARACTERISTICS

( $V_{DD} = +2.7V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = V_{DD} / 2$ ,  $R_L$  connected from OUT to  $V_{DD} / 2$ ,  $\overline{SHDN}_- = V_{DD}$  (MAX4245/MAX4247 only),  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	$V_{DD}$	Inferred from PSRR test	2.5	5.5		V
Supply Current (Per Amplifier)	$I_{DD}$	$V_{DD} = +2.7V$		800		$\mu$ A
Supply Current in Shutdown	$I_{\overline{SHDN}_-}$	$\overline{SHDN}_- = V_{SS}$ (Note 2)		1		$\mu$ A
Input Offset Voltage	$V_{OS}$	$V_{SS} \leq V_{CM} \leq V_{DD}$ (Note 4)		$\pm 3.0$		mV
Input Offset Voltage Drift	$TCV_{OS}$	$V_{SS} \leq V_{CM} \leq V_{DD}$ (Note 4)		$\pm 2$		$\mu\text{V}/^\circ C$
Input Bias Current	$I_B$	$V_{SS} \leq V_{CM} \leq V_{DD}$ (Note 4)		$\pm 100$		nA
Input Offset Current	$I_{OS}$	$V_{SS} \leq V_{CM} \leq V_{DD}$ (Note 4)		$\pm 10$		nA
Input Common-Mode Voltage Range	$V_{CM}$	Inferred from CMRR test (Note 4)	$V_{SS}$	$V_{DD}$		V
Common-Mode Rejection Ratio	CMRR	$V_{SS} \leq V_{CM} \leq V_{DD}$ (Note 4)	60			dB
Power-Supply Rejection Ratio	PSRR	$2.5V \leq V_{DD} \leq 5.5V$	70			dB
Large-Signal Voltage Gain	$A_V$	$V_{SS} + 0.2V \leq V_{OUT} \leq V_{DD} - 0.2V$ , $R_L = 2\text{k}\Omega$	85			dB
Output Voltage Swing High	$V_{OH}$	Specified as $V_{DD} - V_{OUT}$ , $R_L = 2\text{k}\Omega$		90		mV
Output Voltage Swing Low	$V_{OL}$	Specified as $V_{OUT} - V_{SS}$ , $R_L = 2\text{k}\Omega$		90		mV
Output Leakage Current in Shutdown	$I_{OUT(SH)}$	Device in Shutdown Mode ( $\overline{SHDN}_- = V_{SS}$ ), $V_{SS} \leq V_{OUT} \leq V_{DD}$ (Note 3)		$\pm 1.0$		$\mu$ A

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +2.7V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = V_{DD} / 2$ ,  $R_L$  connected from OUT to  $V_{DD} / 2$ ,  $\overline{SHDN}_- = V_{DD}$  (MAX4245/MAX4247 only),  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SHDN <sub>-</sub> Logic Low	V <sub>IL</sub>	(Note 2)			$0.3 \times V_{DD}$	V
SHDN <sub>-</sub> Logic High	V <sub>IH</sub>	(Note 2)			$0.7 \times V_{DD}$	V
SHDN <sub>-</sub> Input Current	I <sub>L/IH</sub>	$V_{SS} \leq \overline{SHDN}_- \leq V_{DD}$ (Notes 2, 3)			100	nA

**Note 1:** Specifications are 100% tested at  $T_A = +25^\circ C$ . All temperature limits are guaranteed by design.

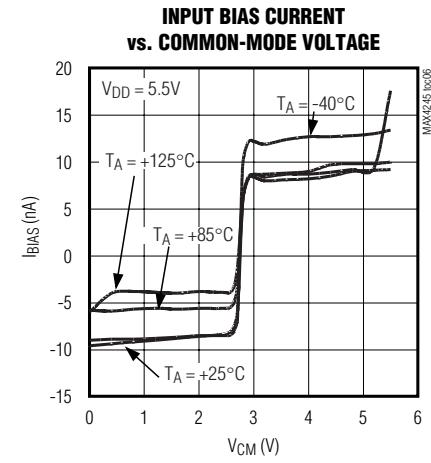
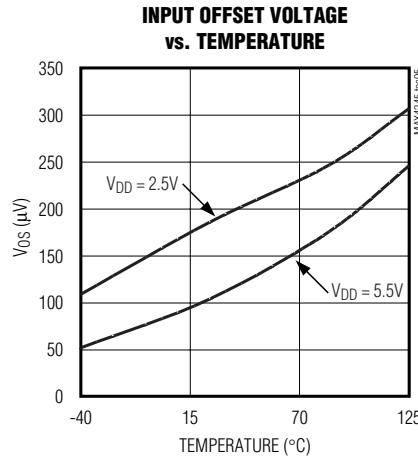
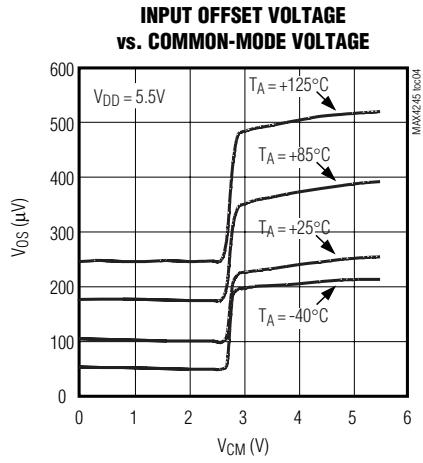
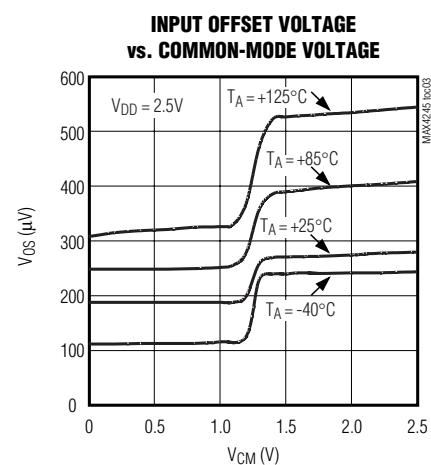
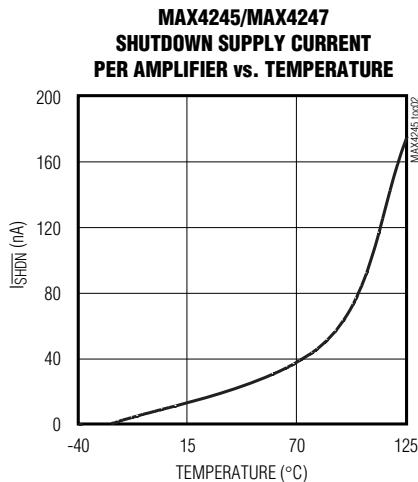
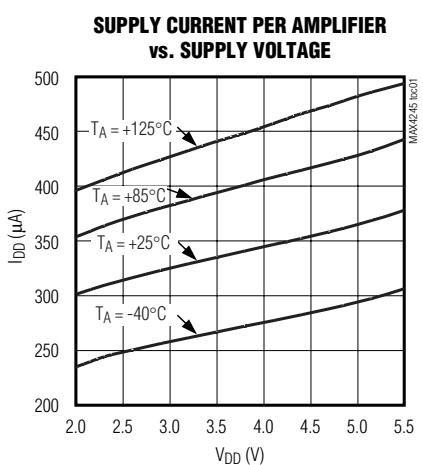
**Note 2:** Shutdown mode is only available in MAX4245 and MAX4247.

**Note 3:** Guaranteed by design, not production tested.

**Note 4:** For  $-40^\circ C$  to  $+85^\circ C$ , Input Common-Mode Range is  $V_{SS} - 0.1V \leq V_{CM} \leq V_{DD} + 0.1V$ .

## Typical Operating Characteristics

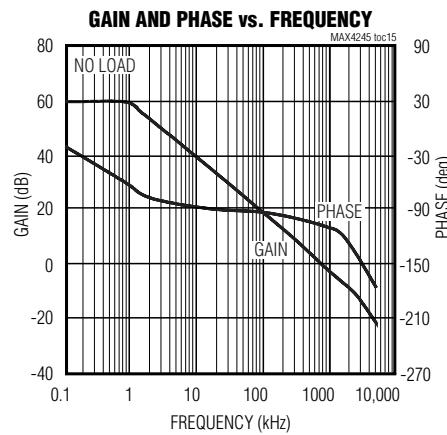
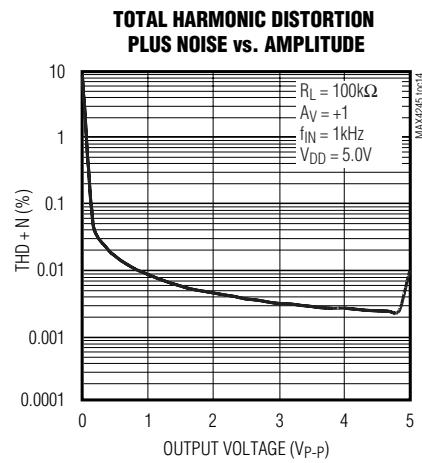
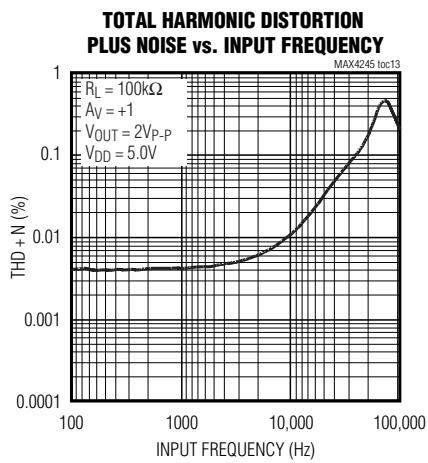
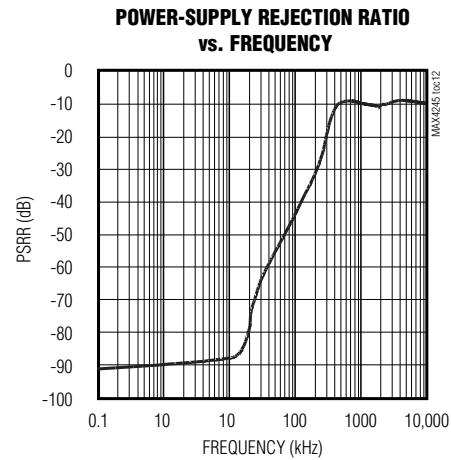
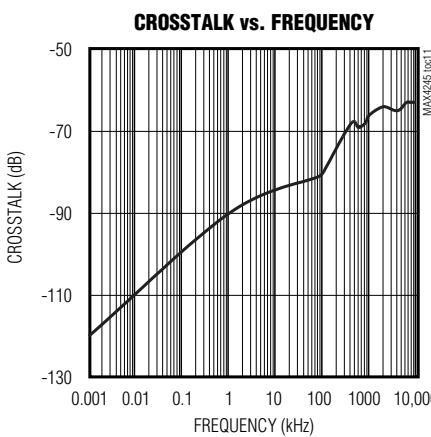
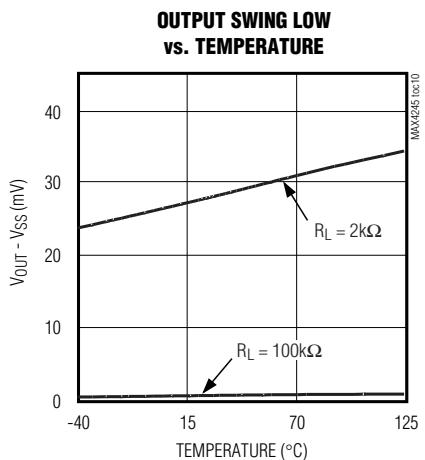
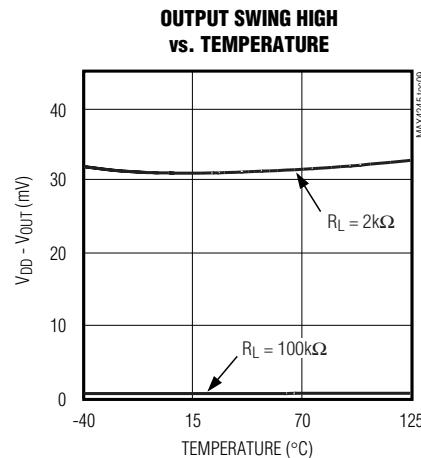
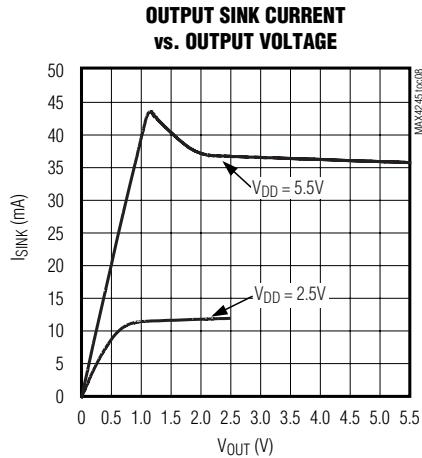
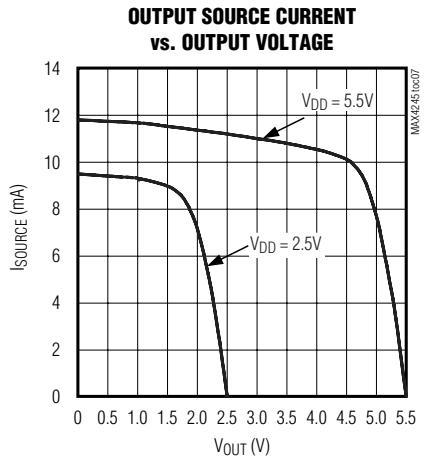
( $V_{DD} = 2.7V$ ,  $V_{SS} = V_{CM} = 0V$ ,  $V_{OUT} = V_{DD} / 2$ , no load,  $T_A = +25^\circ C$ , unless otherwise noted.)



# Ultra-Small, Rail-to-Rail I/O with Disable, Single-/Dual-Supply, Low-Power Op Amps

## Typical Operating Characteristics (continued)

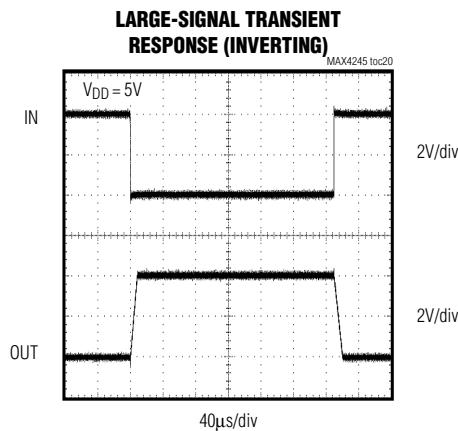
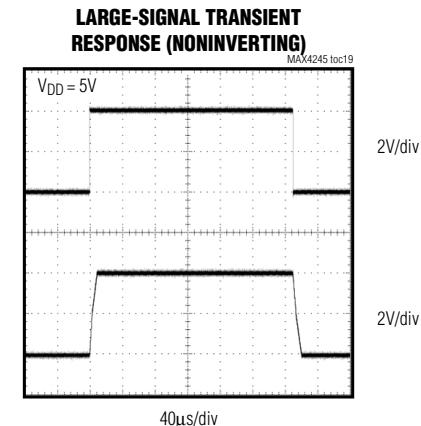
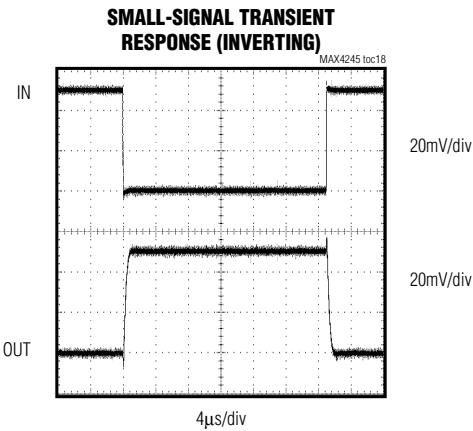
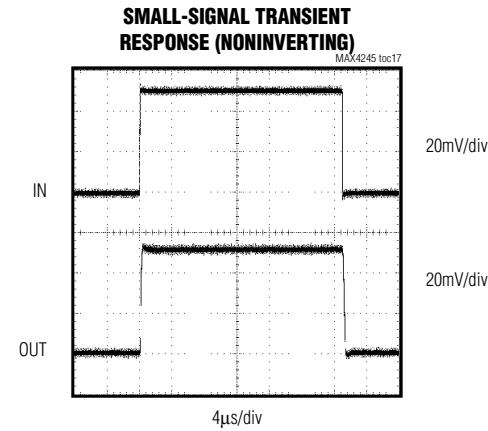
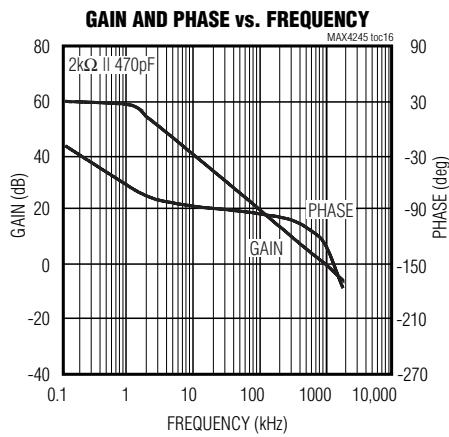
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## Typical Operating Characteristics (continued)

( $V_{DD} = 2.7V$ ,  $V_{SS} = V_{CM} = 0V$ ,  $V_{OUT} = V_{DD} / 2$ , no load,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



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## Pin Description

PIN			NAME	FUNCTION
MAX4245	MAX4246	MAX4247		
1	—	—	IN+	Noninverting Input
2	4	4	Vss	Ground or Negative Supply
3	—	—	IN-	Inverting Input
4	—	—	OUT	Amplifier Output
5	—	—	SHDN	Shutdown
6	8	10	VDD	Positive Supply
—	1	1	OUTA	Amplifier Output Channel A
—	2	2	INA-	Inverting Input Channel A
—	3	3	INA+	Noninverting Input Channel A
—	5	7	INB+	Noninverting Input Channel B
—	6	8	INB-	Inverting Input Channel B
—	7	9	OUTB	Amplifier Output Channel B
—	—	5	SHDNA	Shutdown Channel A
—	—	6	SHDNB	Shutdown Channel B

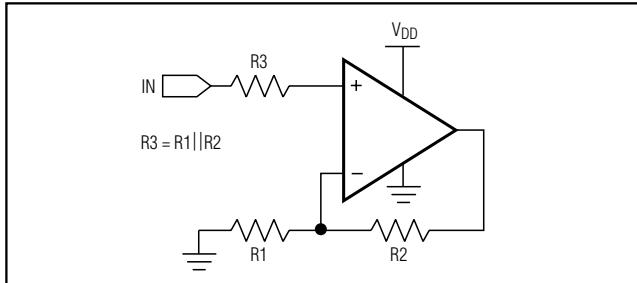


Figure 1a. Minimizing Offset Error Due to Input Bias Current (Noninverting)

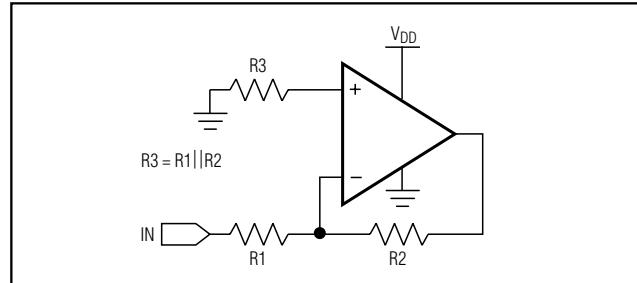


Figure 1b. Minimizing Offset Error Due to Input Bias Current (Inverting)

## Detailed Description

### Rail-to-Rail Input Stage

The MAX4245/MAX4246/MAX4247 have rail-to-rail input and output stages that are specifically designed for low-voltage, single-supply operation. The input stage consists of composite NPN and PNP differential stages, which operate together to provide a common-mode range extending to both supply rails. The crossover region of these two pairs occurs halfway between V<sub>DD</sub> and V<sub>SS</sub>. The input offset voltage is typically  $\pm 400\mu\text{V}$ . Low-operating supply voltage, low supply current and rail-to-rail outputs make this family of operational amplifiers an excellent choice for precision or general-purpose, low-voltage, battery-powered systems.

Since the input stage consists of NPN and PNP pairs, the input bias current changes polarity as the common-

mode voltage passes through the crossover region. Match the effective impedance seen by each input to reduce the offset error caused by input bias currents flowing through external source impedance (Figures 1a and 1b).

The combination of high-source impedance plus input capacitance (amplifier input capacitance plus stray capacitance) creates a parasitic pole that can produce an underdamped signal response. Reducing input capacitance or placing a small capacitor across the feedback resistor improves response in this case.

The MAX4245/MAX4246/MAX4247 family's inputs are protected from large differential input voltages by internal 5.3k $\Omega$  series resistors and back-to-back triple-diode stacks across the inputs (Figure 2). For differential-input voltages much less than 2.1V (triple-diode drop),

MAX4245/MAX4246/MAX4247

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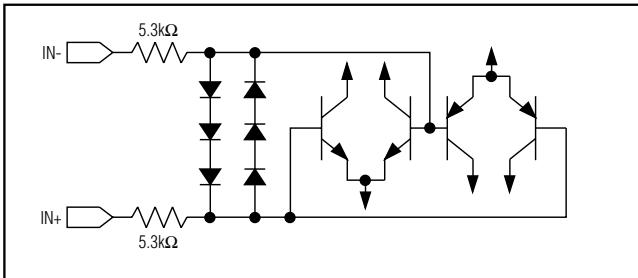


Figure 2. Input Protection Circuit

input resistance is typically  $4\text{M}\Omega$ . For differential voltages greater than 2.1V, input resistance is around  $10.6\text{k}\Omega$ , and the input bias current can be approximated by the following equation:

$$I_B = (V_{\text{DIFF}} - 2.1\text{V}) / 10.6\text{k}\Omega$$

In the region where the differential input voltage approaches 2.1V, the input resistance decreases exponentially from  $4\text{M}\Omega$  to  $10.6\text{k}\Omega$  as the diodes begin to conduct. It follows that the bias current increases with the same curve.

In unity-gain configuration, high slew-rate input signals may capacitively couple to the output through the triple-diode stacks.

## Rail-to-Rail Output Stage

The MAX4245/MAX4246/MAX4247 can drive a  $2\text{k}\Omega$  load and still typically swing within 35mV of the supply rails. Figure 3 shows the output voltage swing of the MAX4245 configured with  $A_V = -1\text{V/V}$ .

## Applications Information

### Power-Supply Considerations

The MAX4245/MAX4246/MAX4247 operate from a single  $+2.5\text{V}$  to  $+5.5\text{V}$  supply (or dual  $\pm 1.25\text{V}$  to  $\pm 2.75\text{V}$  supplies) and consume only  $320\mu\text{A}$  of supply current per amplifier. A 90dB power-supply rejection ratio allows the amplifiers to be powered directly off a decaying battery voltage, simplifying design and extending battery life.

### Power-Up

The MAX4245/MAX4246/MAX4247 output typically settles within  $4\mu\text{s}$  after power-up. Figure 4 shows the output voltage on power-up and power-down.

### Shutdown Mode

The MAX4245/MAX4247 feature a low-power shutdown mode. When SHDN is pulled low, the supply current drops to  $50\text{nA}$  per amplifier, the amplifier is disabled, and the output enters a high-impedance state. Pulling

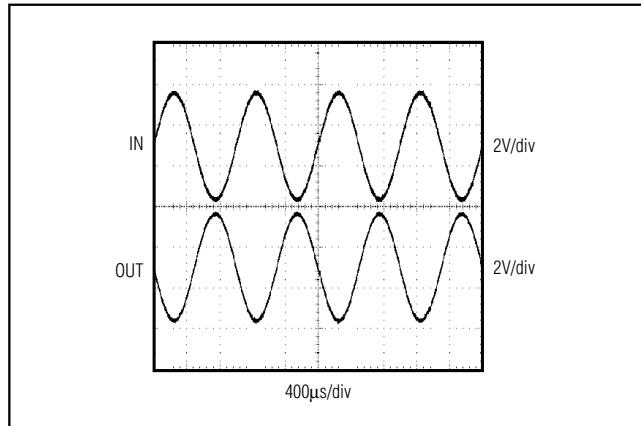


Figure 3. Rail-to-Rail Input/Output Voltage Range

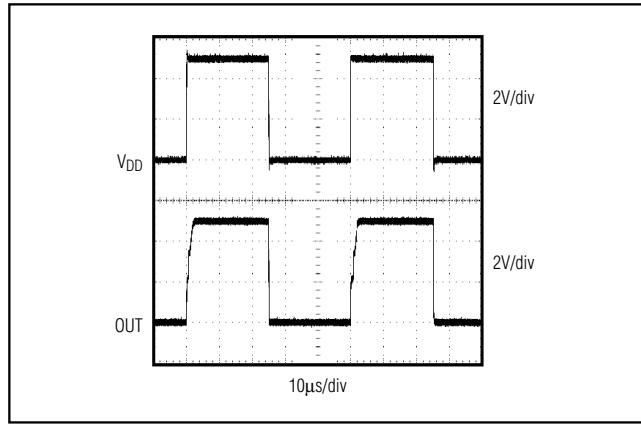


Figure 4. Power-Up/Power-Down Waveform

SHDN high enables the amplifier. Figure 5 shows the MAX4245/MAX4247's shutdown waveform.

Due to the output leakage currents of three-state devices and the small internal pullup current for SHDN, do not let the SHDN float. Floating SHDN may result in indeterminate logic levels, and could adversely affect op amp operation. The logic threshold for SHDN is referred to Vss. When using dual supplies, pull SHDN to Vss, not GND, to shut down the op amp.

### Driving Capacitive Loads

The MAX4245/MAX4246/MAX4247 are unity-gain stable for loads up to  $470\text{pF}$ . Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load

# Ultra-Small, Rail-to-Rail I/O with Disable, Single-/Dual-Supply, Low-Power Op Amps

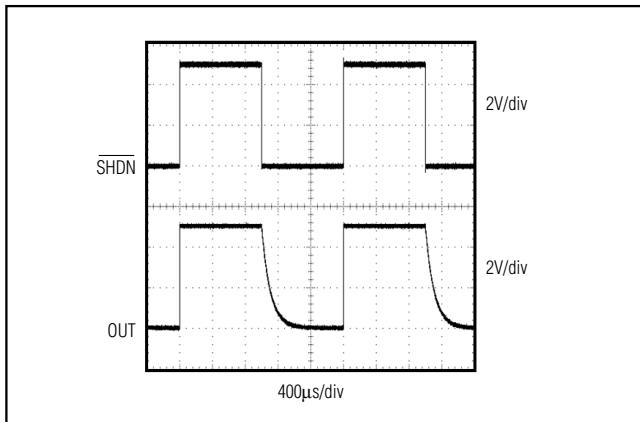


Figure 5. Shutdown Waveform

(Figures 6a, 6b, 6c). Note that this alternative results in a loss of gain accuracy because  $R_{ISO}$  forms a voltage divider with the  $R_{LOAD}$ .

### Power-Supply Bypassing and Layout

The MAX4245/MAX4246/MAX4247 family operates from either a single +2.5V to +5.5V supply or dual  $\pm 1.25V$  to  $\pm 2.75V$  supplies. For single-supply operation, bypass the power supply with a 100nF capacitor to Vss (in this case GND). For dual-supply operation, both the VDD and the Vss supplies should be bypassed to ground with separate 100nF capacitors.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components when possible.

### Pin Configurations (continued)

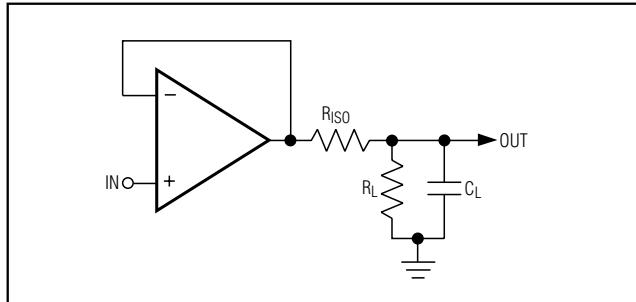
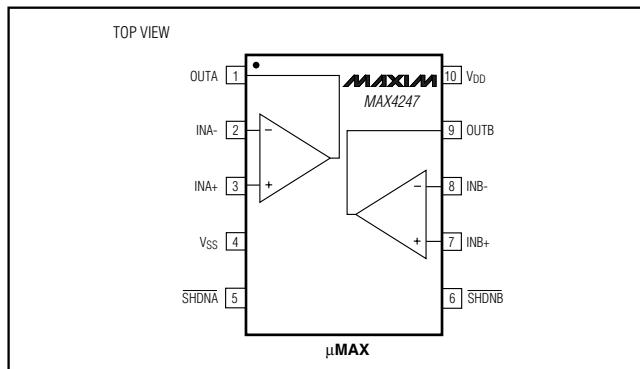


Figure 6a. Using a Resistor to Isolate a Capacitive Load from the Op Amp

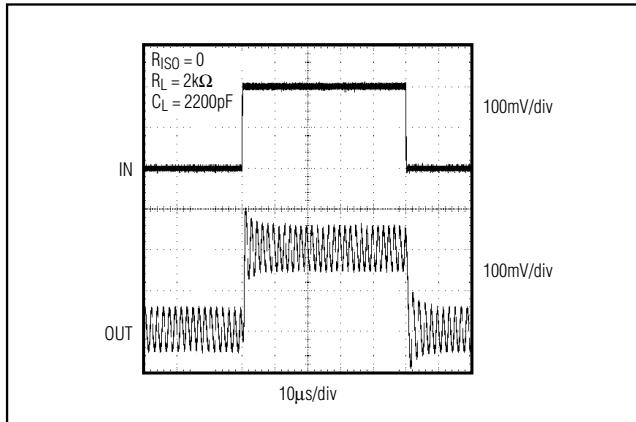


Figure 6b. Pulse Response Without Isolating Resistor

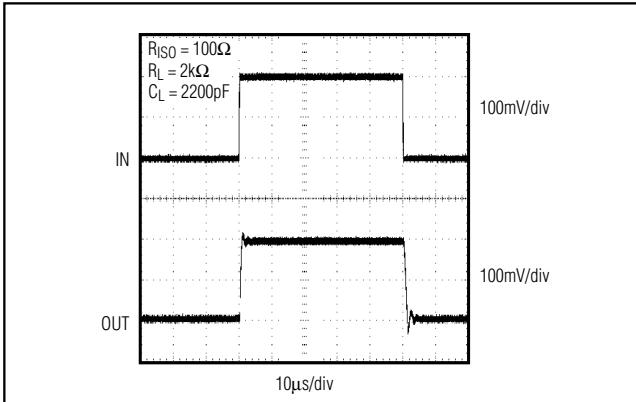


Figure 6c. Pulse Response With Isolating Resistor

### Chip Information

MAX4245 TRANSISTOR COUNT: 207

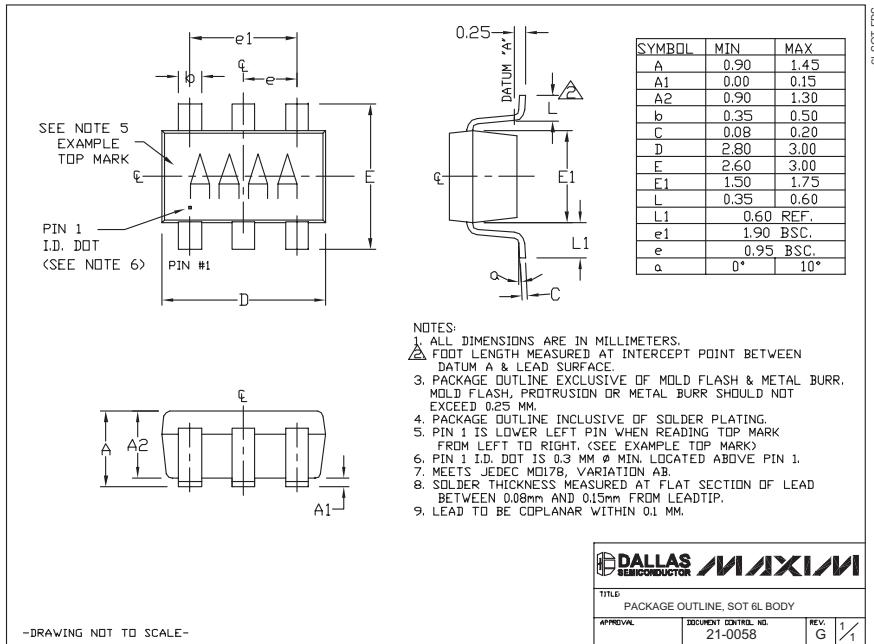
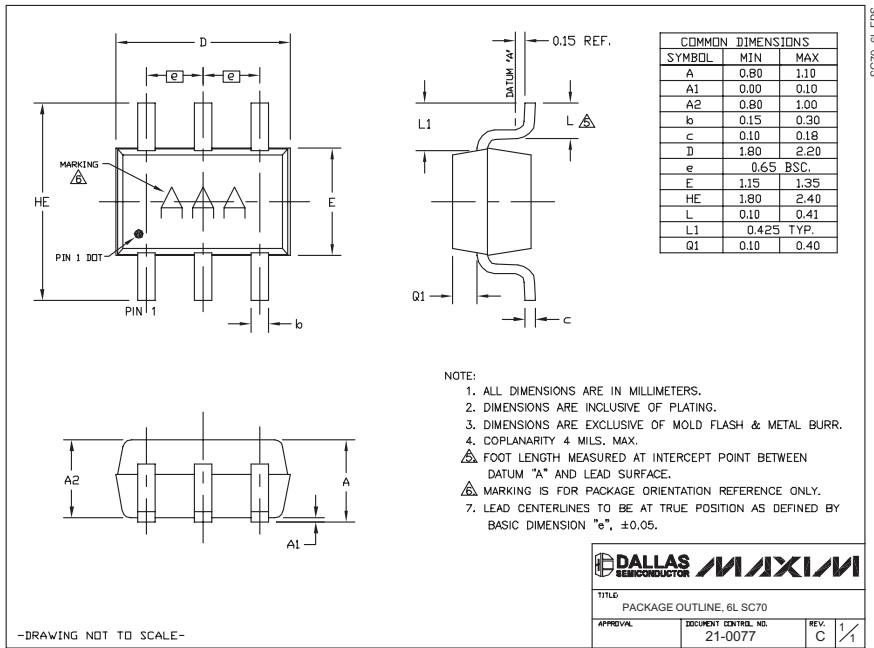
MAX4246/MAX4247 TRANSISTOR COUNT: 414

PROCESS: BiCMOS

# Ultra-Small, Rail-to-Rail I/O with Disable, Single/Dual-Supply, Low-Power Op Amps

## Package Information

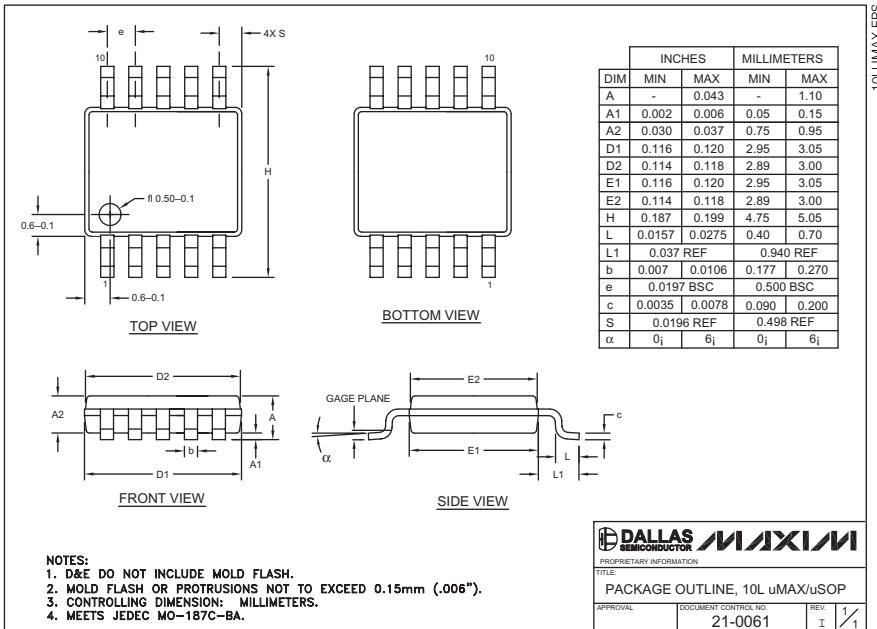
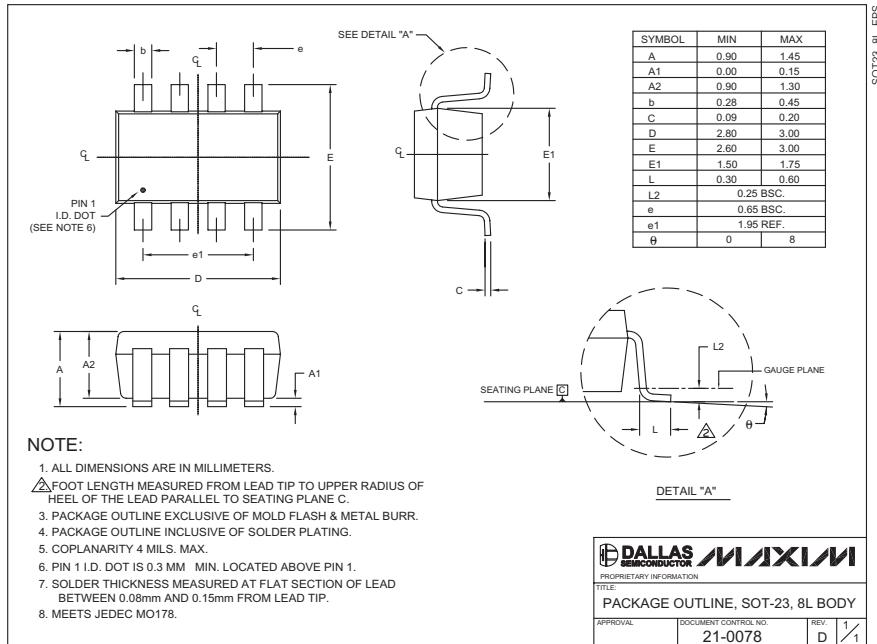
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



# Ultra-Small, Rail-to-Rail I/O with Disable, Single-/Dual-Supply, Low-Power Op Amps

## Package Information (continued)

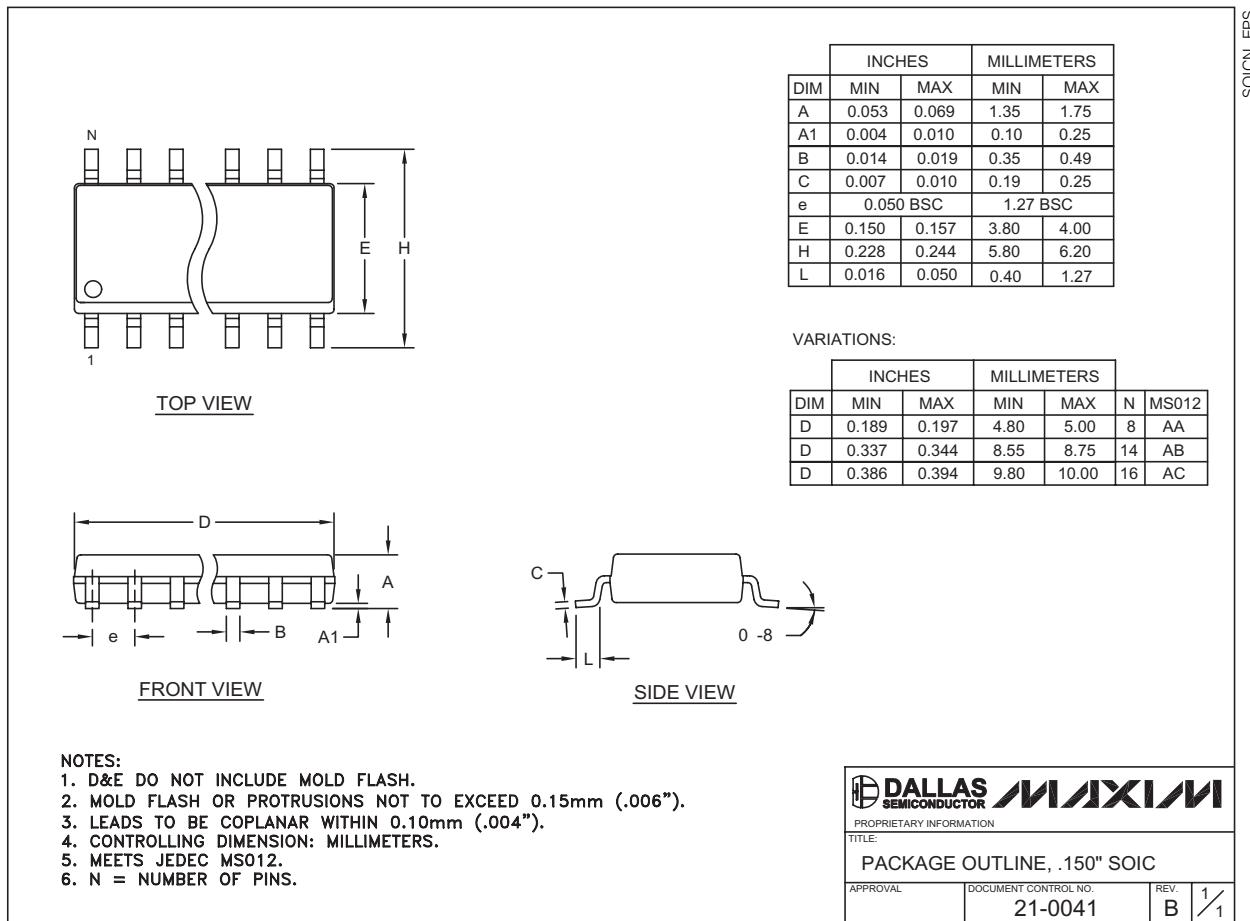
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



# Ultra-Small, Rail-to-Rail I/O with Disable, Single-/Dual-Supply, Low-Power Op Amps

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



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