

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL AVERAGE	TYPICAL
	PROPAGATION DELAY TIME	TOTAL POWER DISSIPATION
'86	14 ns	150 mW
'LS86A	10 ns	30.5 mW
'S86	7 ns	250 mW

description

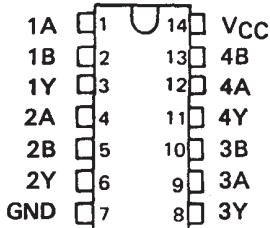
These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \bar{A}B + A\bar{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

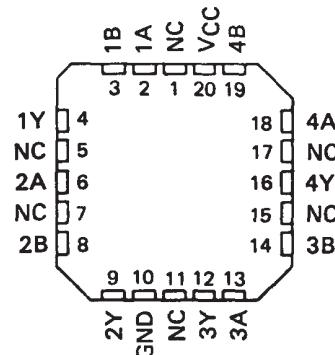
The SN5486, 54LS86A, and the SN54S86 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7486, SN74LS86A, and the SN74S86 are characterized for operation from 0°C to 70°C .

SN5486, SN54LS86A, SN54S86 . . . J OR W PACKAGE
SN7486 . . . N PACKAGE
SN74LS86A, SN74S86 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS86A, SN54S86 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR



These are five equivalent Exclusive-OR symbols valid for an '86 or 'LS86A gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



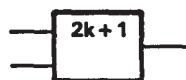
The output is active (low) if all inputs stand at the same logic level (i.e., $A=B$).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

SN5486, SN54LS86A, SN54S86

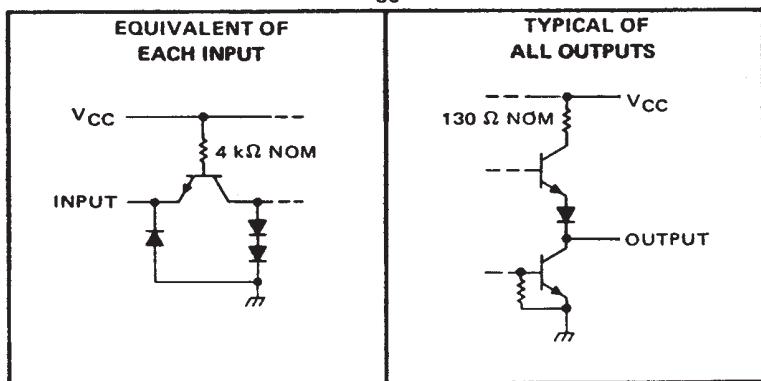
SN7486, SN74LS86A, SN74S86

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

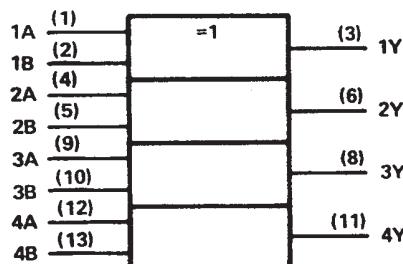
SDLS124 - DECEMBER 1972 - REVISED MARCH 1988

schematics of inputs and outputs

'86

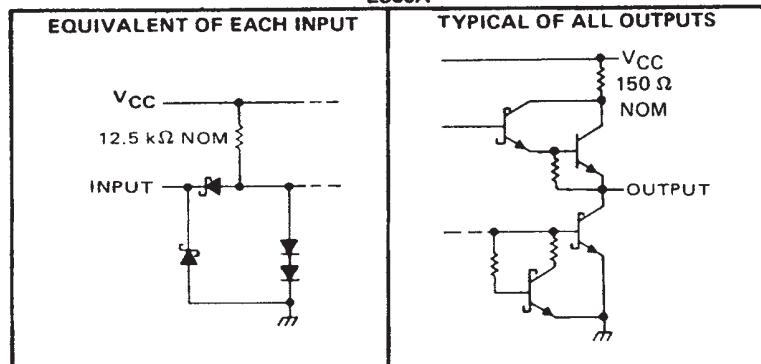


logic symbol†



†This symbol is in accordance with
ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

'LS86A

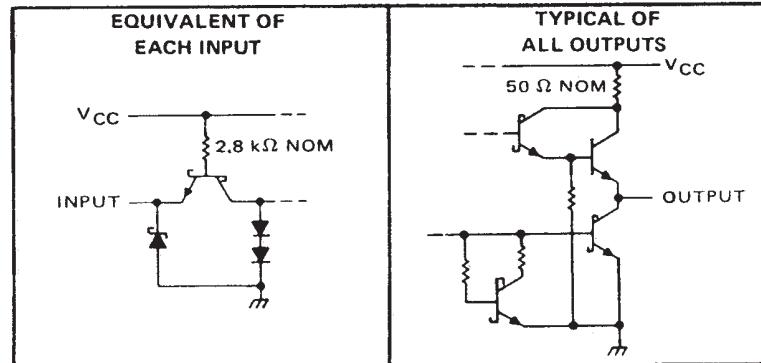


FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

'S86



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5486			SN7486			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}C$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN5486			SN7486			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH}	High-level input voltage			2		2		V
V _{IL}	Low-level input voltage				0.8		0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -8 mA			-1.5		-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 μ A	2.4	3.4		2.4	3.4	V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4 V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1		1	mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.4 V		40		40		μ A
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-1.6		-1.6	mA
I _{OS}	Short-circuit output current [§]	V _{CC} = MAX	--20	-55	-18	-55		mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 2	30	43	30	50		mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

[‡]All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with the inputs grounded and the outputs open.

NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER ¹	FROM (INPUT)	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low			15		23	ns
t_{PHL}					11		17	
t_{PLH}	A or B	Other input high			18		30	ns
t_{PHL}					13		22	

t_{PLH} = propagation delay time, low-to-high-level output

tPHI = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN5486, SN54LS86A, SN54S86

SN7486, SN74LS86A, SN74S86

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS86A	-55°C to 125°C
SN74LS86A	0°C to 70°C

Storage temperature range -65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS86A	SN74LS86A			UNIT	
		MIN	NOM	MAX		
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25
High-level output current, I_{OH}			-400		-400	μA
Low-level output current, I_{OL}			4		8	mA
Operating free-air temperature, T_A	-55		125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS86A			SN74LS86A			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage			0.7			0.8		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4		V
		$I_{OL} = 8 \text{ mA}$				0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$		0.2			0.2		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$		40			40		μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-0.8			-0.8		mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20	-100	-20	-20	-100		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		6.1	10	6.1	10		mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.[§]Not more than one output should be shorted at a time.NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [¶]	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
t_{PLH}	A or B	Other input low	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Note 3	12	23		ns	
t_{PHL}				10	17			
t_{PLH}		Other input high		20	30		ns	
t_{PHL}				13	22			

[¶] t_{PLH} = propagation delay time, low-to-high-level output t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S86			SN74S86			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-1		-1	mA
Low-level output current, I_{OL}				20		20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54S86			SN74S86			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH}	High-level input voltage			2		2		V
V _{IL}	Low-level input voltage				0.8		0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4	V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V V _{IL} = 0.8 V, I _{OL} = 20 mA			0.5		0.5	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1		1		mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V		50		50		μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5 V		-2		-2		mA
I _{OS}	Short-circuit output current [§]	V _{CC} = MAX	-40	-100	-40	-100		mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 2	50	75	50	75		mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

[‡]All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3: I_{OC} is measured with the inputs grounded and the outputs open.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER ¹	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	$C_L = 15 \text{ pF}$, $R_L = 280 \Omega$, See Note 3	7	10.5		ns
t_{PHL}				6.5	10		
t_{PLH}	A or B	Other input high	See Note 3	7	10.5		ns
t_{PHL}				6.5	10		

$t_{\text{tpi H}}$ = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/07501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/07501BCA	Samples
JM38510/07501BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/07501BDA	Samples
JM38510/07501BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/07501BDA	Samples
JM38510/30502B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/30502B2A	Samples
JM38510/30502B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/30502B2A	Samples
JM38510/30502BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/30502BCA	Samples
JM38510/30502BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/30502BCA	Samples
JM38510/30502BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/30502BDA	Samples
JM38510/30502BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/30502BDA	Samples
M38510/07501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/07501BCA	Samples
M38510/07501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/07501BCA	Samples
M38510/07501BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/07501BDA	Samples
M38510/07501BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/07501BDA	Samples
M38510/30502B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/30502B2A	Samples
M38510/30502B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/30502B2A	Samples
M38510/30502BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/30502BCA	Samples
M38510/30502BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/30502BCA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/30502BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30502BDA	Samples
M38510/30502BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30502BDA	Samples
SN5486J	OBsolete	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125	SN5486J	
SN5486J	OBsolete	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125	SN5486J	
SN54LS86AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS86AJ	Samples
SN54LS86AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS86AJ	Samples
SN54S86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S86J	Samples
SN54S86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S86J	Samples
SN7486N	OBsolete	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN7486N	OBsolete	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN7486N3	OBsolete	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN7486N3	OBsolete	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS86AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS86A	Samples
SN74LS86AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS86A	Samples
SN74LS86ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS86A	Samples
SN74LS86ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS86A	Samples
SN74LS86ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS86A	Samples
SN74LS86ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS86A	Samples
SN74LS86ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS86A	Samples
SN74LS86ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS86A	Samples
SN74LS86AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS86AN	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS86AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS86AN	Samples
SN74LS86AN3	OBsolete	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS86AN3	OBsolete	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS86ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS86AN	Samples
SN74LS86ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS86AN	Samples
SN74LS86ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS86A	Samples
SN74LS86ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS86A	Samples
SN74S86D	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S86	
SN74S86D	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S86	
SN74S86N	NRND	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S86N	
SN74S86N	NRND	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S86N	
SN74S86N3	OBsolete	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74S86N3	OBsolete	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SNJ5486J	OBsolete	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125	SNJ5486J	
SNJ5486J	OBsolete	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125	SNJ5486J	
SNJ5486W	OBsolete	CFP	W	14		TBD	Call TI	Call TI	-55 to 125	SNJ5486W	
SNJ5486W	OBsolete	CFP	W	14		TBD	Call TI	Call TI	-55 to 125	SNJ5486W	
SNJ54LS86AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS86AFK	Samples
SNJ54LS86AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS86AFK	Samples
SNJ54LS86AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS86AJ	Samples
SNJ54LS86AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS86AJ	Samples
SNJ54LS86AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS86AW	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS86AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS86AW	Samples
SNJ54S86FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 86FK	Samples
SNJ54S86FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 86FK	Samples
SNJ54S86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S86J	Samples
SNJ54S86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S86J	Samples
SNJ54S86W	NRND	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S86W	
SNJ54S86W	NRND	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S86W	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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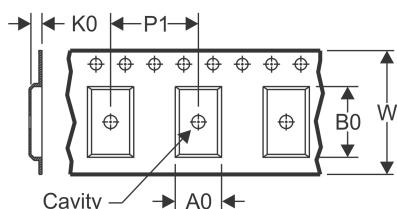
OTHER QUALIFIED VERSIONS OF SN5486, SN54LS86A, SN54S86, SN7486, SN74LS86A, SN74S86 :

- Catalog: [SN7486](#), [SN74LS86A](#), [SN74S86](#)
- Military: [SN5486](#), [SN54LS86A](#), [SN54S86](#)

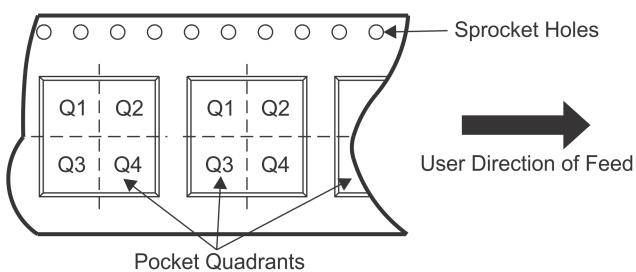
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

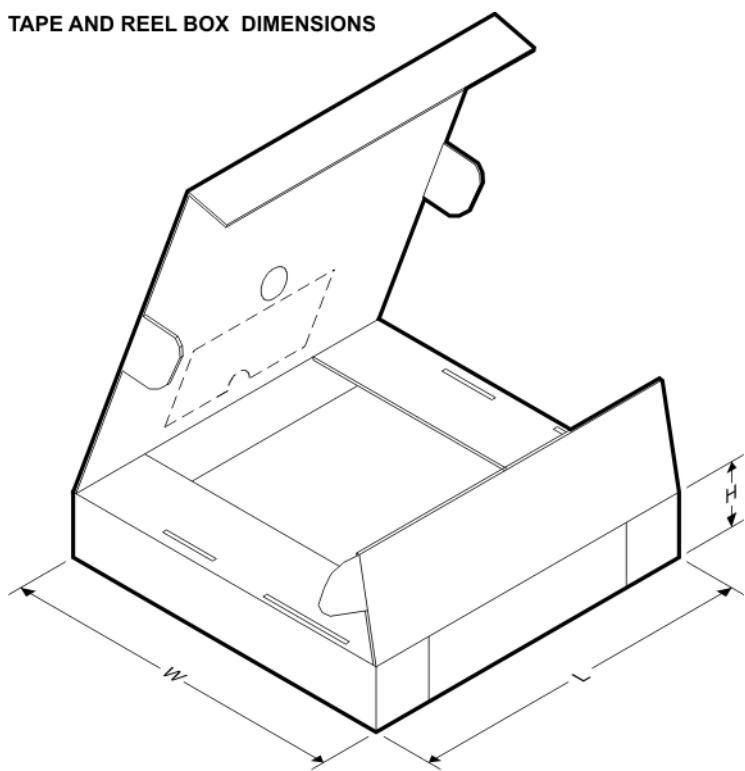
TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS86ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

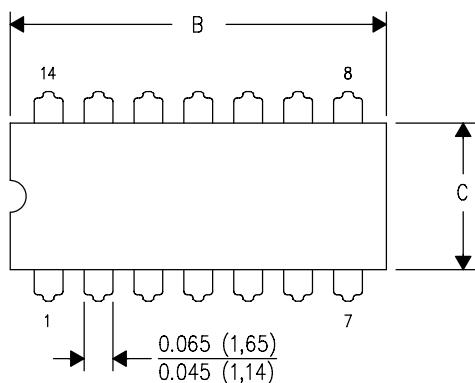
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS86ADR	SOIC	D	14	2500	367.0	367.0	38.0

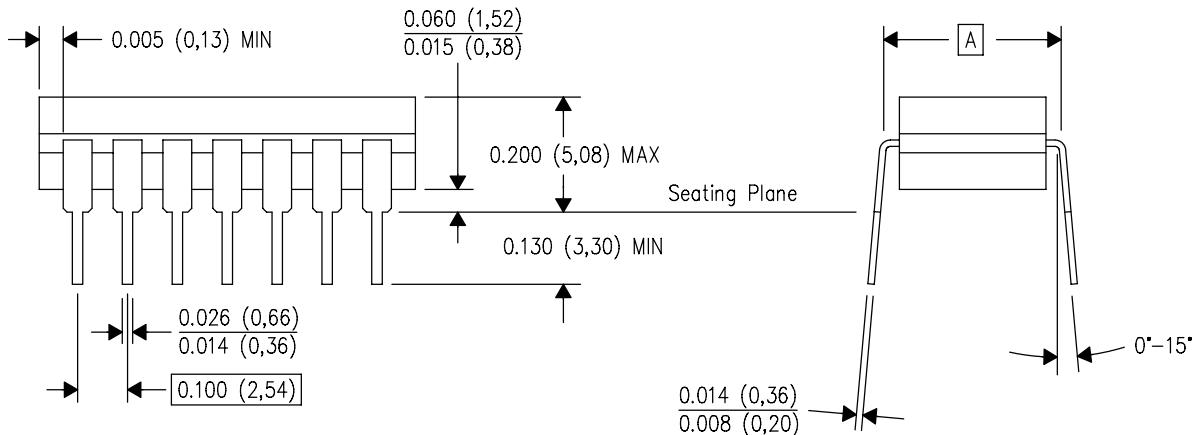
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

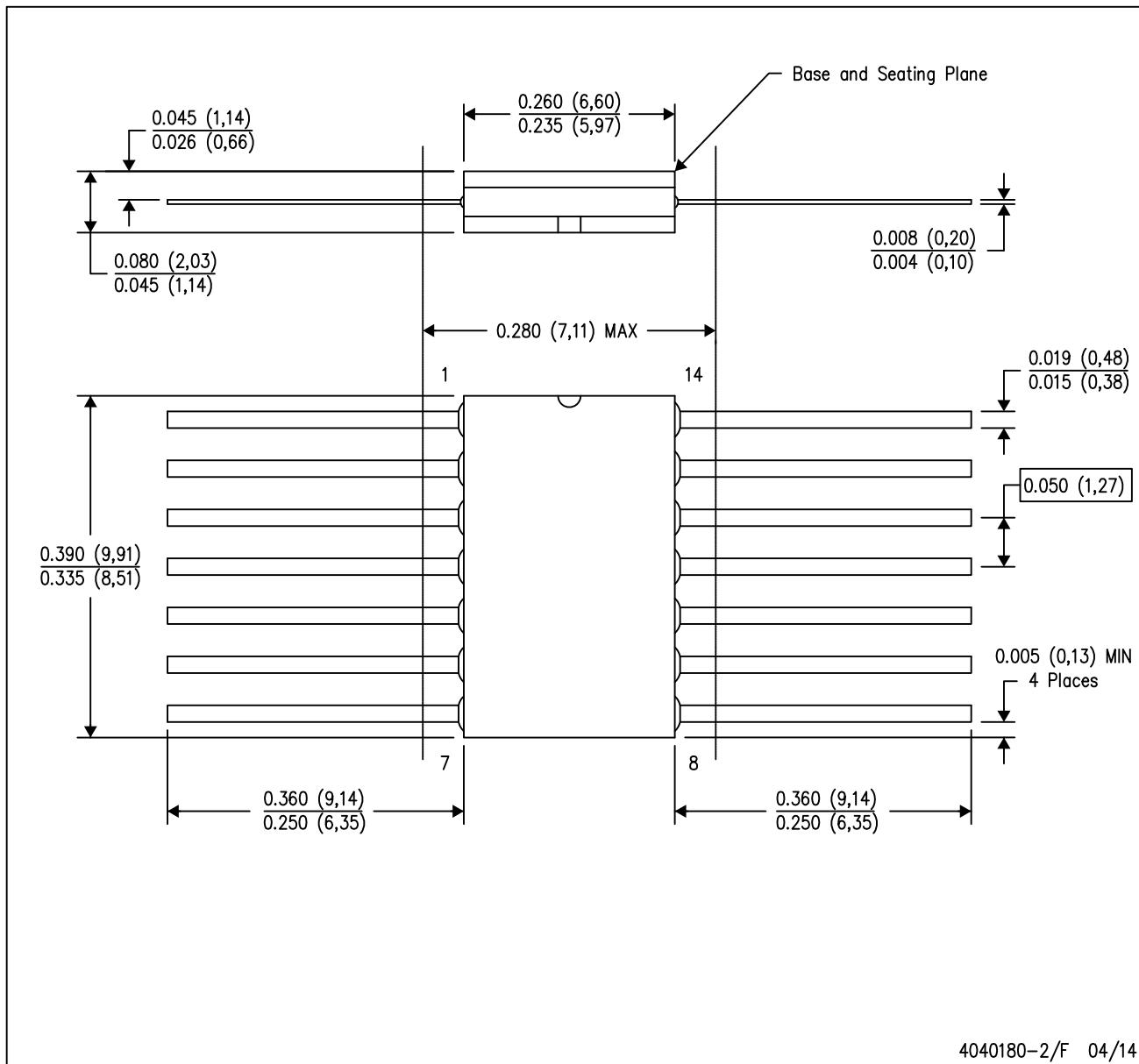


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



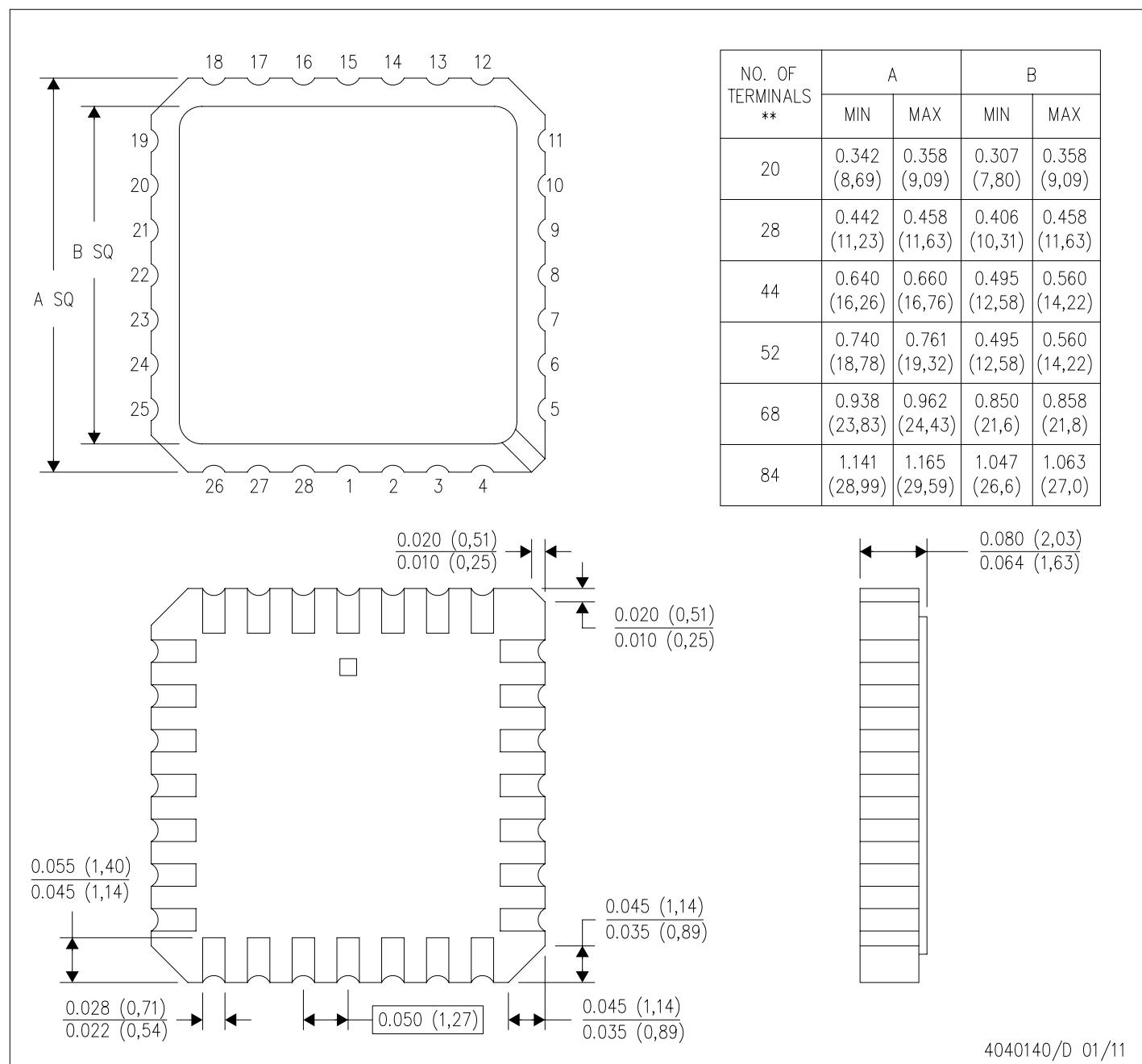
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

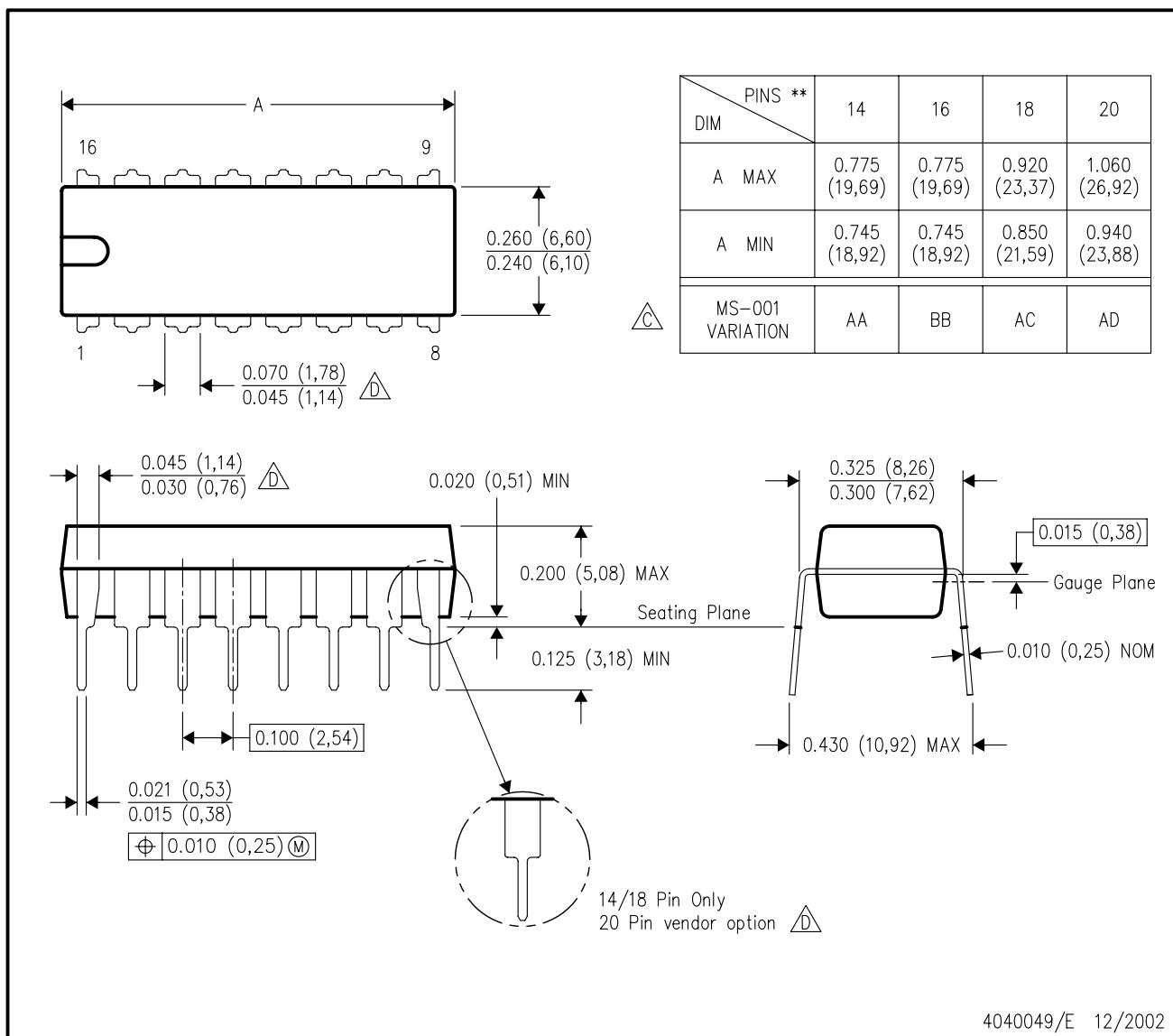
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



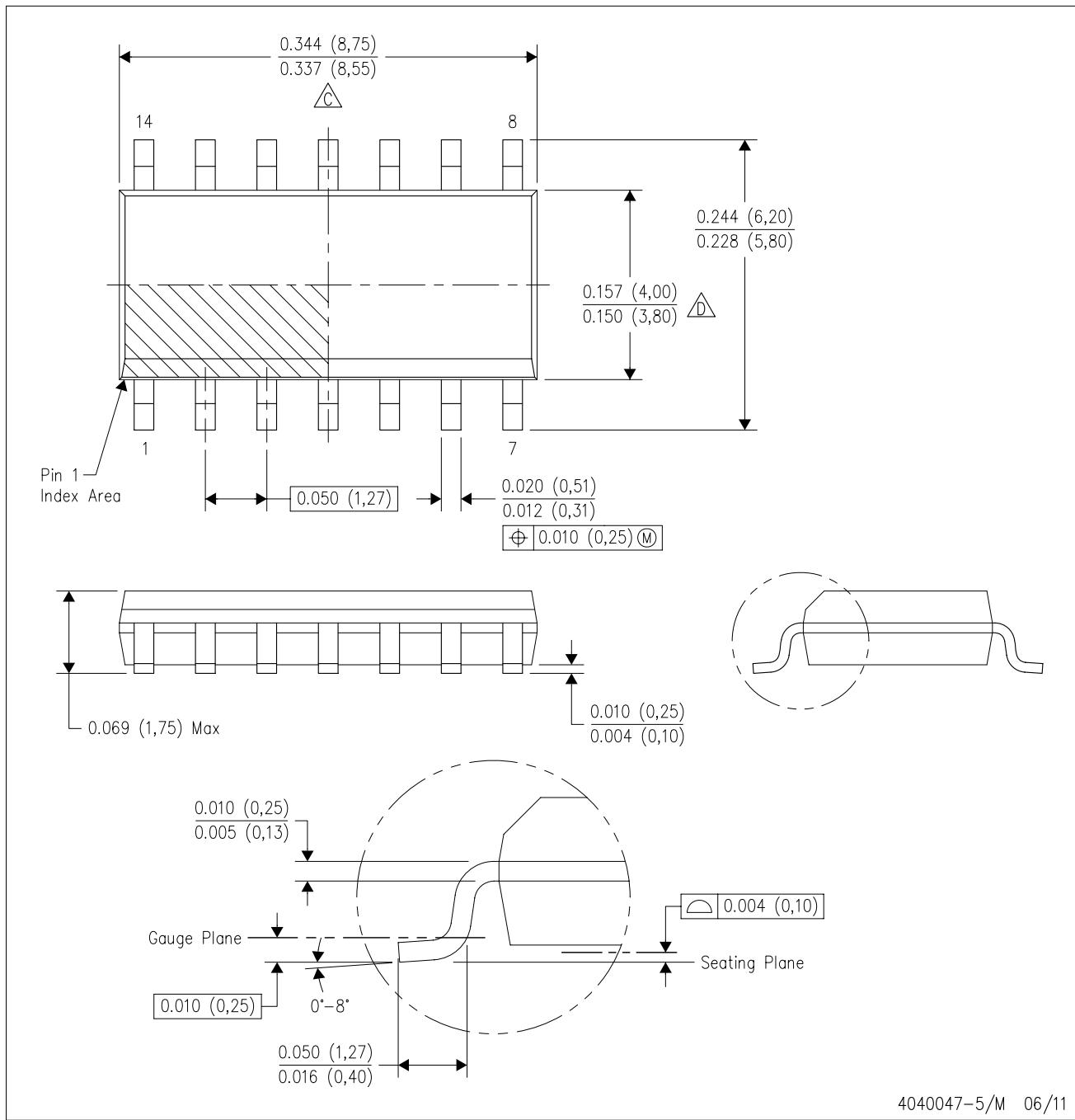
NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

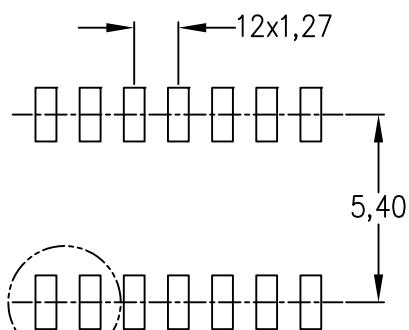
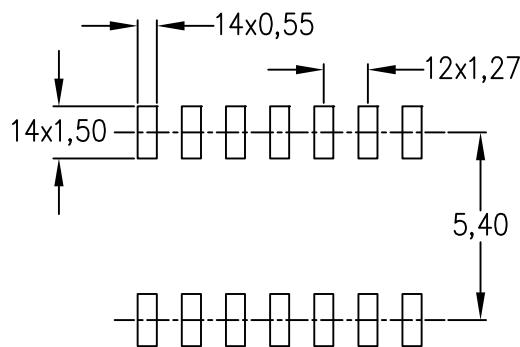
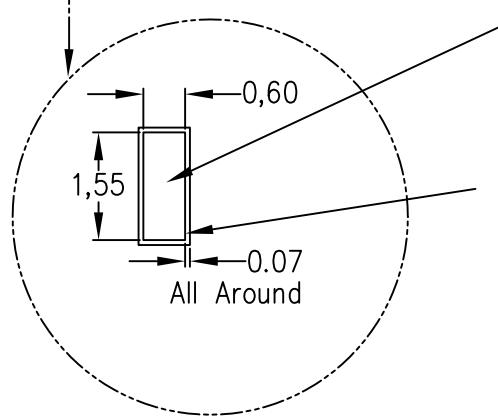
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211283-3/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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