

## CMOS 8-Bit Microcontroller

### TMP86CH49UG/F, TMP86CM49UG/F

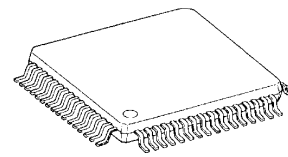
The TMP86CH49/M49 are the high-speed, high-performance and low-power consumption 8-bit microcontroller, including ROM, RAM, multi-function timer/counter, serial interface (UART, SIO, I<sup>2</sup>C), a 10-bit AD converter and two clock generators on chip.

Product No.	ROM	RAM	Package	OTP MCU
TMP86CH49UG/F	16k x 8 bits	512 bits	P-LQFP64-1010-0.50	TMP86PM49UG/F
TMP86CM49UG/F	32k x 8 bits	1k x 8 bits	P-QFP64-1414-0.80A	

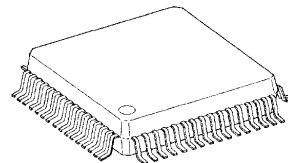
## Features

- ◆ 8-bit single chip microcomputer TLCS-870/C series
- ◆ Instruction execution time: 0.25  $\mu$ s (at 16 MHz)  
122  $\mu$ s (at 32.768 kHz)
- ◆ 132 types and 731 basic instructions
- ◆ 24 interrupt sources (External: 5, Internal: 19)
- ◆ Input/output ports (56 pins)
- ◆ 16-bit timer counter: 2 ch
  - Timer, Event counter, External trigger timer, Window, Pulse width measurement, PPG output modes
- ◆ 8-bit timer counter: 4 ch
  - Timer, Event counter, Programmable divider output, PWM output, Capture modes
- ◆ Time base timer
- ◆ Divider output function

P-LQFP64-1010-0.50

TMP86CH49UG  
TMP86CM49UG

P-QFP64-1414-0.80A

TMP86CH49F  
TMP86CHM49F

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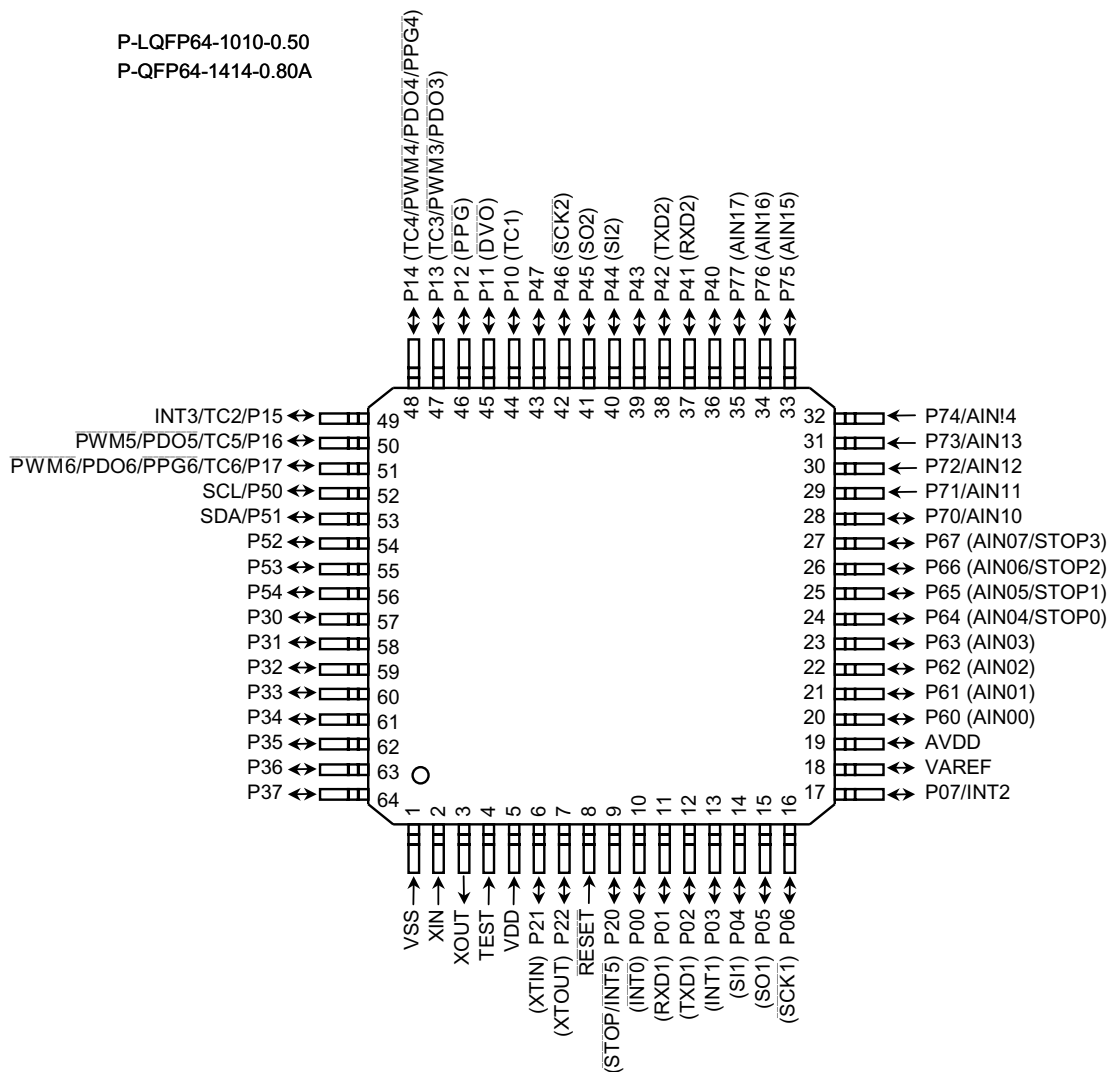
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  - For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.



Purchase of TOSHIBA I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

- ◆ Watchdog timer
  - Interrupt source/internal reset generate (Programmable)
- ◆ Serial interface
  - UART: 2ch
  - SIO: 2ch
  - I<sup>2</sup>C bus: 1ch
- ◆ 10-bit successive approximation type AD converter
  - Analog input: 16 ch
- ◆ Four Key-on wake-up: 4ch
- ◆ Dual clock operation
  - Single/dual-clock mode
- ◆ Nine power saving operating modes
  - STOP mode: Oscillation stops. Battery/capacitor back-up.  
Port output hold/High-impedance.
  - SLOW 1, 2 mode: Low-power consumption operation using low-frequency clock (32.768 kHz)
  - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer. Release by falling edge of TBTCCR<TBTCK> setting.
  - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock.  
Release by interrupts.
  - IDLE 2 mode: CPU stops, and peripherals operate using high and low-frequency clock.  
Release by interrupts.
  - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of time-base-timer. Release by falling edge of TBTCCR<TBTCK> setting.
  - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock.  
Release by interrupts.
  - SLEEP 2 mode: CPU stops, and peripherals operate using high- and low-frequency clock.  
Release by interrupts.
- ◆ Wide operating voltage: 4.5 to 5.5 V at 16 MHz/32.768 kHz  
2.7 to 5.5 V at 8 MHz/32.768 kHz  
1.8 to 5.5 V at 4.2 MHz/32.768 kHz

## Pin Assignments (Top view)



## Block Diagram

