XN01872 (XN1872)

Silicon n-channel enhancement MOSFET

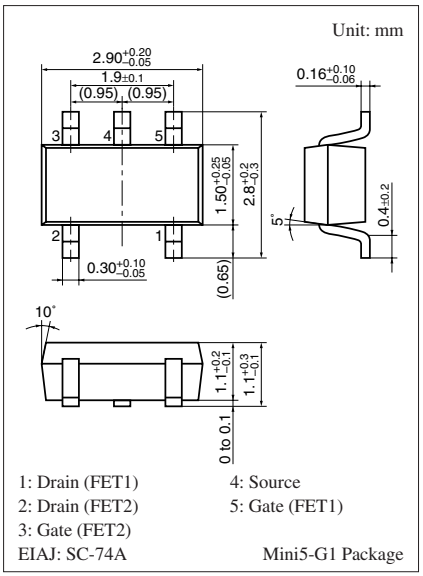
For switching

■ Features

- Two elements incorporated into one package (Source-coupled FETs)
- Reduction of the mounting area and assembly cost by one half

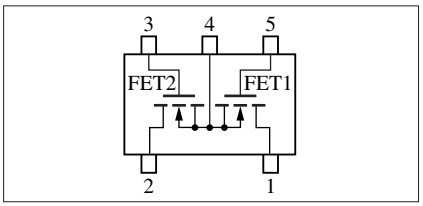
■ Basic Part Number

- 2SK0621 (2SK621) × 2



Marking Symbol: 5U

Internal Connection



■ Absolute Maximum Ratings $T_a = 25°C$

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	V_{DSS}	50	V
Gate-source voltage (Drain open)	V_{GSO}	8	V
Drain curennt	I_D	100	mA
Peak drain current	I_{DP}	200	mA
Total power dissipation	P_T	300	mW
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	−55 to +150	°C

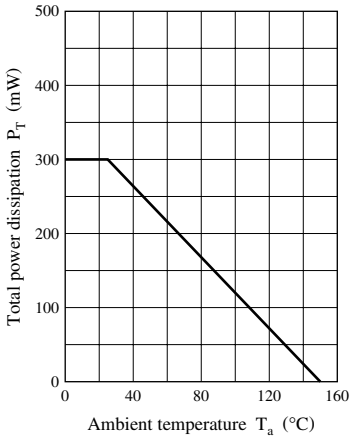
■ Electrical Characteristics $T_a = 25°C \pm 3°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	I_D = 100 µA, V_{GS} = 0	50			V
Drain-source cutoff current	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0			10	µA
Gate-source cutoff current	I_{GSS}	V_{GS} = 8 V, V_{DS} = 0	40		80	µA
Gate threshold voltage	V_{th}	I_D = 100 µA, V_{DS} = V_{GS}	1.5		3.5	V
Drain-source ON resistance	$R_{DS(on)}$	I_D = 20 mA, V_{GS} = 5 V			50	Ω
Forward transfer admittance	$\|Y_{fs}\|$	I_D = 20 mA, V_{DS} = 5 V, f = 1 kHz	20	30		mS
Output voltage high-level	V_{OH}	V_{DS} = 5 V, V_{GS} = 1 V, R_L = 200 Ω	4.5			V
Output voltage low-level	V_{OL}	V_{DS} = 5 V, V_{GS} = 5 V, R_L = 200 Ω			1.0	V
Input resistance *1	R_1+R_2		100		200	kΩ
Turn-on time *2	t_{on}	V_{DD} = 5 V, V_{GS} = 0 V to 5 V, R_L = 200 Ω			1.0	µs
Turn-off time *2	t_{off}	V_{DD} = 5 V, V_{GS} = 5 V to 0 V, R_L = 200 Ω			1.0	µs
Short-circuit forward transfer capacitance (Common-source)	C_{iss}	V_{DS} = 5 V, V_{GS} = 0, f = 1 MHz		9	15	pF

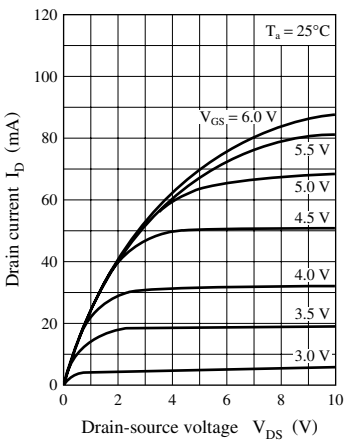
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.
2. ∗1: Resistance ratio R_1/R_2 = 1/50
∗2: Pulse measurement

Note) The part number in the parenthesis shows conventional part number.

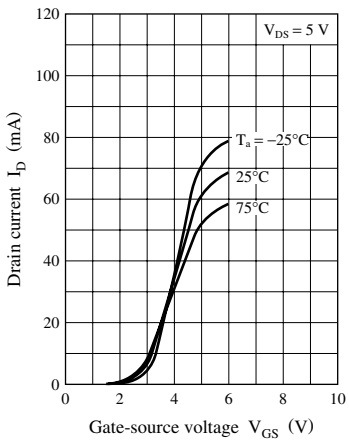
P_T — T_a



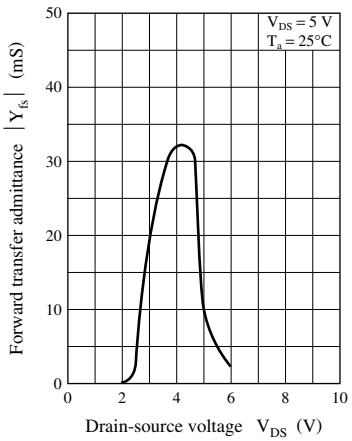
I_D — V_{DS}



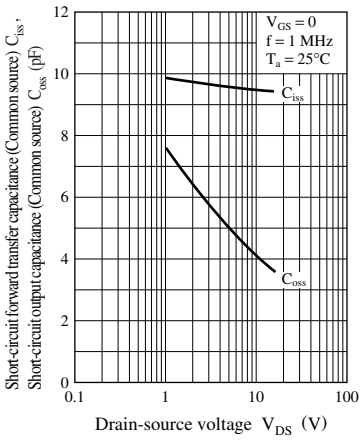
I_D — V_{GS}



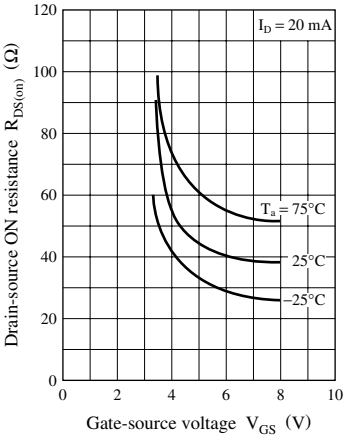
$|Y_{fs}|$ — V_{DS}



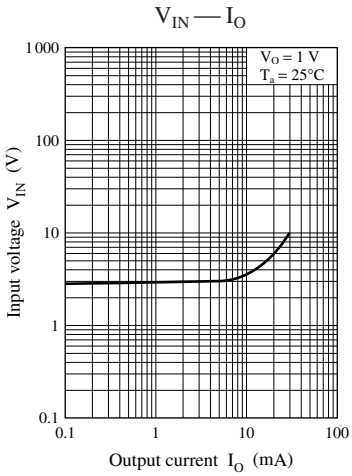
C_{iss} , C_{oss} — V_{DS}



$R_{DS(on)}$ — V_{GS}



V_{IN} — I_O



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