

1.5-A 60-V STEP-DOWN SWIFT™ DC-DC CONVERTER WITH Eco-mode™ CONTROL

Check for Samples: [TPS54160-Q1](#)

FEATURES

- Qualified for Automotive Applications
- 3.5-V to 60-V Input Voltage Range
- 200-mΩ High-Side MOSFET
- High Efficiency at Light Loads With Pulse-Skipping Eco-mode™ Control Scheme
- 116-μA Operating Quiescent Current
- 1.3-μA Shutdown Current
- 100-kHz to 2.5-MHz Switching Frequency
- Synchronizes to External Clock
- Adjustable Slow Start and Sequencing
- Undervoltage and Overvoltage Power-Good Output

- Adjustable Undervoltage Lockout (UVLO) Voltage and Hysteresis
- 0.8-V Internal Voltage Reference
- Supported by SwitcherPro™ Software Tool (<http://focus.ti.com/docs/toolsw/folders/print/switcherpro.html>)
- For SWIFT™ power products documentation, see the TI Web site at <http://www.ti.com/swift>.

APPLICATIONS

- 12-V, 24-V, and 48-V Industrial and Commercial Low-Power Systems
- Aftermarket Automotive Accessories: Video, GPS, Entertainment

DESCRIPTION

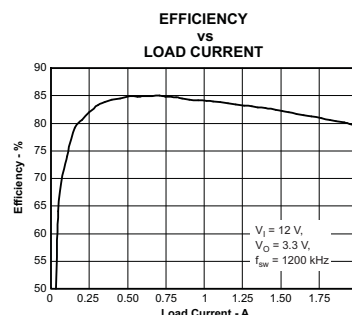
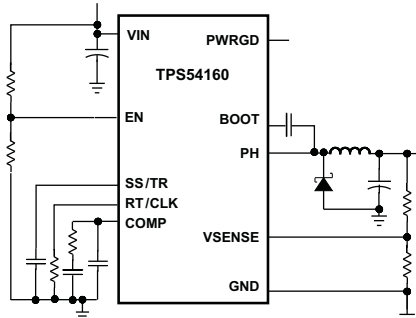
The TPS54160-Q1 device is a 60-V 1.5-A step-down regulator with an integrated high-side MOSFET. Current-mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the no-load, input supply current to 116 μA. Using the enable pin reduces the shutdown supply current to 1.3 μA.

Undervoltage lockout is set internally at 2.5 V but can be increased using the enable pin. The slow-start pin, which is also configurable for sequencing or tracking, controls the output-voltage start-up ramp. An open-drain power-good signal indicates the output is within 92% to 109% of its nominal voltage.

A wide switching-frequency range allows optimization of efficiency and external component size. Frequency foldback and thermal shutdown protect the part during an overload condition.

The TPS54160-Q1 is available in a 10-pin thermally enhanced MSOP (DGQ) or 10-pin SON (DRC) PowerPAD™ package.

SIMPLIFIED SCHEMATIC



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE AND ORDERING INFORMATION

For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating temperature range (unless otherwise noted)

V _{IN}	Input voltage	VIN		–0.3 V to 65 V
		EN ⁽²⁾		–0.3 V to 5 V
		BOOT		73 V
		VSENSE		–0.3 V to 3 V
		COMP		–0.3 V to 3 V
		PWRGD		–0.3 V to 6 V
		SS/TR		–0.3 V to 3 V
		RT/CLK		–0.3 V to 3.6 V
		V _{OUT}	Output voltage	BOOT to PH
PH				–0.6 V to 65 V
	200 ns			–1 V to 65 V
	30 ns			–2 V to 65 V
	Maximum dc voltage, T _J = –40°C			–0.85 V
V _{DIFF}	Differential voltage	PAD to GND		±200 mV
I _{SOURCE}	Source current	EN		100 μA
		BOOT		100 mA
		VSENSE		10 μA
		PH		Current limit
		RT/CLK		100 μA
I _{SINK}	Sink current	VIN		Current limit
		COMP		100 μA
		PWRGD		10 mA
		SS/TR		200 μA
ESD	Electrostatic discharge protection	Human-body model (HBM) (AEC-Q100-002)		500 V
		Machine model (MM) (AEC-Q100-003)		50 V
		Charged-device model (CDM) (AEC-Q100-011)		1000 V
T _J	Operating junction temperature range			–40°C to 150°C
T _{stg}	Storage temperature range			–65°C to 150°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) See [Enable and Adjusting Undervoltage Lockout](#) for details.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾⁽²⁾		TPS54160-Q1		UNIT
		DGQ	DRC	
		10 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance (standard board)	62.5	56.5	°C/W
θ_{JA}	Junction-to-ambient thermal resistance (custom board) ⁽³⁾	57	61.5	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance	83	52.1	°C/W
θ_{JB}	Junction-to-board thermal resistance	28	20.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.1	20.8	°C/W
θ_{JCbott}	Junction-to-case (bottom) thermal resistance	21	5.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) Determine the power rating at a specific ambient temperature T_A with a junction temperature of 150°C. This is the point where distortion starts to increase substantially. See the power-dissipation estimate in the application section of this data sheet for more information.
- (3) Test-board conditions:
- (a) 3 inches (7.62 cm) × 3 inches (7.62 cm), two layers, thickness: 0.062 inch (1.59 mm)
 - (b) 2-oz. (0.071-mm thick) copper traces located on the top of the PCB
 - (c) 2-oz. (0.071-mm thick) copper ground plane, bottom layer
 - (d) Six thermal vias (13-mil), 0.33-mm located under the device package

ELECTRICAL CHARACTERISTICS

$T_J = -40^\circ\text{C}$ to 150°C , $V_{IN} = 3.5\text{ V}$ to 60 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
Operating input voltage			3.5		60	V
Internal undervoltage-lockout threshold		No voltage hysteresis, rising and falling		2.5		V
Shutdown supply current		EN = 0 V, 25°C, 3.5 V ≤ VIN ≤ 60 V		1.5	4	μA
		EN = 0 V, 125°C, 3.5 V ≤ VIN ≤ 60 V		1.9	6.5	
Operating nonswitching supply current		VSENSE = 0.83 V, VIN = 12 V, TJ = 25°C		116	136	
ENABLE AND UVLO (EN PIN)						
Enable threshold voltage		No voltage hysteresis, rising and falling, TJ = 25°C	0.9	1.25	1.55	V
Input current		Enable threshold 50 mV		−3.8		μA
		Enable threshold −50 mV		−0.9		
Hysteresis current				−2.9		μA
VOLTAGE REFERENCE						
Voltage reference		TJ = 25°C	0.792	0.8	0.808	V
			0.784	0.8	0.816	
HIGH-SIDE MOSFET						
On-resistance		VIN = 3.5 V, BOOT-PH = 3 V		300		mΩ
		VIN = 12 V, BOOT-PH = 6 V		200	410	
ERROR AMPLIFIER						
Input current				50		nA
gm	Error-amplifier transconductance	−2 μA < ICOMP < 2 μA, VCOMP = 1 V		97		μS
gm	Error-amplifier transconductance during slow start	−2 μA < ICOMP < 2 μA, VCOMP = 1 V, VSENSE = 0.4 V		26		μS
Error-amplifier dc gain		VSENSE = 0.8 V		10,000		V/V
Error-amplifier bandwidth				2700		kHz
Error-amplifier source/sink		V(Comp) = 1 V, 100-mV overdrive		±7		μA

ELECTRICAL CHARACTERISTICS (continued) $T_J = -40^{\circ}\text{C}$ to 150°C , $V_{IN} = 3.5\text{ V}$ to 60 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMP to switch current transconductance			6		A/V

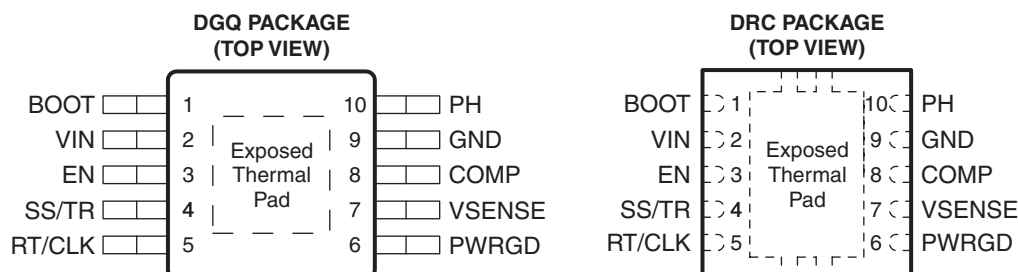
ELECTRICAL CHARACTERISTICS (continued)

 $T_J = -40^{\circ}\text{C}$ to 150°C , $V_{IN} = 3.5\text{ V}$ to 60 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
Current-limit threshold		VIN = 12 V, TJ = 25°C	1.8	2.7		A
THERMAL SHUTDOWN						
Thermal shutdown				182		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
	Switching frequency range using RT mode	VIN = 12 V	100		2500	kHz
fsw	Switching frequency	VIN = 12 V, RT = 200 kΩ	450	581	720	kHz
	Switching-frequency range using CLK mode	VIN = 12 V	300		2200	kHz
	Minimum CLK input-pulse duration			40		ns
	RT/CLK high threshold	VIN = 12 V		1.9	2.2	V
	RT/CLK low threshold	VIN = 12 V	0.45	0.7		V
	RT/CLK falling-edge to PH rising-edge delay	Measured at 500 kHz with RT resistor in series		60		ns
	PLL lock-in time	Measured at 500 kHz		100		μs
SLOW START AND TRACKING (SS/TR)						
	Charge current	VSS/TR = 0.4 V		2		μA
	SS/TR-to-VSENSE matching	VSS/TR = 0.4 V		45		mV
	SS/TR-to-reference crossover	98% nominal		1.0		V
	SS/TR discharge current (overload)	VSENSE = 0 V, V(SS/TR) = 0.4 V		112		μA
	SS/TR discharge voltage	VSENSE = 0 V		54		mV
POWER GOOD (PWRGD PIN)						
VVSENSE	VSENSE threshold	VSENSE falling (fault)		92%		
		VSENSE rising (good)		94%		
		VSENSE rising (fault)		109%		
		VSENSE falling (good)		107%		
	Hysteresis	VSENSE falling		2%		
	Output high leakage	VSENSE = VREF, V(PWRGD) = 5.5 V, TJ = 25°C		10		nA
	On resistance	I(PWRGD) = 3 mA, VSENSE < 0.79 V		50		Ω
	Minimum VIN for defined output	V(PWRGD) < 0.5 V, I(PWRGD) = 100 μA		0.95	1.5	V

DEVICE INFORMATION

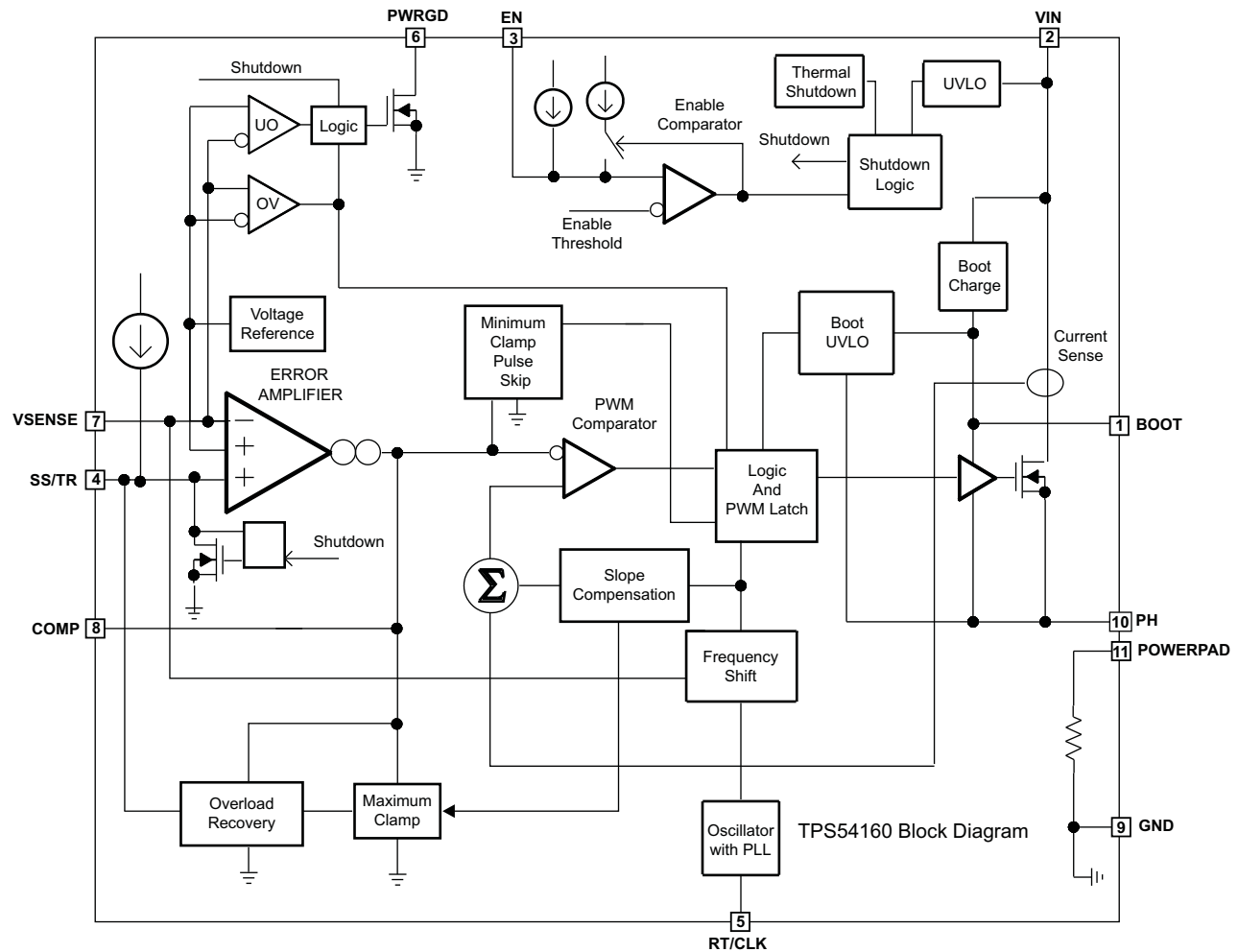
PIN CONFIGURATION



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	The device requires a bootstrap capacitor between BOOT and PH. A voltage on this capacitor that is below the minimum required by the output device, forces the output to switch off until the capacitor recharges.
COMP	8	O	Error-amplifier output, and input to the output-switch current comparator. Connect frequency-compensation components to COMP.
EN	3	I	Enable pin, internal pullup current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
GND	9	–	Ground
PH	10	I	The source of the internal high-side power MOSFET
PWRGD	6	O	Open-drain output, asserts low if output voltage is low due to thermal shutdown, dropout, overvoltage, or EN shutdown.
RT/CLK	5	I	Resistor timing and external clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The mode change disables the internal amplifier and the pin is a high-impedance clock input to the internal PLL. Stoppage of the clocking edges re-enables the internal amplifier, and the mode returns to a resistor-set function.
SS/TR	4	I	Slow-start and tracking. An external capacitor connected to this pin sets the rise time of the output. The voltage on this pin overrides the internal reference, which allows use of the pin for tracking and sequencing.
VIN	2	I	Input supply voltage, 3.5 V to 60 V
VSENSE	7	I	Inverting node of the transconductance (gm) error amplifier
Thermal pad			Connect the GND pin electrically to the exposed pad on the printed circuit board for proper operation.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

ON-RESISTANCE vs JUNCTION TEMPERATURE

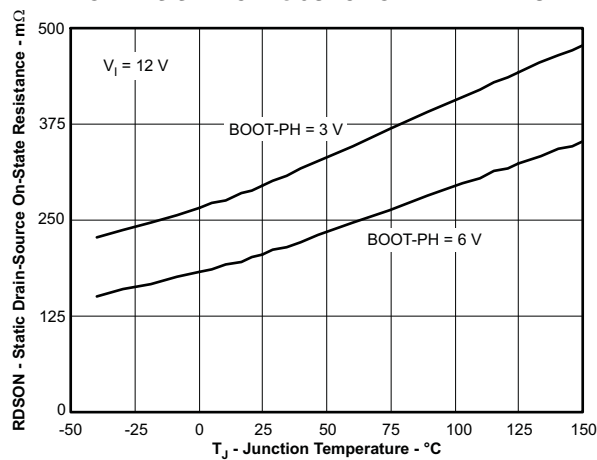


Figure 1.

VOLTAGE REFERENCE versus JUNCTION TEMPERATURE

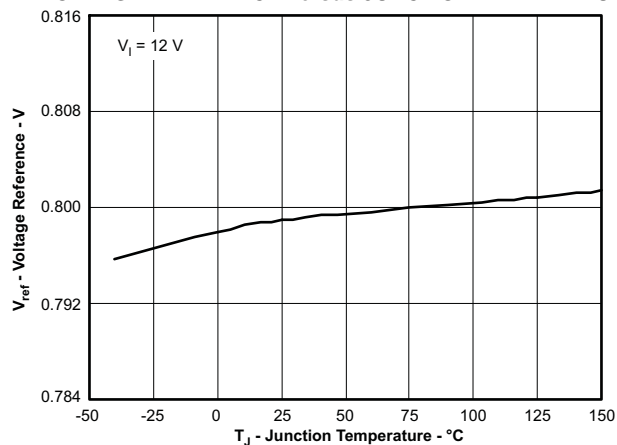


Figure 2.

SWITCH-CURRENT LIMIT versus JUNCTION TEMPERATURE

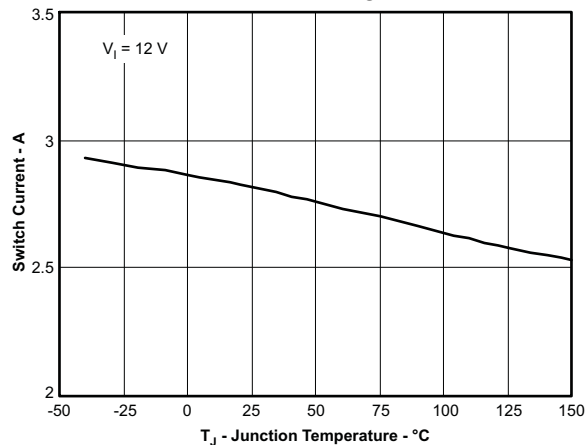


Figure 3.

SWITCHING FREQUENCY versus JUNCTION TEMPERATURE

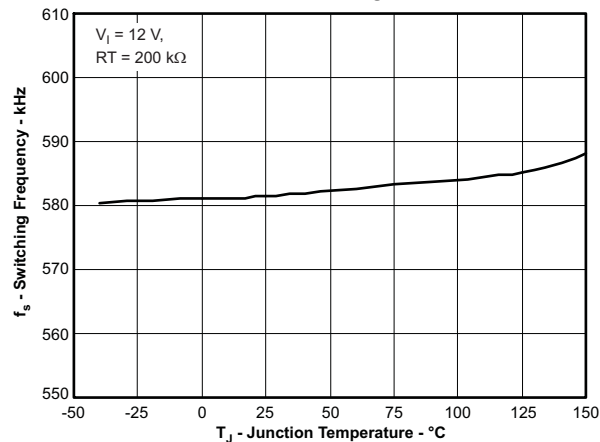


Figure 4.

SWITCHING FREQUENCY versus RT/CLK RESISTANCE HIGH-FREQUENCY RANGE

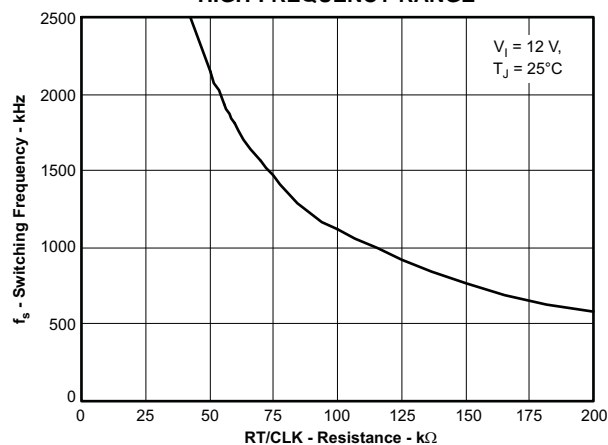


Figure 5.

SWITCHING FREQUENCY versus RT/CLK RESISTANCE-LOW FREQUENCY RANGE

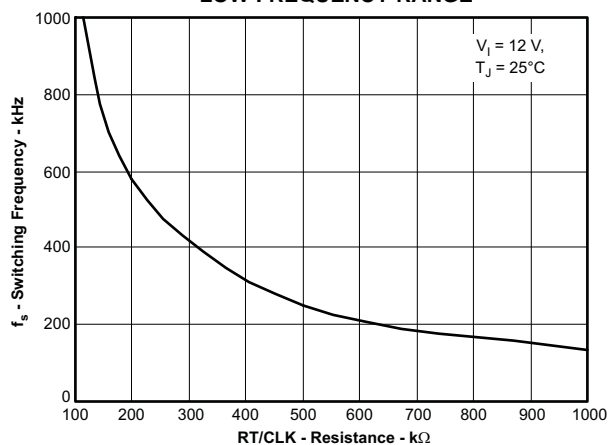


Figure 6.

TYPICAL CHARACTERISTICS (continued)

EA TRANSCONDUCTANCE DURING SLOW START versus JUNCTION TEMPERATURE

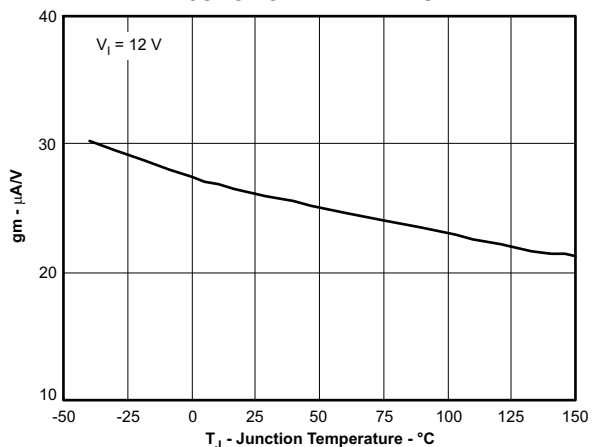


Figure 7.

EA TRANSCONDUCTANCE versus JUNCTION TEMPERATURE

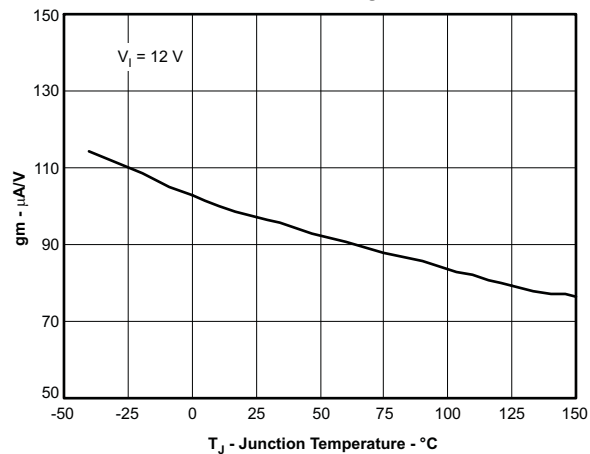


Figure 8.

EN PIN VOLTAGE versus JUNCTION TEMPERATURE

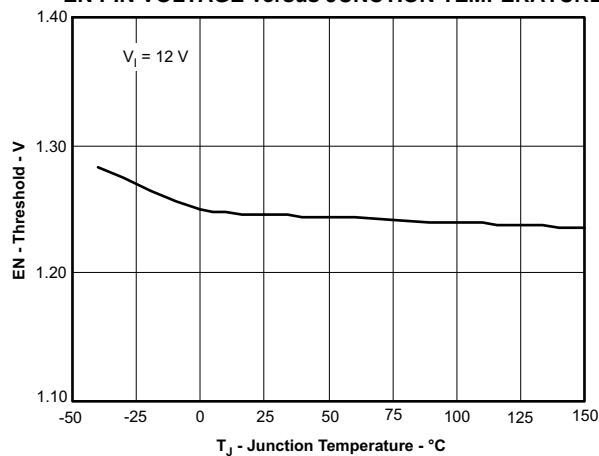


Figure 9.

EN PIN CURRENT versus JUNCTION TEMPERATURE

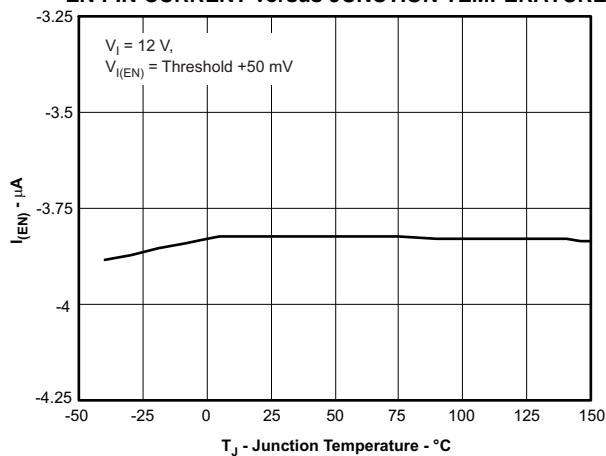


Figure 10.

EN PIN CURRENT versus JUNCTION TEMPERATURE

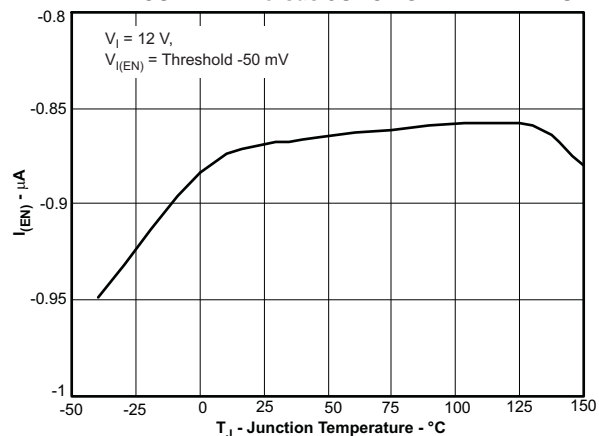


Figure 11.

SS/TR CHARGE CURRENT versus JUNCTION TEMPERATURE

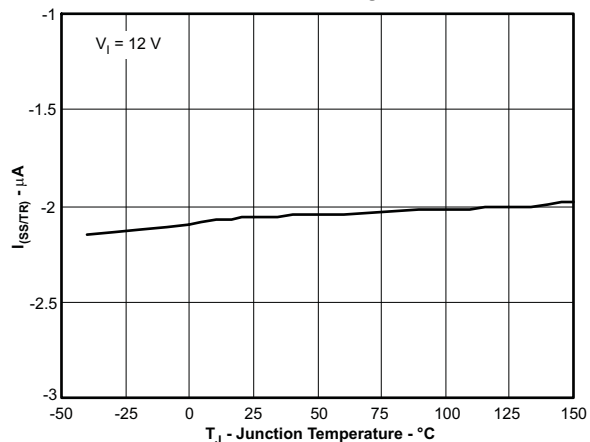
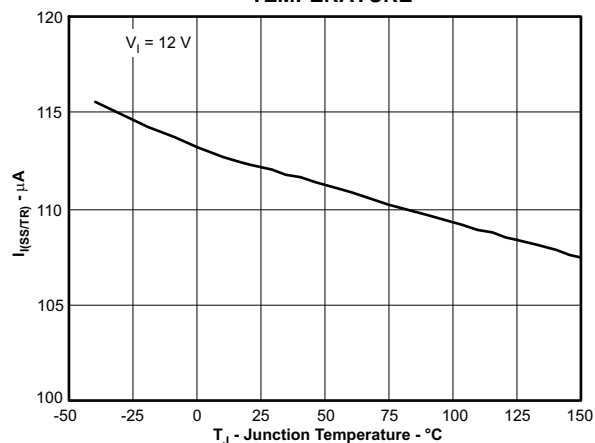
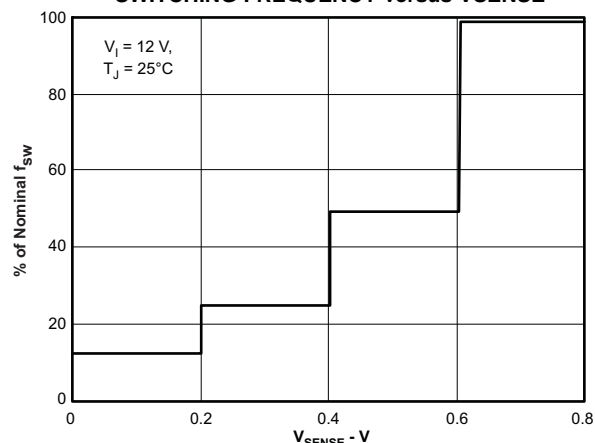
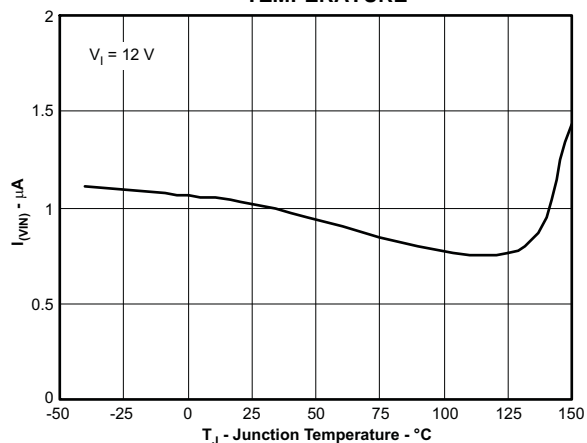
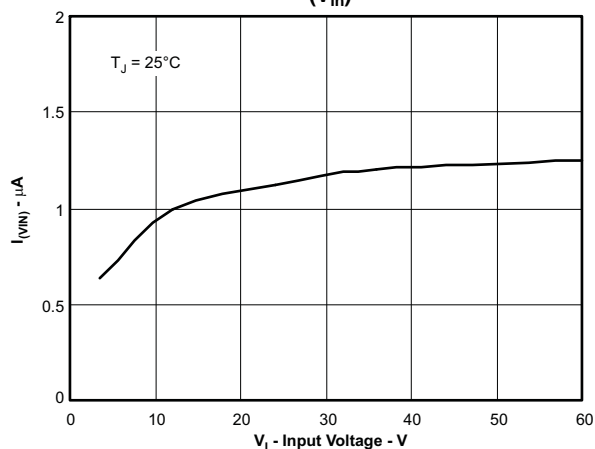
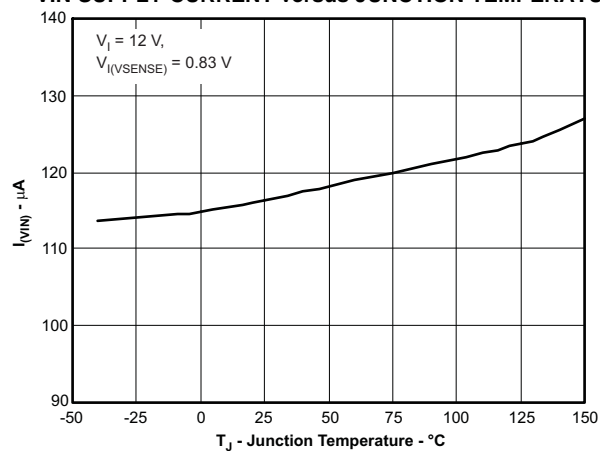
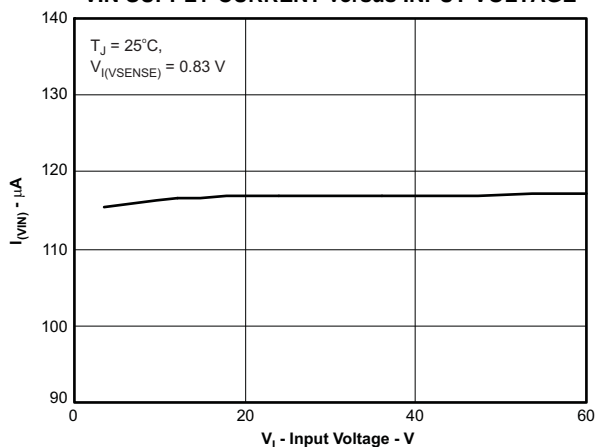


Figure 12.

TYPICAL CHARACTERISTICS (continued)**SS/TR DISCHARGE CURRENT versus JUNCTION TEMPERATURE****Figure 13.****SWITCHING FREQUENCY versus VSENSE****Figure 14.****SHUTDOWN SUPPLY CURRENT versus JUNCTION TEMPERATURE****Figure 15.****SHUTDOWN SUPPLY CURRENT versus INPUT VOLTAGE (V_{in})****Figure 16.****VIN SUPPLY CURRENT versus JUNCTION TEMPERATURE****Figure 17.****VIN SUPPLY CURRENT versus INPUT VOLTAGE****Figure 18.**

TYPICAL CHARACTERISTICS (continued)

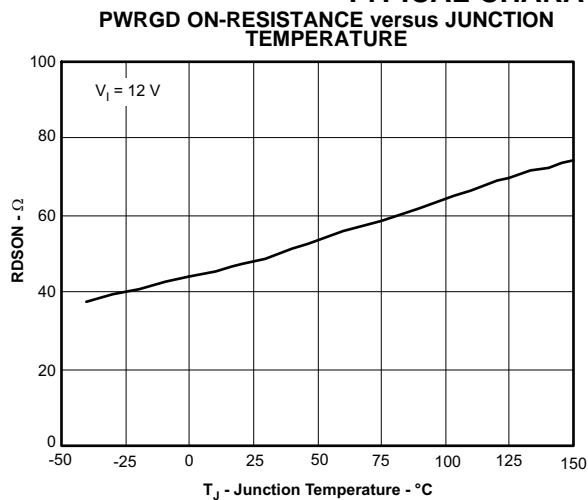


Figure 19.

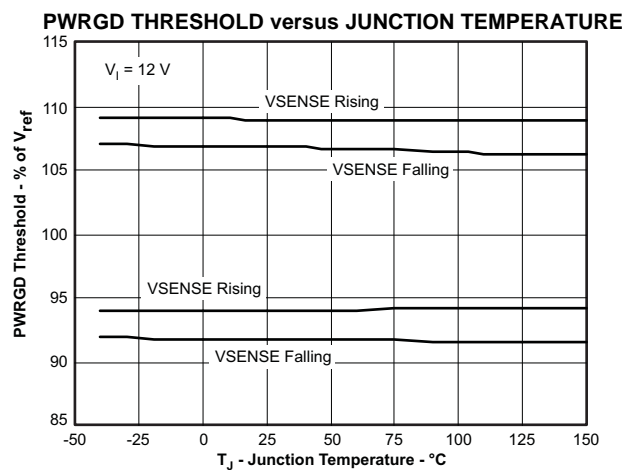


Figure 20.

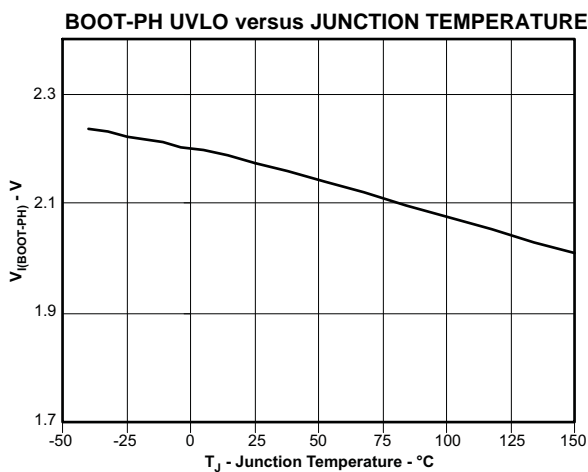


Figure 21.

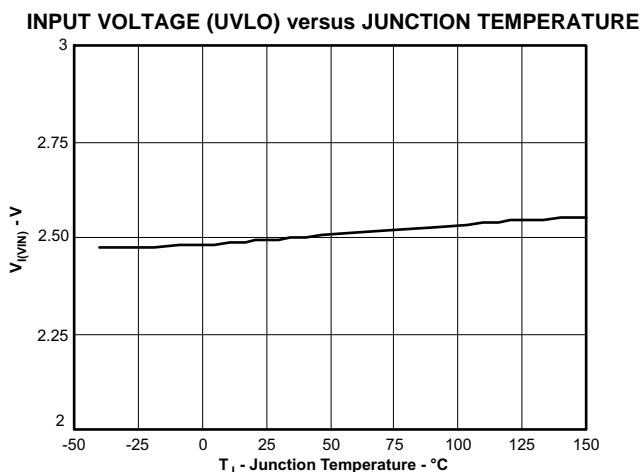


Figure 22.

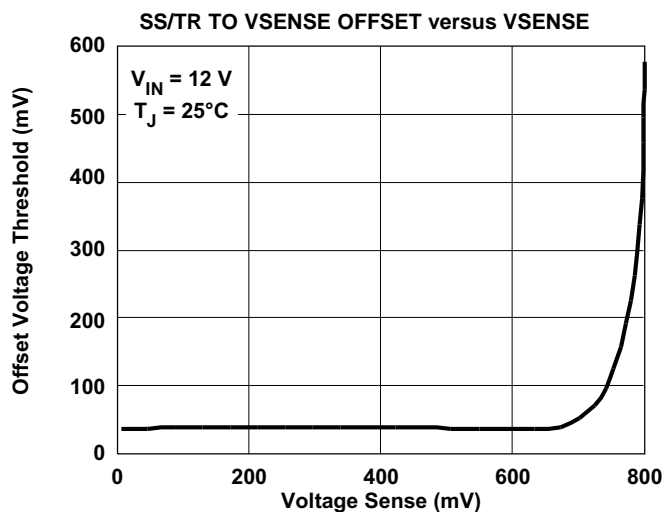


Figure 23.

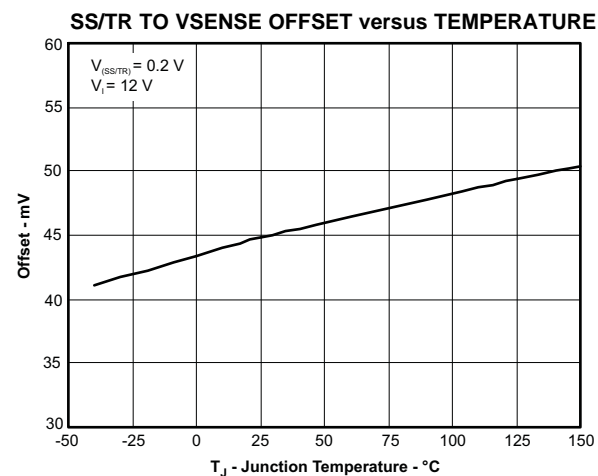


Figure 24.

OVERVIEW

The TPS54160-Q1 device is a 60-V 1.5-A step-down (buck) regulator with an integrated high-side n-channel MOSFET. To improve performance during line and load transients, the device implements a constant-frequency, current-mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency of 100 kHz to 2500 kHz allows for efficiency and size optimization when selecting the output filter components. A resistor to ground on the RT/CLK pin adjusts the switching frequency. The device has an internal phase-lock loop (PLL) on the RT/CLK pin that synchronizes the power-switch turnon to the falling edge of an external system clock.

The TPS54160-Q1 has a default start-up voltage of approximately 2.5 V. The EN pin has an internal pullup current source that one can use to adjust the input-voltage undervoltage lockout (UVLO) threshold with two external resistors. In addition, the pullup current provides a default condition. When the EN pin is floating, the device can operate. The operating current is 116 μ A when not switching and under no load. When the device is disabled, the supply current is 1.3 μ A.

The integrated 200-m Ω high-side MOSFET allows for high-efficiency power-supply designs capable of delivering 1.5-A continuous current to a load. The TPS54160-Q1 reduces the external component count by integrating the boot-recharge diode. A capacitor between the BOOT and PH pins supplies the bias voltage for the integrated high-side MOSFET. A UVLO circuit monitors the boot capacitor voltage and turns off the high-side MOSFET when the boot voltage falls below a preset threshold. The TPS54160-Q1 can operate at high duty cycles because of the boot UVLO. It is permissible to step the output voltage down to as low as the 0.8-V reference.

The TPS54160-Q1 has a power-good comparator (PWRGD), which asserts when the regulated output voltage is less than 92% or greater than 109% of the nominal output voltage. The PWRGD pin is an open-drain output which de-asserts when the VSENSE pin voltage is between 94% and 107% of the nominal output voltage, allowing the pin to transition high when using a pullup resistor.

The TPS54160-Q1 minimizes excessive output overvoltage (OV) transients by taking advantage of the OV power-good comparator. Activation of the OV comparator turns off the high-side MOSFET and masks it from turning on until the output voltage is lower than 107%.

One can use the SS/TR (slow start/tracking) pin to minimize inrush currents or provide power-supply sequencing during power up. Connect a small-value capacitor to the pin to adjust the slow-start time. Connect a resistor divider to the pin for critical power-supply sequencing requirements. Discharge of the SS/TR pin occurs before the output powers up. This discharging ensures a repeatable restart after an overtemperature fault, UVLO fault, or a disabled condition.

The TPS54160-Q1 also discharges the slow-start capacitor during overload conditions with an overload-recovery circuit. The overload-recovery circuit slow-starts the output from the fault voltage to the nominal regulation voltage after removal of a fault condition. A frequency foldback circuit reduces the switching frequency during start-up and overcurrent-fault conditions to help control the inductor current.

DETAILED DESCRIPTION

Fixed-Frequency PWM Control

The TPS54160-Q1 uses an adjustable fixed-frequency, peak-current mode control. An internal voltage reference compares the output voltage through external resistors on the VSENSE pin to an error amplifier which drives the COMP pin. An internal oscillator initiates the turn-on of the high-side power switch. The device compares the error amplifier output to the high-side power-switch current. When the power-switch current reaches the level set by the COMP voltage, the power switch turns off. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level. The device implements the Eco-mode control scheme with a minimum clamp on the COMP pin.

Slope-Compensation Output Current

The TPS54160-Q1 adds a compensating ramp to the switch-current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty-cycle range.

Pulse-Skip Eco-Mode Control Scheme

The TPS54160-Q1 operates in a pulse-skip Eco-mode control scheme at light load currents to improve efficiency by reducing switching and gate-drive losses. If the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse-skipping current threshold, the device enters Eco-mode control. This current threshold is the current level corresponding to a nominal COMP voltage of 500 mV.

When in Eco-mode, a clamp holds the COMP pin voltage at 500 mV, inhibiting the high-side MOSFET. Further decreases in load current or in output voltage cannot drive the COMP pin below the voltage level of this clamp.

Because the device is not switching, the output voltage begins to decay. As the voltage-control loop compensates for the falling output voltage, the COMP pin voltage begins to rise. At this time, the high-side MOSFET turns on, initiating a switching pulse on the next switching cycle. The COMP pin voltage sets the peak current. The output voltage recharges the regulated value (see Figure 25), then the peak switch current starts to decrease, and eventually falls below the control-scheme threshold, at which time the device again enters the Eco-mode control scheme.

For Eco-mode control-scheme operation, the TPS54160-Q1 senses peak current, not average or load current, so the load current where the device enters the Eco-mode control scheme depends on the output inductor value. For example, the circuit in Figure 51 enters the Eco-mode control scheme at about 18 mA of output current. When the load current is low and the output voltage is within regulation, the device enters a sleep mode and draws only 116 μ A of input quiescent current. The internal PLL remains operating when in sleep mode. When operating at light load currents in the pulse-skip mode, the switching transitions occur synchronously with the external clock signal.

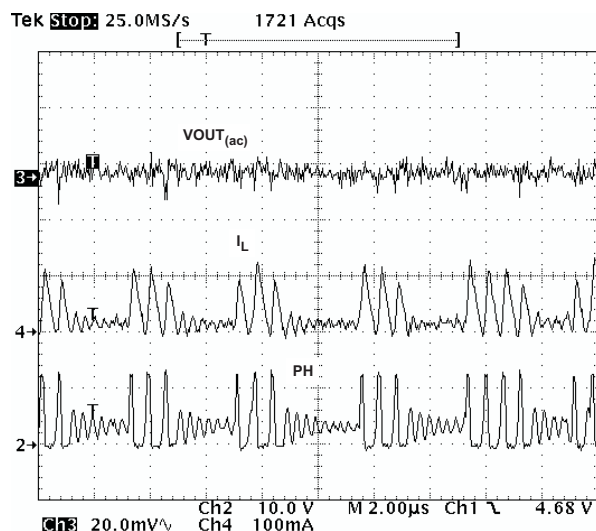


Figure 25. Pulse-Skip Mode Operation

DETAILED DESCRIPTION (continued)

Low-Dropout Operation and Bootstrap Voltage (BOOT)

The TPS54160-Q1 has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. The BOOT capacitor recharges when the high-side MOSFET is off and the low-side diode conducts. The value of this ceramic capacitor should be 0.1 μ F. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric and a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage.

To improve dropout, the TPS54160-Q1 operates at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than 2.1 V. When the voltage from BOOT to PH drops below 2.1 V, a UVLO circuit turns off the high-side MOSFET, which allows the low-side diode to conduct and refresh the charge on the BOOT capacitor. Because the supply current sourced from the BOOT capacitor is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor; thus, the effective duty cycle of the switching regulator is high.

The voltage drops across the power MOSFET, inductor resistance, low-side diode, and printed-circuit board resistance mainly influence the effective duty cycle during dropout of the regulator. During operating conditions in which the input voltage drops and the regulator is operating in continuous conduction mode, the high-side MOSFET can remain on for 100% of the duty cycle to maintain output regulation, until the BOOT-to-PH voltage falls below 2.1 V.

Pay attention in maximum-duty-cycle applications which experience extended time periods with light loads or no load. When the voltage across the BOOT capacitor falls below the 2.1-V UVLO threshold, the high-side MOSFET turns off, but there may not be enough inductor current to pull the PH pin down to recharge the BOOT capacitor. The high-side MOSFET of the regulator stops switching because the voltage across the BOOT capacitor is less than 2.1 V. The output capacitor then decays until the difference in the input voltage and output voltage is greater than 2.1 V, at this point exceeding the BOOT UVLO threshold, and the device starts switching again until the desired output voltage is reached. This operating condition persists until the input voltage and/or the load current increases. TI recommends adjusting the VIN stop voltage greater than the BOOT UVLO trigger condition at the minimum load of the application, using the adjustable VIN UVLO feature with resistors on the EN pin.

Figure 26 and Figure 27 show the start and stop voltages for typical 3.3-V and 5-V output applications. The voltages are plotted versus load current. The start-voltage definition is the input voltage needed to regulate the output within 1%. The stop-voltage definition is the input voltage at which the output drops by 5% or stops switching.

During high-duty-cycle conditions, the inductor-current ripple increases while the BOOT capacitor is being recharged, resulting in an increase in ripple voltage on the output. This is due to the recharge time of the boot capacitor being longer than the typical high-side off time when switching occurs every cycle.

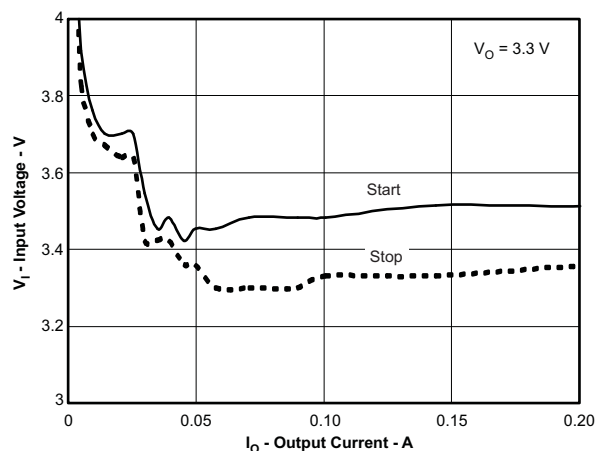


Figure 26. 3.3-V Start and Stop Voltages

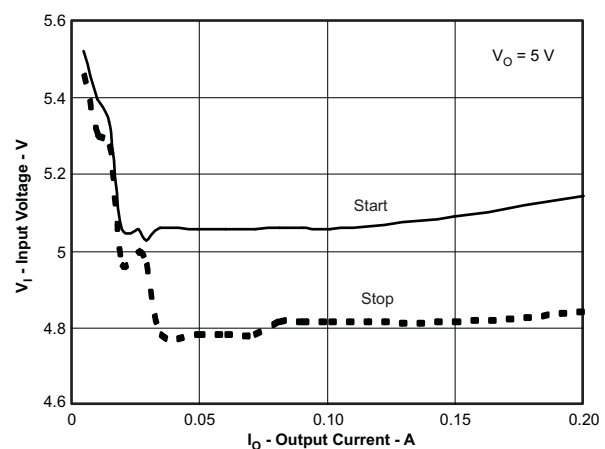


Figure 27. 5-V Start and Stop Voltages

DETAILED DESCRIPTION (continued)

Error Amplifier

The TPS54160-Q1 has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.8-V voltage reference. The transconductance (gm) of the error amplifier is 97 $\mu\text{A/V}$ during normal operation. During the slow-start operation, the transconductance is a fraction of the normal operating gm. When the voltage of the VSENSE pin is below 0.8 V and the device regulates using the SS/TR voltage, the gm is 25 $\mu\text{A/V}$.

The frequency compensation components (capacitor, series resistor, and capacitor) are added to the COMP pin to ground.

Voltage Reference

The voltage reference system produces a precise $\pm 2\%$ voltage reference over temperature by scaling the output of a temperature-stable band-gap circuit.

Adjusting the Output Voltage

A resistor divider from the output node to the VSENSE pin sets the output voltage. TI recommends using 1% tolerance or better divider resistors. Start with 10 k Ω for the R2 resistor and use [Equation 1](#) to calculate R1. To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise, and voltage errors from the VSENSE input current are noticeable.

$$R1 = R2 \times \left(\frac{V_{\text{OUT}} - 0.8 \text{ V}}{0.8 \text{ V}} \right) \quad (1)$$

Enable and Adjusting Undervoltage Lockout

The VIN pin voltage falling below 2.5 V disables the TPS54160-Q1. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in [Figure 28](#) to adjust the input voltage UVLO by using two external resistors. Though it is not necessary to use the UVLO adjust resistors, for operation TI highly recommends providing consistent power-up behavior. The EN pin has an internal pullup current source, I1, of 0.9 μA that provides the default condition of the TPS54160-Q1 operating when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, a comparator adds an additional 2.9 μA of hysteresis, I_{HYS}. This additional current facilitates input voltage hysteresis. Use [Equation 2](#) to set the external hysteresis for the input voltage. Use [Equation 3](#) to set the input start voltage.

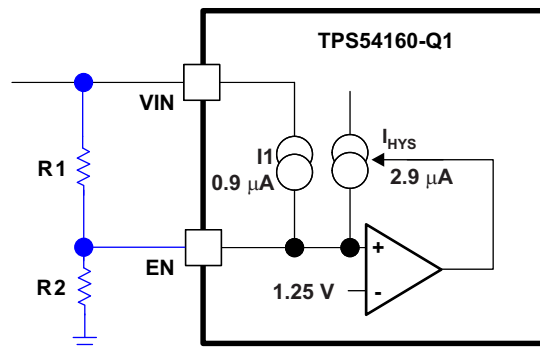


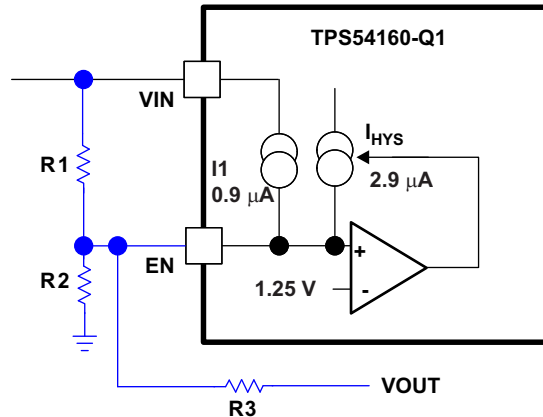
Figure 28. Adjustable Undervoltage Lockout (UVLO)

$$R1 = \frac{V_{\text{START}} - V_{\text{STOP}}}{I_{\text{HYS}}} \quad (2)$$

$$R2 = \frac{V_{\text{ENA}}}{\frac{V_{\text{START}} - V_{\text{ENA}}}{R1} + I_1} \quad (3)$$

DETAILED DESCRIPTION (continued)

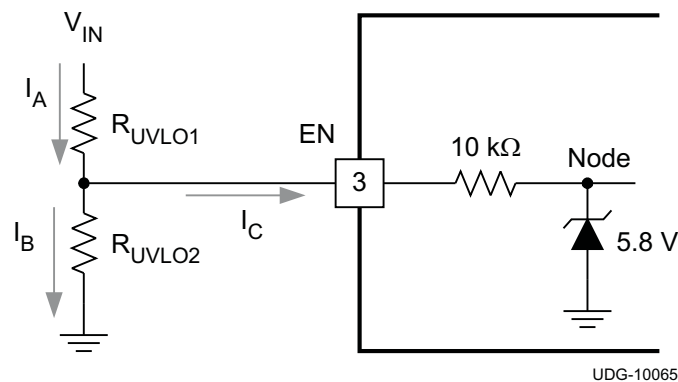
Figure 29 shows another technique to add input voltage hysteresis. One can use this method if the resistance values are high from the previous method and there is a need for wider voltage hysteresis. The resistor R3 sources additional hysteresis current into the EN pin.

**Figure 29. Adding Additional Hysteresis**

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS} + \frac{V_{OUT}}{R3}} \quad (4)$$

$$R2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1 - \frac{V_{ENA}}{R3}} \quad (5)$$

Do not place a low-impedance voltage source with greater than 5 V directly on the EN pin. Do not place a capacitor directly on the EN pin if $V_{EN} > 5$ V when using a voltage divider to adjust the start and stop voltage. The node voltage, (see Figure 30) must remain equal to or less than 5.8 V. The Zener diode can sink up to 100 μ A. The EN pin voltage can be greater than 5 V if the V_{IN} voltage source has a high impedance and does not source more than 100 μ A into the EN pin.

**Figure 30. Node Voltage**

DETAILED DESCRIPTION (continued)

Slow Start or Tracking Pin (SS/TR)

The TPS54160-Q1 effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the power-supply reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow-start time. The TPS54160-Q1 has an internal pullup current source of 2 μ A that charges the external slow-start capacitor. Equation 6 shows the calculations for the slow-start time (10% to 90%). The voltage reference (V_{REF}) is 0.8 V and the slow-start current (I_{SS}) is 2 μ A. The slow-start capacitor should be less than 0.47 μ F and greater than 0.47 nF.

$$C_{SS} \text{ (nF)} = \frac{T_{SS} \text{ (ms)} \times I_{SS} \text{ (}\mu\text{A)}}{V_{REF} \text{ (V)} \times 0.8} \quad (6)$$

At power up, the TPS54160-Q1 does not start switching until the slow-start pin discharges to less than 40 mV; to ensure a proper power up, see Figure 31.

Also, during normal operation, the TPS54160-Q1 stops switching and SS/TR must discharge to 40 mV on exceeding the VIN UVLO, pulling the EN pin below 1.25 V, or a thermal shutdown event.

The VSENSE voltage follows the SS/TR pin voltage with a 45-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% on the internal reference voltage, the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference (see Figure 23). The SS/TR voltage ramps linearly until clamped at 1.7 V.

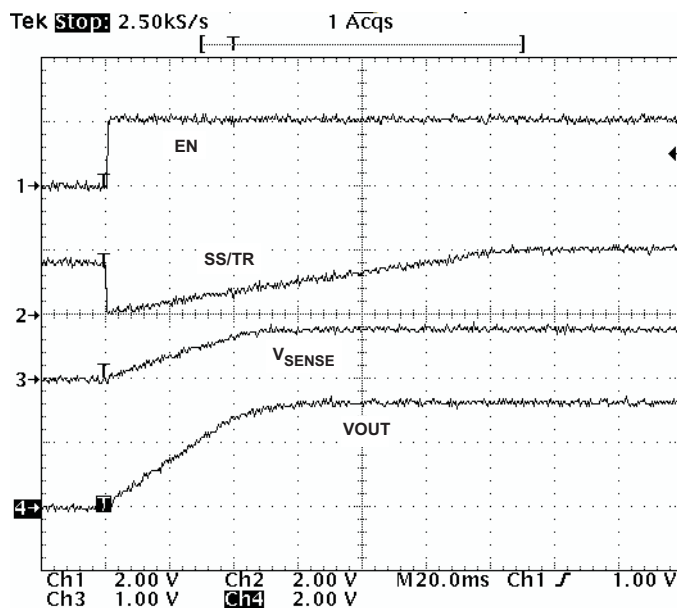


Figure 31. Operation of SS/TR Pin When Starting

Overload Recovery Circuit

The TPS54160-Q1 has an overload recovery (OLR) circuit. The OLR circuit slow-starts the output from the overload voltage to the nominal regulation voltage on removal of the fault condition. The OLR circuit discharges the SS/TR pin to a voltage slightly greater than the VSENSE pin voltage using an internal pulldown of 100 μ A when the error amplifier is changed to a high voltage from a fault condition. On removal of the fault condition, the output slow-starts from the fault voltage to nominal output voltage.

DETAILED DESCRIPTION (continued)

Sequencing

One can implement many of the common power-supply sequencing methods using the SS/TR, EN, and PWRGD pins. One implementation of the sequential method uses the open-drain output of a power-on-reset pin of another device. Figure 32 illustrates the sequential method using two TPS54160-Q1 devices. The power-good output connects to the EN pin on the second TPS54160-Q1, which enables the second power supply once the primary supply reaches regulation. If needed, a 1-nF ceramic capacitor on the EN pin of the second power supply provides a 1-ms start-up delay. Figure 33 shows the results of Figure 32.

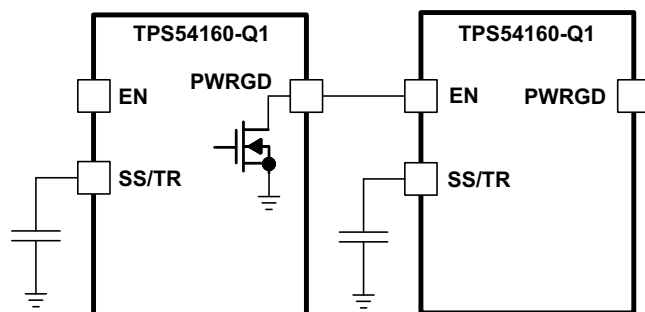


Figure 32. Schematic for Sequential Start-Up Sequence

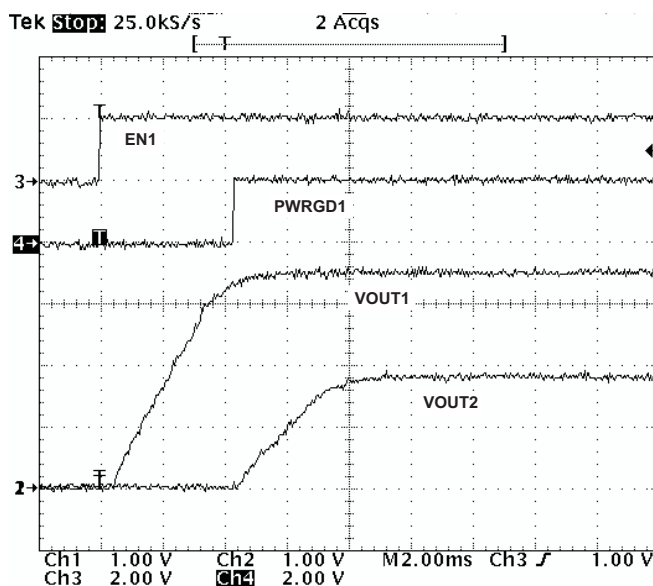


Figure 33. Sequential Startup Using EN and PWRGD

DETAILED DESCRIPTION (continued)

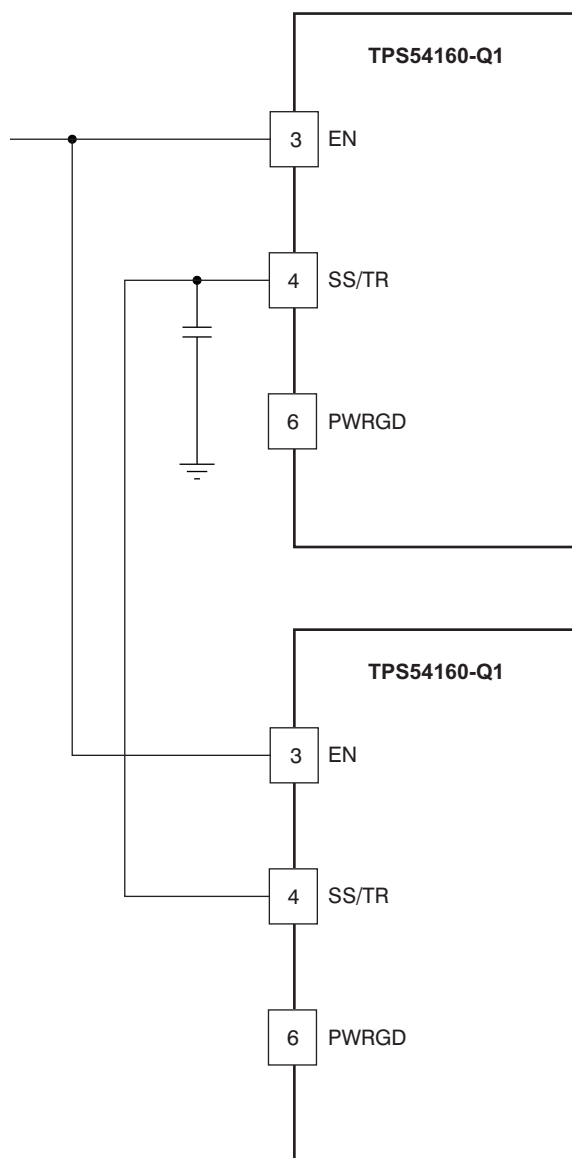


Figure 34. Schematic for Ratiometric Start-Up Using Coupled SS/TR Pins

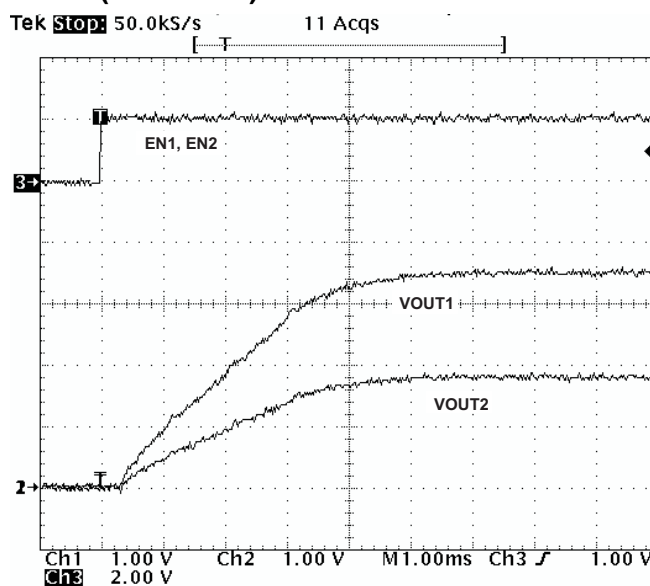
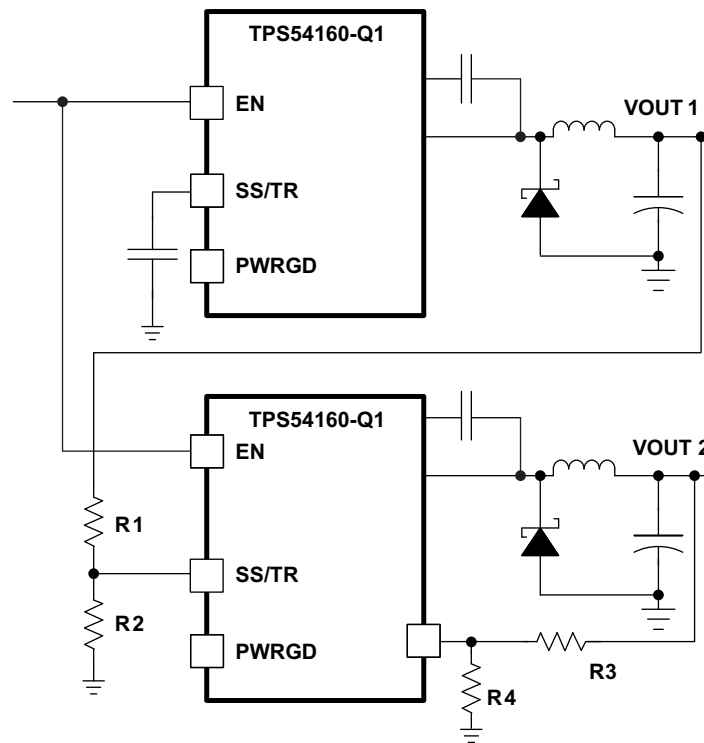


Figure 35. Ratiometric Startup Using Coupled SS/TR Pins

Figure 34 shows a method for ratiometric start-up sequence by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow-start time, the pullup double current source in Equation 6. Figure 35 shows the results of Figure 34.

DETAILED DESCRIPTION (continued)**Figure 36. Schematic for Ratiometric and Simultaneous Start-Up Sequence**

One can implement ratiometric and simultaneous power supply sequencing by connecting the resistor network of R1 and R2 shown in [Figure 36](#) to the output of the power supply to track or to another voltage-reference source. Using [Equation 7](#) and [Equation 8](#), calculate the tracking resistors to initiate Vout2 slightly before, after, or at the same time as Vout1. [Equation 9](#) is the voltage difference between Vout1 and Vout2 at the 95% point of nominal output regulation.

The ΔV variable is zero volts for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset ($V_{SSOFFSET}$) in the slow-start circuit and the offset created by the pullup current source (I_{SS}) and tracking resistors, the equations include $V_{SSOFFSET}$ and I_{SS} as variables.

To design a ratiometric start-up in which the Vout2 voltage is slightly greater than the Vout1 voltage when Vout2 reaches regulation, use a negative number in [Equation 7](#) through [Equation 9](#) for ΔV . [Equation 9](#) results in a positive number for applications in which Vout2 is slightly lower than Vout1 when achieving Vout2 regulation.

Because of the requirement to pull the SS/TR pin below 40 mV before starting after an EN, UVLO, or thermal-shutdown fault, careful selection of the tracking resistors is needed to ensure device restart after a fault. Make sure the calculated R1 value from [Equation 7](#) is greater than the value calculated in [Equation 10](#) to ensure the device can recover from a fault.

As the SS/TR voltage becomes more than 85% of the nominal reference voltage, $V_{SSOFFSET}$ becomes larger as the slow-start circuits gradually hand off the regulation reference to the internal voltage reference. The SS/TR pin voltage must be greater than 1.3 V for a complete handoff to the internal voltage reference as shown in [Figure 23](#).

$$R1 = \frac{V_{OUT2} + \Delta V}{V_{REF}} \times \frac{V_{SSOFFSET}}{I_{SS}} \quad (7)$$

$$R2 = \frac{V_{REF} \times R1}{V_{OUT2} + \Delta V - V_{REF}} \quad (8)$$

$$\Delta V = V_{OUT1} - V_{OUT2} \quad (9)$$

$$R1 > 2800 \times V_{OUT1} - 180 \times \Delta V \quad (10)$$

DETAILED DESCRIPTION (continued)

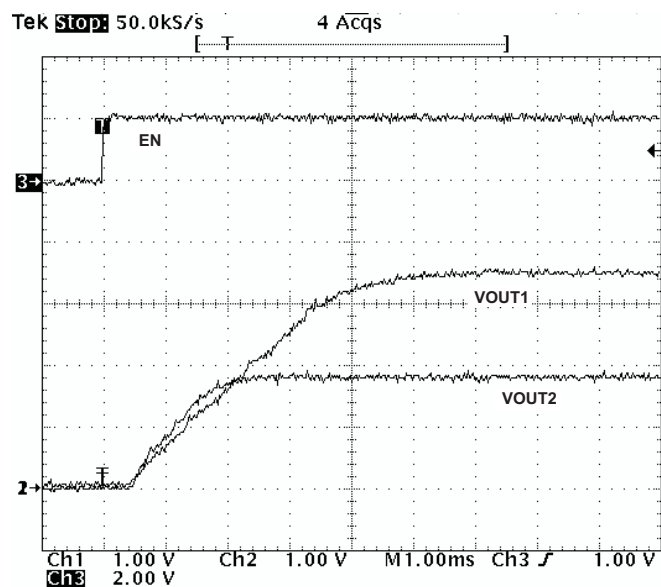


Figure 37. Ratiometric Startup With V_{OUT2} Leading V_{OUT1}

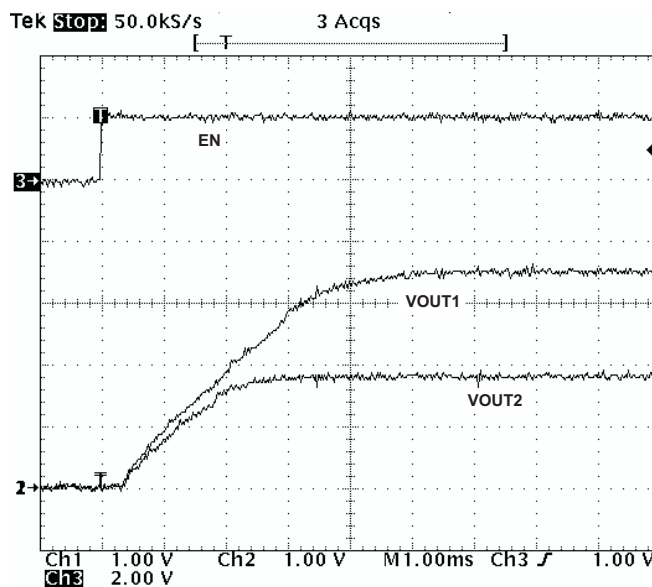


Figure 38. Ratiometric Startup With V_{OUT1} Leading V_{OUT2}

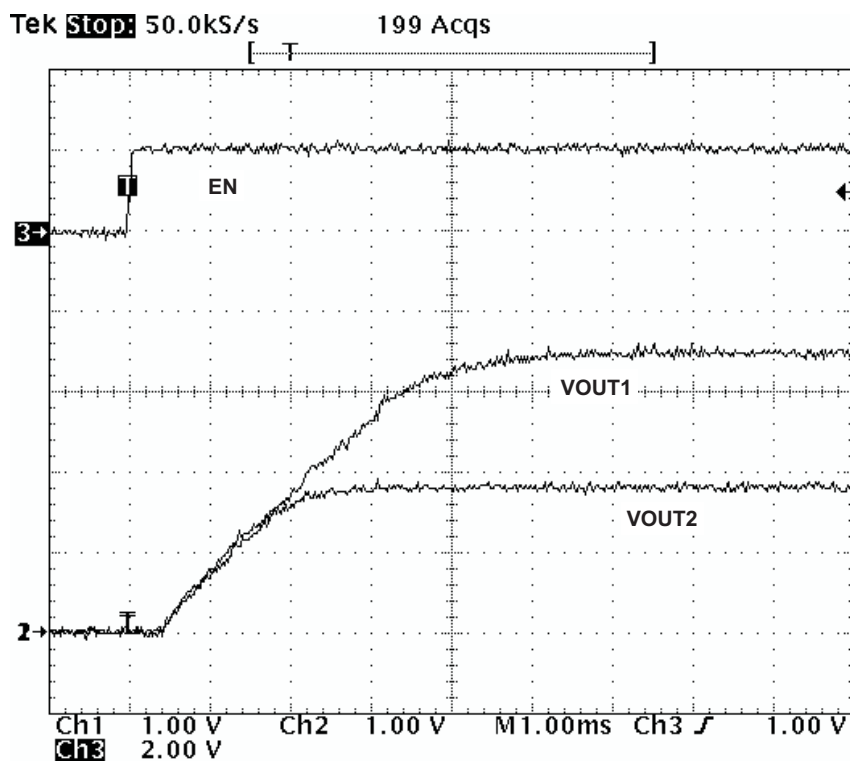


Figure 39. Simultaneous Startup With Tracking Resistor

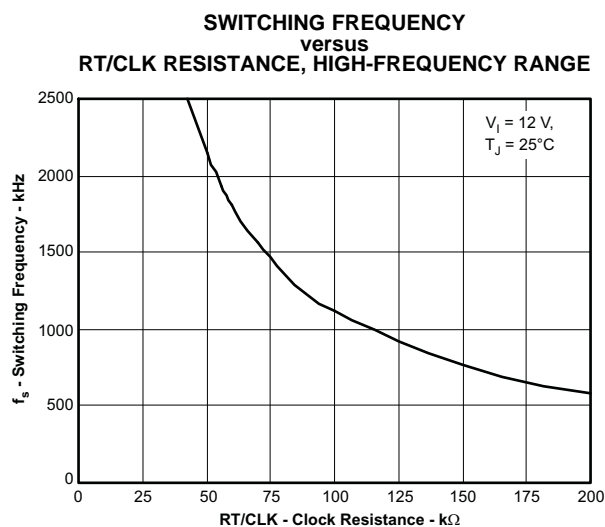
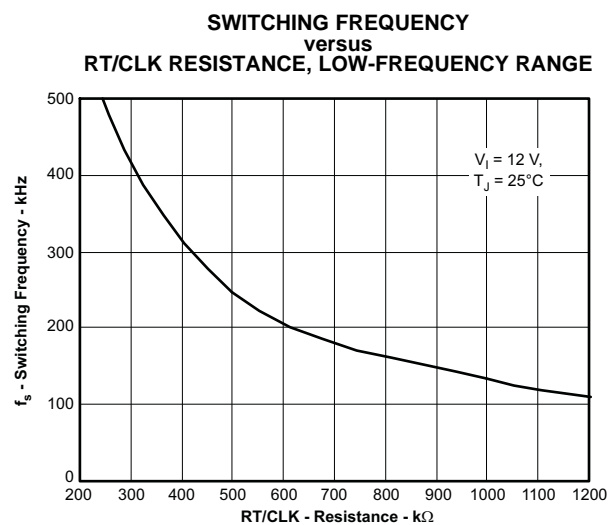
DETAILED DESCRIPTION (continued)**Constant Switching Frequency and Timing Resistor (RT/CLK Pin)**

The switching frequency of the TPS54160-Q1 is adjustable over a wide range from approximately 100 kHz to 2500 kHz by placing a resistor on the RT/CLK pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 11 or the curves in Figure 40 or Figure 41. To reduce the solution size, one would typically set the switching frequency as high as possible, but consider tradeoffs of the supply efficiency, maximum input voltage, and minimum controllable on-time.

The minimum controllable on-time is typically 130 ns and limits the maximum operating input voltage.

The frequency-shift circuit also limits the maximum switching frequency. More discussion on the details of the maximum switching frequency follows.

$$R_T \text{ (k}\Omega\text{)} = \frac{206033}{f_{SW} \text{ (kHz)}^{1.0888}} \quad (11)$$

**Figure 40. High-Range RT****Figure 41. Low-Range RT****Overcurrent Protection and Frequency Shift**

The TPS54160-Q1 implements current-mode control, which uses the COMP pin voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. Each cycle has a comparison of the switch current and COMP pin voltage; when the peak switch current intersects the COMP voltage, the high-side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. There is an internal clamp on the error-amplifier output, which functions as a switch-current limit.

To increase the maximum operating switching frequency at high input voltages, the TPS54160-Q1 implements a frequency shift. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 V to 0.8 V on the VSENSE pin.

The device implements a digital frequency shift to enable synchronizing to an external clock during normal start-up and fault conditions. Because the device can divide the switching frequency only by 8, there is a maximum input-voltage limit at which the device operates and can maintain frequency-shift protection.

During short-circuit events (particularly with high-input-voltage applications), the control loop has a finite minimum controllable on-time and the output has a low voltage. During the switch-on time, the inductor current ramps to the peak current limit because of the high input voltage and minimum on-time. During the switch-off time, the inductor would normally not have enough off-time and output voltage for the inductor to ramp down by the ramp-up amount. The frequency shift effectively increases the off-time, allowing the current to ramp down.

DETAILED DESCRIPTION (continued)

Selecting the Switching Frequency

The selected switching frequency should be the lower value of the two equations, [Equation 12](#) and [Equation 13](#). [Equation 12](#) is the maximum switching frequency limitation set by the minimum controllable on time. Setting the switching frequency above this value causes the regulator to skip switching pulses.

[Equation 13](#) is the maximum switching-frequency limit set by the frequency-shift protection. To have adequate output short-circuit protection at high input voltages, set the switching frequency to be less than the $f_{sw(maxshift)}$ frequency. In [Equation 13](#), to calculate the maximum switching frequency one must take into account that as the output voltage decreases from the nominal voltage to 0 volts, the f_{div} integer increases from 1 to 8 corresponding to the frequency shift.

In [Figure 42](#), the solid line illustrates a typical safe operating area regarding frequency shift and assumes the output voltage is zero volts, the resistance of the inductor is 0.1 Ω , the FET on-resistance is 0.2 Ω , and the diode voltage drop is 0.5 V. The dashed line is the maximum switching frequency to avoid pulse skipping. Enter these equations in a spreadsheet or other software or use the SwitcherPro design software to determine the switching frequency.

$$f_{SW(maxskip)} = \frac{1}{t_{ON}} \times \left(\frac{I_L \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_L \times R_{DS(on)} + V_d} \right) \quad (12)$$

$$f_{SWshift} = \frac{f_{DIV}}{t_{ON}} \times \left(\frac{I_L \times R_{dc} + V_{OUT(sc)} + V_d}{V_{IN} - I_L \times R_{DS(on)} + V_d} \right) \quad (13)$$

I_L	Inductor current
R_{dc}	Inductor resistance
V_{IN}	Maximum input voltage
V_{OUT}	Output voltage
V_{OUTSC}	Output voltage during short
V_d	Diode voltage drop
$R_{DS(on)}$	Switch on-resistance
t_{ON}	Controllable on-time
f_{DIV}	Frequency divide; equals (1, 2, 4, or 8)

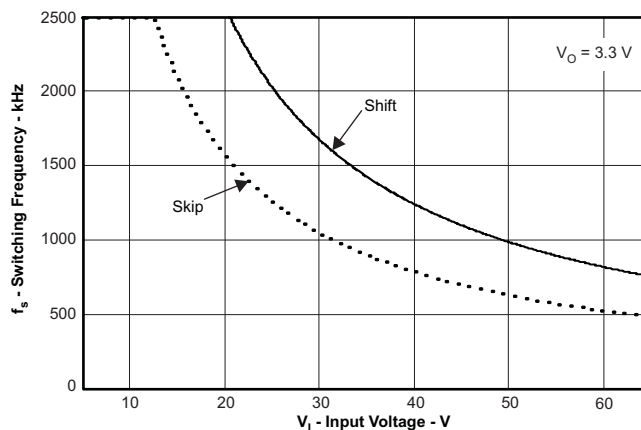


Figure 42. Maximum Switching Frequency versus Input Voltage

DETAILED DESCRIPTION (continued)

How to Interface to the RT/CLK Pin

One can use the RT/CLK pin to synchronize the regulator to an external system clock. To implement the synchronization feature, connect a square wave to the RT/CLK pin through the circuit network shown in Figure 43. The square-wave amplitude must transition lower than 0.5 V and higher than 2.2 V on the RT/CLK pin and have an on-time greater than 40 ns and an off-time greater than 40 ns. The synchronization frequency range is 300 kHz to 2200 kHz. The rising edge of PH is synchronized to the falling edge of the RT/CLK pin signal. Design the external synchronization circuit in such a way that the device has the default-frequency-set resistor connected from the RT/CLK pin to ground should the synchronization signal turn off. It is recommended to use a frequency-set resistor connected as shown in Figure 43 through a 50-Ω resistor to ground. The resistor should set the switching frequency close to the external CLK frequency. TI recommends to ac-couple the synchronization signal through a 10-pF ceramic capacitor to the RT/CLK pin and a 4-kΩ series resistor. The series resistor reduces PH jitter in heavy-load applications when synchronizing to an external clock and in applications which transition from synchronizing mode to RT mode. The first time CLK is pulled above the CLK threshold, the device switches from the RT resistor frequency to the PLL mode. The internal 0.5-V voltage source is removed and the CLK pin becomes high-impedance as the PLL starts to lock onto the external signal. Because there is a PLL on the regulator, the switching frequency can be higher or lower than the frequency set with the external resistor. The device transitions from the resistor mode to the PLL mode and then increases or decreases the switching frequency until the PLL locks onto the CLK frequency within 100 μs.

When the device transitions from the PLL mode to the resistor mode, the switching frequency slows down from the CLK frequency to 150 kHz; then reapply the 0.5-V voltage and the resistor then sets the switching frequency. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 V to 0.8 V on the VSENSE pin. The device implements a digital-frequency shift to enable synchronizing to an external clock during normal start-up and fault conditions. Figure 44, Figure 45, and Figure 46 show the device synchronized to an external system clock in continuous-conduction mode (CCM), discontinuous-conduction mode (DCM), and pulse-skip mode (PSM).

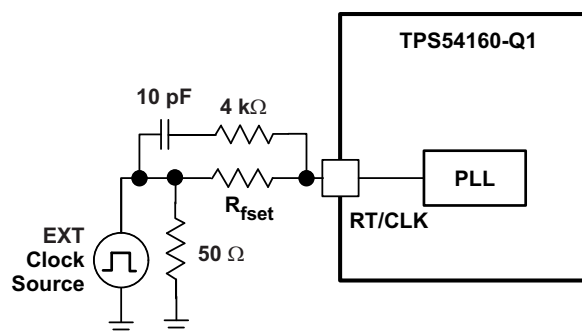


Figure 43. Synchronizing to a System Clock

DETAILED DESCRIPTION (continued)

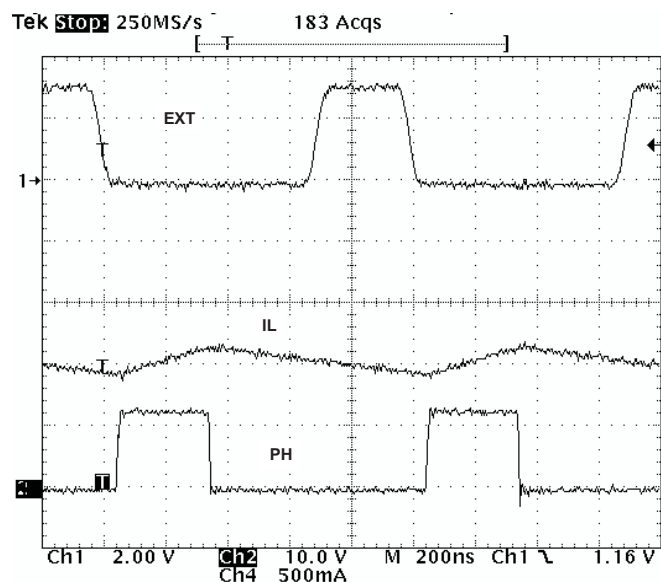


Figure 44. Plot of Synchronizing in CCM

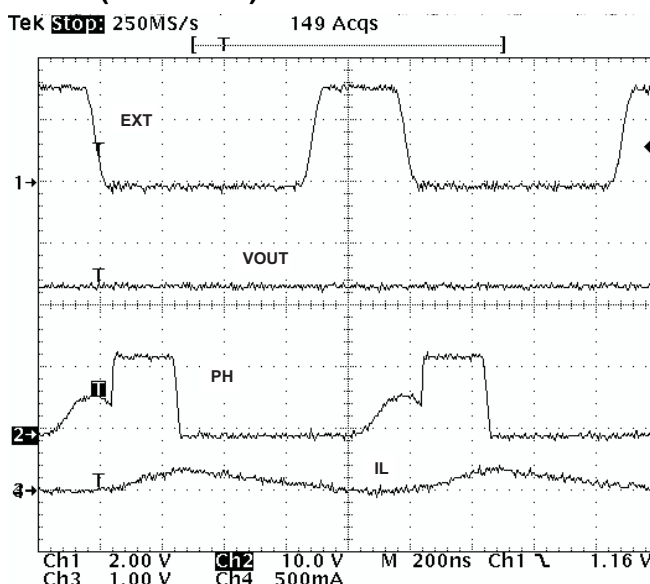


Figure 45. Plot of Synchronizing in DCM

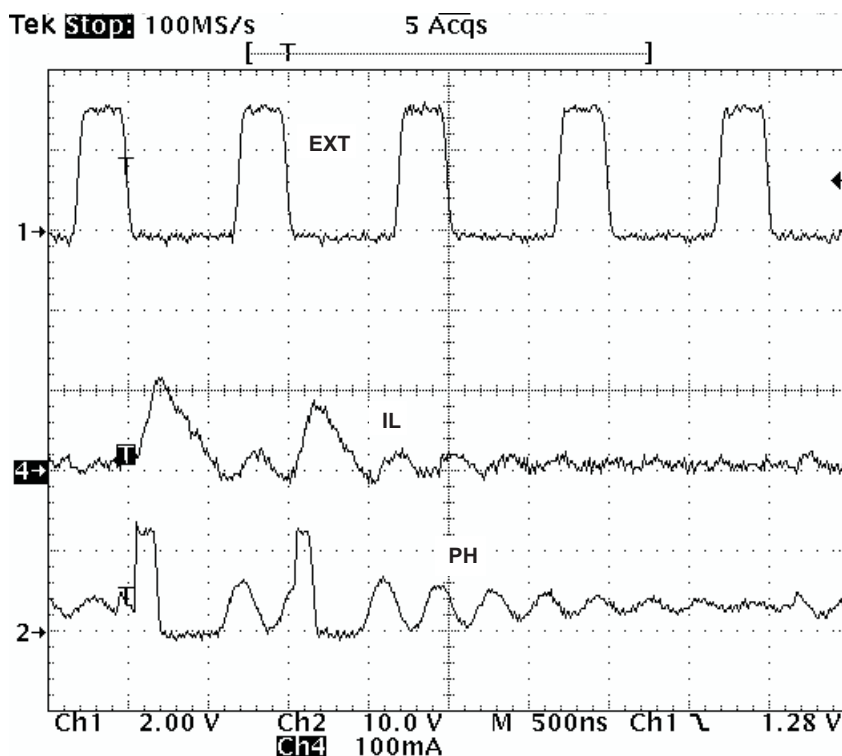


Figure 46. Plot of Synchronizing in PSM

Power-Good (PWRGD Pin)

The PWRGD pin is an open-drain output. Once the VSENSE pin is between 94% and 107% of the internal voltage reference, de-assertion of the PWRGD pin occurs, and the pin floats. TI recommends using a pullup resistor between the values of 1 k Ω and 100 k Ω to a voltage source that is 5.5 V or less. PWRGD is in a defined state once the VIN input voltage is greater than 1.5 V, but with reduced current-sinking capability. PWRGD achieves full current-sinking capability as the VIN input voltage approaches 3 V.

DETAILED DESCRIPTION (continued)

The PWRGD pin is pulled low when the VSENSE is lower than 92% or greater than 109% of the nominal internal reference voltage. Also, PWRGD is pulled low if UVLO or thermal shutdown is asserted or EN is pulled low.

Overvoltage Transient Protection

The TPS54160-Q1 incorporates an overvoltage-transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power-supply designs with low-value output capacitance. For example, with the power-supply output overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier responds by clamping the error-amplifier output to a high voltage, thus requesting the maximum output current. On removal of the condition, the regulator output rises and the error amplifier output transitions to the steady-state duty cycle. In some applications, the power-supply output voltage can respond faster than the error-amplifier output can respond; this actuality leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot, when using a low-value output capacitor, by implementing a circuit to compare the VSENSE pin voltage to OVTP threshold, which is 109% of the internal voltage reference. The VSENSE pin voltage rising above the OVTP threshold disables the high-side MOSFET, preventing current from flowing to the output and minimizing output overshoot. The VSENSE voltage dropping below the OVTP threshold allows the high-side MOSFET to turn on at the next clock cycle.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 182°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 182°C, the device reinitiates the power-up sequence by discharging the SS/TR pin.

Small-Signal Model for Loop Response

Figure 47 shows an equivalent model for the TPS54160-Q1 control loop, which can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a $g_{m_{EA}}$ of 97 $\mu A/V$. One can model the error amplifier using an ideal voltage-controlled current source. Resistor R_O and capacitor C_O model the open-loop gain and frequency response of the amplifier. The 1-mV ac voltage source between nodes a and b effectively breaks the control loop for the frequency-response measurements. Plotting c / a shows the small-signal response of the frequency compensation. Plotting a / b shows the small-signal response of the overall loop. One can check the dynamic loop response by replacing R_L with a current source with the appropriate load-step amplitude and step rate in a time-domain analysis. This equivalent model is only valid for continuous-conduction-mode designs.

DETAILED DESCRIPTION (continued)

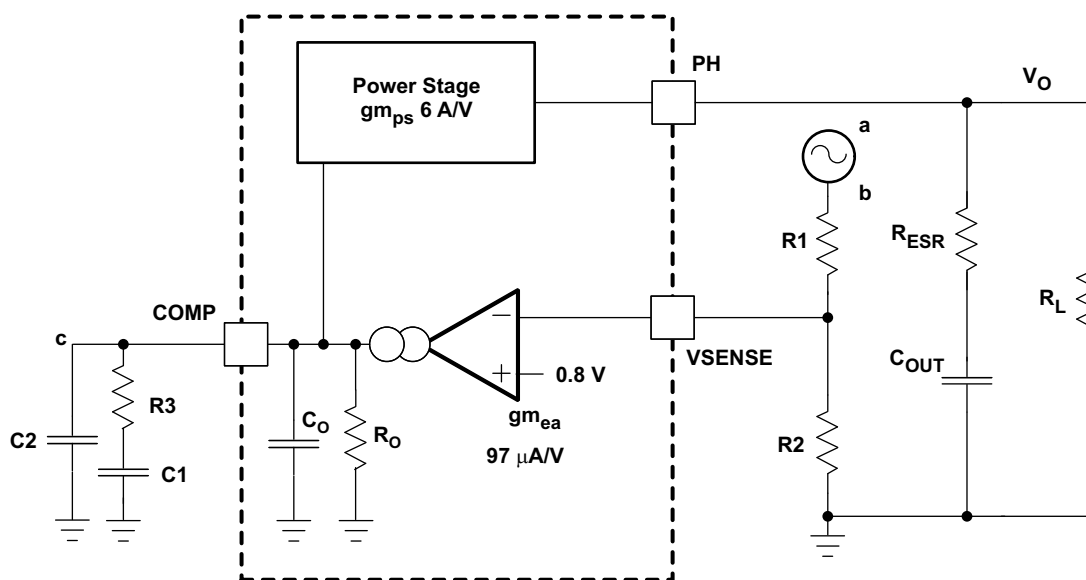


Figure 47. Small-Signal Model for Loop Response

Simple Small-Signal Model for Peak-Current-Mode Control

Figure 48 describes a simple small-signal model that one can use to understand how to design the frequency compensation. A voltage-controlled current source (duty-cycle modulator) supplying current to the output capacitor and load resistor can approximate the TPS54160-Q1 power stage. Equation 14 shows the control-to-output transfer function, which consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 47) is the power-stage transconductance. The $g_{m_{ps}}$ for the TPS54160-Q1 is 6 A/V. The low-frequency gain of the power-stage frequency response is the product of the transconductance and the load resistance as shown in Equation 15.

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 16). The dashed line in the right half of Figure 48 highlights the combined effect. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions, which makes it easier to design the frequency compensation. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency-compensation design. Using high-ESR aluminum electrolytic capacitors may reduce the number of frequency-compensation components needed to stabilize the overall loop, because the phase margin increases from the ESR zero at the lower frequencies (see Equation 17).

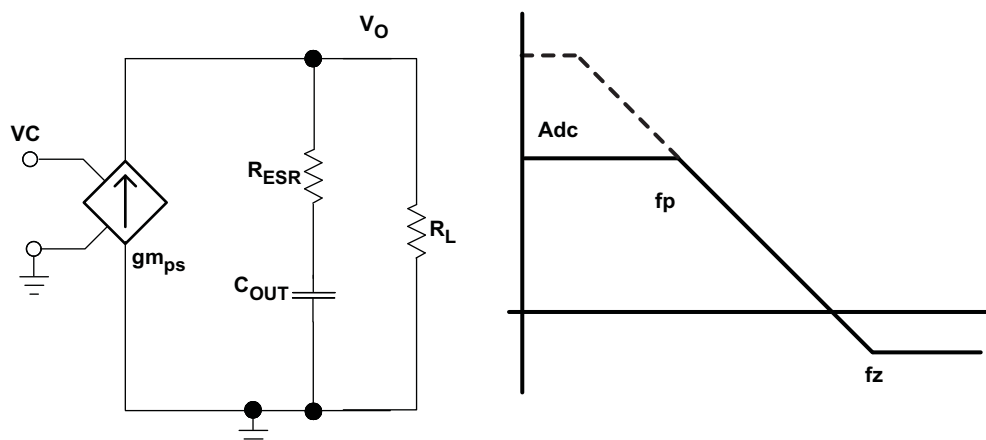


Figure 48. Simple Small-Signal Model and Frequency Response for Peak-Current-Mode Control

DETAILED DESCRIPTION (continued)

$$\frac{V_{OUT}}{V_C} = A_{dc} \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (14)$$

$$A_{dc} = g_{m_{ps}} \times R_L \quad (15)$$

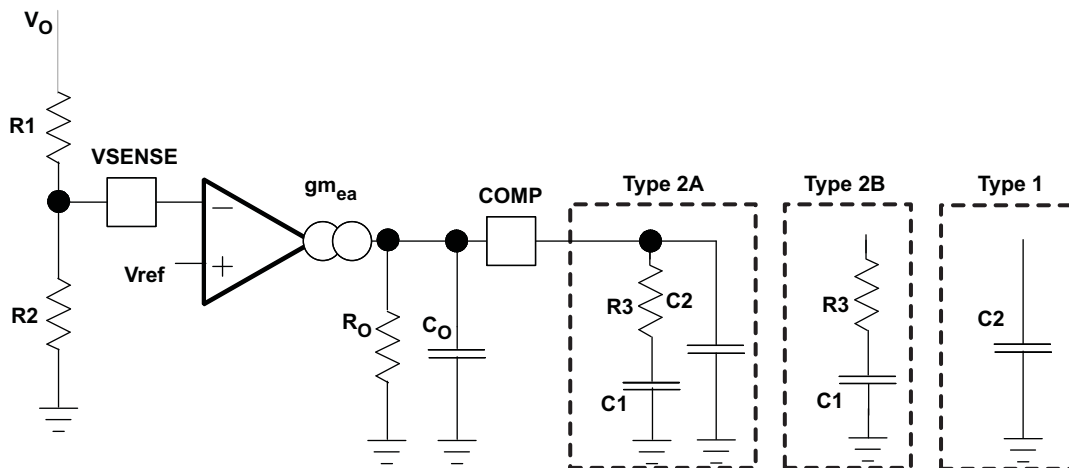
$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (16)$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (17)$$

Small-Signal Model for Frequency Compensation

The TPS54160-Q1 uses a transconductance amplifier for the error amplifier and readily supports three of the commonly-used frequency compensation circuits. Figure 49 shows compensation circuits Type 2A, Type 2B, and Type 1. Type 2 circuit implementation is most likely in high-bandwidth power-supply designs using low-ESR output capacitors. The Type 1 circuit is for power-supply designs with high-ESR aluminum electrolytic or tantalum capacitors. Equation 18 and Equation 19 show how to relate the frequency response of the amplifier to the small-signal model in Figure 49. Modeling of the open-loop gain and bandwidth uses R_O and C_O , shown in Figure 49. See the application section for a design example using a Type 2A network with a low-ESR output capacitor.

Those who prefer to compensate using the preferred methods should see Equation 18 through Equation 27 as a reference. Those who prefer to use the prescribed method use the method outlined in the *Application Information* section or use switched information.

**Figure 49. Types of Frequency Compensation**

DETAILED DESCRIPTION (continued)

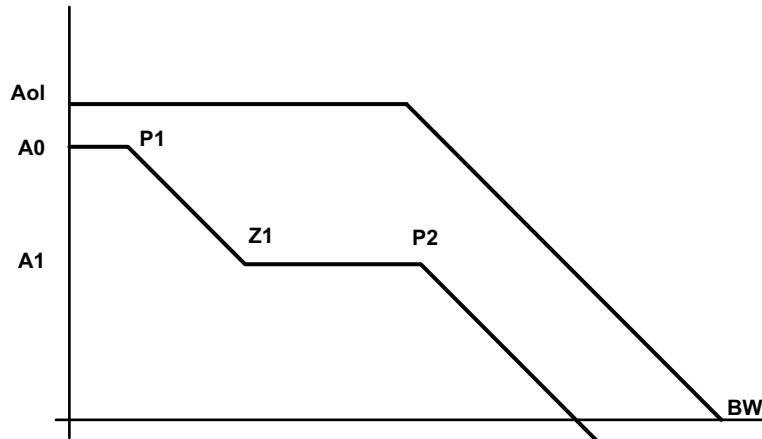


Figure 50. Frequency Response of the Type 2A and Type 2B Frequency Compensation

$$R_o = \frac{A_{ol}(V/V)}{g_{m_{ea}}} \quad (18)$$

$$C_{OUT} = \frac{g_{m_{ea}}}{2\pi \times BW \text{ (Hz)}} \quad (19)$$

$$EA = A_0 \times \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{P2}}\right)} \quad (20)$$

$$A_0 = g_{m_{ea}} \times R_o \times \frac{R_2}{R_1 + R_2} \quad (21)$$

$$A_1 = g_{m_{ea}} \times R_o || R_3 \times \frac{R_2}{R_1 + R_2} \quad (22)$$

$$P_1 = \frac{1}{2\pi \times R_o \times C_1} \quad (23)$$

$$Z_1 = \frac{1}{2\pi \times R_3 \times C_1} \quad (24)$$

$$P_2 = \frac{1}{2\pi \times R_3 || R \times (C_2 + C_{OUT})} \text{ type 2a} \quad (25)$$

$$P_2 = \frac{1}{2\pi \times R_3 || R \times C_{OUT}} \text{ type 2b} \quad (26)$$

$$P_2 = \frac{1}{2\pi \times R \times (C_2 + C_{OUT})} \text{ type 1} \quad (27)$$

APPLICATION INFORMATION

Design Guide — Step-By-Step Design Procedure

This example details the design of a high-frequency switching-regulator design using ceramic output capacitors. One must know a few parameters to start the design process. Determination of these parameters is typically at the system level. For this example, start with the following known parameters:

Output voltage	3.3 V
Transient response, 0 to 1.5-A load step	$\Delta V_{out} = 4\%$
Maximum output current	1.5 A
Input voltage	12 V (nom), 8 V to 18 V
Output-voltage ripple	$< 33 \text{ mV}_{pp}$
Start input voltage (rising VIN)	7.25 V
Stop input voltage (falling VIN)	6.25 V

Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user wants to choose the highest switching frequency possible, because this produces the smallest solution size. The high switching frequency allows for lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The minimum on-time of the internal power switch, the input voltage, the output voltage, and the frequency-shift limitation limit the selectable switching frequency.

Use [Equation 12](#) and [Equation 13](#) to find the maximum switching frequency for the regulator; choose the lower value of the two equations. Switching frequencies higher than these values result in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on-time (t_{onmin}) is 130 ns for the TPS54160-Q1. For this example, the output voltage is 3.3 V and the maximum input voltage is 18 V, which allows for a maximum switch frequency up to 1600 kHz when including the inductor resistance, on-resistance, and diode voltage in [Equation 12](#). To ensure overcurrent runaway in your design is not a concern during short circuits, use [Equation 13](#) or the solid curve in [Figure 42](#) to determine the maximum switching frequency. With a maximum input voltage of 20 V, for some margin above 18 V, assuming a diode voltage of 0.5 V, inductor resistance of 100 mΩ, switch resistance of 200 mΩ, a current-limit value of 2.7 A, the maximum switching frequency is approximately 2500 kHz.

Choosing the lower of the two values and adding some margin, a switching frequency of 1200 kHz is used. To determine the timing resistance for a given switching frequency, use [Equation 11](#) or the curve in [Figure 40](#).

Resistor RT, shown in [Figure 51](#), sets the switching frequency.

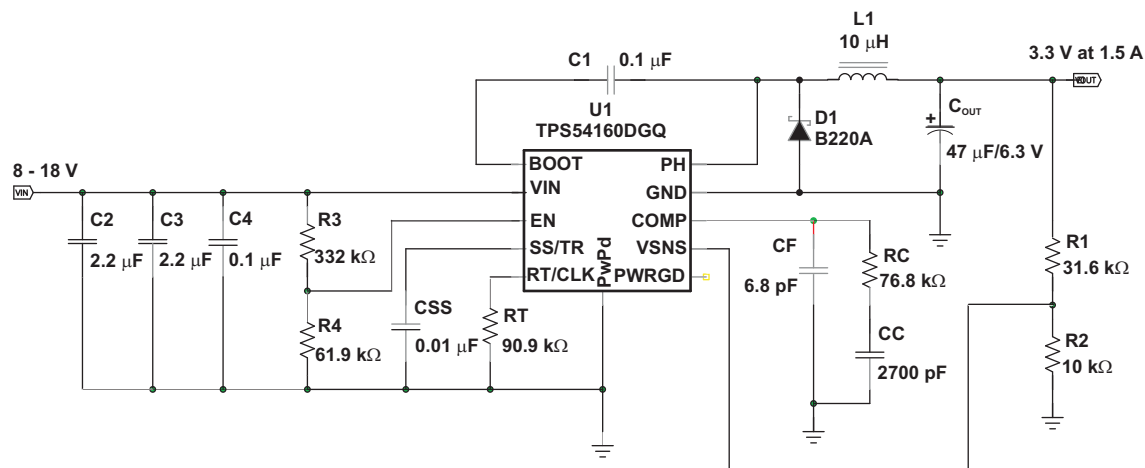


Figure 51. High-Frequency, 3.3-V Output Power-Supply Design With Adjusted UVLO

Output Inductor Selection (L_O)

To calculate the minimum value of the output inductor, use [Equation 28](#).

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

The output capacitor filters the inductor ripple current. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor, because the output capacitor must have a ripple-current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, the following guidelines may be used.

For designs using low-ESR output capacitors such as ceramics, one may use a value as high as $K_{IND} = 0.3$. When using higher-ESR output capacitors, $K_{IND} = 0.2$ yields better results. Because the inductor ripple current is part of the PWM control system, the inductor ripple current should always be greater than 100 mA for dependable operation. In a wide-input-voltage regulator, it is best to choose an inductor ripple current on the larger side. This allows the inductor to still have a measurable ripple current with the input voltage at its minimum.

For this design example, use $K_{IND} = 0.2$ and the minimum calculated inductor value is 7.6 μH . For this design, the nearest standard value was chosen: 10 μH . For the output-filter inductor, it is important not to exceed the rms-current and saturation-current ratings. One can find the rms and peak inductor current from [Equation 30](#) and [Equation 31](#).

For this design, the rms inductor current is 1.506 A and the peak inductor current is 1.62 A. The chosen inductor is a MSS6132-103. It has a saturation-current rating of 1.64 A and an rms-current rating of 1.9 A.

As the equation set demonstrates, lower ripple currents reduce the output-voltage ripple of the regulator but require a larger value of inductance. Selecting higher ripple currents increases the output voltage ripple of the regulator but allows for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor-current level previously calculated. In transient conditions, the inductor current can increase up to the switch-current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch-current limit rather than the peak inductor current.

$$L_{O \min} = \frac{V_{inmax} - V_{out}}{I_O \times K_{IND}} \times \frac{V_{out}}{V_{inmax} \times f_{sw}} \quad (28)$$

$$I_{RIPPLE} \leq I_O \times K_{IND} \quad (29)$$

$$I_{L(rms)} = \sqrt{(I_O)^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{inmax} - V_{OUT})}{V_{inmax} \times L_O \times f_{SW}} \right)^2} \quad (30)$$

$$I_{LPeak} = I_{OUT} + \frac{I_{RIPPLE}}{2} \quad (31)$$

Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output-voltage ripple, and how the regulator responds to a large change in load current. Select the output capacitance based on the most-stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator also temporarily is not able to supply sufficient output current if there is a large fast increase in the current needs of the load, such as transitioning from no load to a full load. The regulator usually requires two or more clock cycles for the control loop to see the change in load current and output voltage and then adjust the duty cycle to react to the change. The output capacitor size must be able to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles, while only allowing a tolerable amount of droop in the output voltage. [Equation 32](#) shows the minimum output capacitance necessary to accomplish this.

Where ΔI_{out} is the change in output current, f_{sw} is the regulator switching frequency, and ΔV_{out} is the allowable change in the output voltage. For this example, the specified transient-load response is a 4% change in V_{out} for a load step from 0 A (no load) to 1.5 A (full load). For this example, $\Delta I_{out} = 1.5 - 0 = 1.5$ A and $\Delta V_{out} = 0.04 \times 3.3 = 0.132$ V. Using these numbers gives a minimum capacitance of 18.9 μ F. This value does not take the ESR of the output capacitor into account in the output-voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that should be taken into account.

The catch diode of the regulator cannot sink current, so any stored energy in the inductor produces an output-voltage overshoot when the load current rapidly decreases (see [Figure 52](#)). The output capacitor size must be able to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. The excess energy that is stored in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Use [Equation 33](#) to calculate the minimum capacitance to keep the output voltage overshoot to a desired value, where L is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_f is the final peak output voltage, and V_i is the initial capacitor voltage. For this example, the worst-case load step us from 1.5 A to 0 A. The output voltage increases during this load transition, and the stated maximum in our specification is 4% of the output voltage. This makes $V_f = 1.04 \times 3.3 = 3.432$. V_i is the initial capacitor voltage, which is the nominal output voltage of 3.3 V. Using these numbers in [Equation 33](#) yields a minimum capacitance of 25.3 μ F.

[Equation 34](#) calculates the minimum output capacitance needed to meet the output-voltage ripple specification, where f_{sw} is the switching frequency, V_{ripple} is the maximum allowable output-voltage ripple, and I_{ripple} is the inductor ripple current. [Equation 35](#) yields 0.7 μ F.

[Equation 35](#) calculates the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. [Equation 35](#) indicates the ESR should be less than 147 m Ω .

The most stringent criterion for the output capacitor is 25.3 μ F of capacitance to keep the output voltage in regulation during an unload transient.

Additional capacitance de-ratings for aging, temperature, and dc bias should be factored in, which increases this minimum value. For this example, a 47- μ F 6.3-V X7R ceramic capacitor with 5-m Ω ESR is used.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. Select an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the root-mean-square (rms) value of the maximum ripple current. Use [Equation 36](#) to calculate the rms ripple current that the output capacitor must support. For this application, [Equation 36](#) yields 64.8 mA.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (32)$$

$$C_{OUT} > L_O \times \frac{((I_{OH})^2 - (I_{OL})^2)}{((V_f)^2 - (V_i)^2)} \quad (33)$$

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\frac{V_{OUT(ripple)}}{I_{RIPPLE}} \right)} \quad (34)$$

$$R_{ESR} = \frac{V_{OUT(ripple)}}{I_{RIPPLE}} \quad (35)$$

$$I_{COUT(rms)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{\sqrt{12} \times V_{IN(max)} \times L_O \times f_{SW}} \quad (36)$$

Catch Diode

The TPS54160-Q1 requires an external catch diode between the PH pin and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{in(max)}$. The peak-current rating of the diode must be greater than the maximum inductor current. The diode should also have a low forward voltage. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, the higher the voltage and current ratings the diode has, the higher the forward voltage. Because the design example has an input voltage up to 18 V, a diode with a minimum of 20-V reverse voltage is selected.

For the example design, the B220A Schottky diode is selected for its lower forward voltage, and it comes in a larger package size, which has good thermal characteristics compared with smaller devices. The typical forward voltage of the B220A is 0.5 V.

The diode selection must also be based on an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode, which equals the conduction losses of the diode. At higher switch frequencies, one must take into account the ac losses of the diode. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery. Use [Equation 37](#) to calculate the total power dissipation, conduction losses plus ac losses, of the diode.

The B220A has a junction capacitance of 120 pF. Using [Equation 37](#), the selected diode dissipates 0.632 W. This power dissipation, depending on mounting techniques, should produce a 16°C temperature rise in the diode when the input voltage is 18 V and the load current is 1.5 A.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{(V_{IN(max)} - V_{OUT}) \times I_{OUT} \times V_{fd}}{V_{IN(max)}} + \frac{C_j \times f_{SW} \times (V_{IN} + V_{fd})^2}{2} \quad (37)$$

Input Capacitor

The TPS54160-Q1 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 3-μF effective capacitance and, in some applications, a bulk capacitance. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple-current rating greater than the maximum input-current ripple of the TPS54160-Q1. One can calculate the input ripple current using [Equation 38](#).

The value of a ceramic capacitor varies significantly over temperature and the amount of dc bias applied to the capacitor. One can minimize the capacitance variations due to temperature by selecting a dielectric material that is stable over temperature. Designers usually select X5R and X7R ceramic dielectrics for power-regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. Also select the output capacitor with the dc bias taken into account. The capacitance value of a capacitor decreases as the dc bias across a capacitor increases.

This example design requires a ceramic capacitor with at least a 20-V voltage rating to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V, and 100 V, so select a 25-V capacitor. The selection for this example is two 2.2-μF 25-V capacitors in parallel. [Table 1](#) shows a selection of high-voltage capacitors. The input capacitance value determines the input ripple voltage of the regulator. One can calculate the input voltage ripple using [Equation 39](#). Using the design example values, $I_{outmax} = 1.5\text{ A}$, $C_{in} = 4.4\text{ }\mu\text{F}$, $f_{sw} = 1200\text{ kHz}$, yields an input voltage ripple of 71 mV and an rms input ripple current of 0.701 A.

$$I_{cirms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{in\ min}}} \times \frac{(V_{in\ min} - V_{out})}{V_{in\ min}} \quad (38)$$

$$\Delta V_{in} = \frac{I_{out\ max} \times 0.25}{C_{in} \times f_{sw}} \quad (39)$$

Table 1. Capacitor Types

VENDOR	VALUE (μF)	EIA SIZE	VOLTAGE	DIELECTRIC	COMMENTS
Murata	1 to 2.2	1210	100 V	X7R	GRM32 series
	1 to 4.7		50 V		
	1	1206	100 V		GRM31 series
	1 to 2.2		50 V		
Vishay	1 10 1.8	2220	50 V		VJ X7R series
	1 to 1.2		100 V		
	1 to 3.9	2225	50 V		
	1 to 1.8		100 V		
TDK	1 to 2.2	1812	100 V		C series C4532
	1.5 to 6.8		50 V		
	1 to 2.2	1210	100 V		C series C3225
	1 to 3.3		50 V		
AVX	1 to 4.7	1210	50 V		X7R dielectric series
	1		100 V		
	1 to 4.7	1812	50 V		
	1 to 2.2		100 V		

Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time required for the output voltage to reach its nominal programmed value during power up. A slow-start capacitor is useful if a load requires a controlled voltage slew rate. A slow-start capacitor is also used if the output capacitance is large and would require large amounts of current to charge the capacitor quickly to the output-voltage level. The large currents necessary to charge the capacitor may make the TPS54160-Q1 reach the current limit, or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output-voltage slew rate solves both of these problems.

The slow-start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. One can use [Equation 40](#) to find the minimum slow-start time, t_{ss} , necessary to charge the output capacitor, C_{out} , from 10% to 90% of the output voltage, V_{out} , with an average slow-start current of I_{ssavg} . In the example, to charge the 47-μF output capacitor up to 3.3 V while only allowing the average input current to be 0.125 A requires a 1-ms slow-start time.

Once the slow-start time is known, one can calculate the slow-start capacitor value using [Equation 6](#). For the example circuit, the slow-start time is not too critical, because the output capacitor value is 47 μF, which does not require much current to charge to 3.3 V. The example circuit has the slow-start time set to an arbitrary value of 1 ms, which requires a 3.3-nF capacitor.

$$T_{ss} > \frac{C_{OUT} \times V_{OUT} \times 0.8}{I_{SSAVG}} \quad (40)$$

Bootstrap Capacitor Selection

Proper operation requires a 0.1- μ F ceramic capacitor connected between the BOOT and PH pins. TI recommends using a ceramic capacitor with X5R or better-grade dielectric. The capacitor should have a 10-V or higher voltage rating.

Undervoltage Lockout (UVLO) Set Point

One can adjust the UVLO using an external voltage divider on the EN pin of the TPS54160-Q1. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 7.25 V (enabled). After the regulator starts switching, it should continue to do so until the input voltage falls below 6.25 V (UVLO stop).

The programmable UVLO and enable voltages are set using a resistor divider between Vin and ground to the EN pin. Use [Equation 2](#) through [Equation 3](#) to calculate the resistance values necessary. The example application requires 332 k Ω between Vin and EN and 61.9 k Ω between EN and ground to produce the 7.25-V and 6.25-V start and stop voltages.

Output Voltage and Feedback Resistors Selection

For the example design, the R2 selection was 10.0 k Ω . Using [Equation 1](#), the calculated value of R1 is 31.25 k Ω . The nearest standard 1% resistor is 31.6 k Ω . Due to current leakage of the VSENSE pin, the current flowing through the feedback network should be greater than 1 μ A to maintain the output voltage accuracy. This requirement makes the maximum value of R2 equal to 800 k Ω . Choosing higher resistor values decreases quiescent current and improves efficiency at low output currents, but may introduce noise immunity problems.

Compensation

There are several industry techniques used to compensate dc-dc regulators. The method presented here yields high phase margins. For most conditions, the regulator has a phase margin between 60 and 90 degrees. The method presented here ignores the effects of the slope compensation that is internal to the TPS54160-Q1. Ignoring the slope compensation results in an actual crossover frequency that is usually lower than the crossover frequency used in the calculations.

Use SwitcherPro software for a more accurate design.

The uncompensated regulator has a dominant pole, typically located between 300 Hz and 3 kHz due to the output capacitor and load resistance, and a pole due to the error amplifier. One zero exists due to the output capacitor and the ESR. The zero-frequency is higher than either of the two poles.

If left uncompensated, the double pole created by the error amplifier and the modulator would lead to an unstable regulator. To stabilize the regulator, one pole must be canceled out. One design approach is to locate a compensating zero at the modulator pole. Then select a crossover frequency that is higher than the modulator pole. One can calculate the gain of the error amplifier to achieve the desired crossover frequency. The capacitor used to create the compensation zero, along with the output impedance of the error amplifier, form a low-frequency pole to provide a -1 slope through the crossover frequency. Then the addition of a compensating pole cancels the zero due to the output-capacitor ESR. Ignore an ESR zero that resides at a frequency higher than the switching frequency.

To compensate the TPS54160-Q1 using this method, first calculate the modulator pole and zero using the following equations:

$$f_{P(mod)} = \frac{I_{OUT(max)}}{2 \times \pi \times V_{OUT} \times C_{OUT}} \quad (41)$$

where

$I_{OUT(max)}$ is the maximum output current.

C_{OUT} is the output capacitance.

V_{OUT} is the nominal output voltage.

$$f_{Z(mod)} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} \quad (42)$$

For the example design, the modulator pole location is 1.5 kHz and the ESR zero location is 338 kHz.

Next, the designer selects a crossover frequency which determines the bandwidth of the control loop. The crossover-frequency location must be at a frequency at least five times higher than the modulator pole. The crossover frequency selection must also be such that the available gain of the error amplifier at the crossover frequency is high enough to allow for proper compensation.

Use [Equation 47](#) to calculate the maximum crossover frequency when the ESR-zero location is at a frequency that is higher than the desired crossover frequency. This usually is the case for ceramic or low-ESR tantalum capacitors. Aluminum electrolytic and tantalum capacitors typically produce a modulator zero at a low frequency due to their high ESR.

The example application uses a low-ESR ceramic capacitor with 10 mΩ of ESR, making the zero at 338 kHz.

This value is much higher than typical crossover frequencies, so the maximum crossover frequency is calculated using both [Equation 43](#) and [Equation 46](#).

Using [Equation 46](#) gives a minimum crossover frequency of 7.6 kHz and [Equation 43](#) gives a maximum crossover frequency of 45.3 kHz.

An arbitrary crossover-frequency selection from this range is 45 kHz.

For ceramic capacitors use [Equation 43](#):

$$f_{C(max)} \leq 2100 \sqrt{\frac{f_{P(mod)}}{V_{OUT}}} \quad (43)$$

For tantalum or aluminum capacitors use [Equation 44](#):

$$f_{C(max)} \leq \frac{51442}{\sqrt{V_{OUT}}} \quad (44)$$

For all cases use [Equation 45](#) and [Equation 46](#):

$$f_{C(max)} \leq \frac{f_{SW}}{5} \quad (45)$$

$$f_{C(min)} \geq 5 \times f_{P(mod)} \quad (46)$$

After selecting a crossover frequency, f_C , one can calculate the gain of the modulator at the crossover frequency using [Equation 47](#).

$$G_{MOD(f_C)} = \frac{g_{m(PS)} \times R_{LOAD} \times (2\pi \times f_C \times C_{OUT} \times R_{ESR} + 1)}{2\pi \times f_C \times C_{OUT} \times (R_{LOAD} + R_{ESR}) + 1} \quad (47)$$

For the example problem, the gain of the modulator at the crossover frequency is 0.542. Next, calculate the compensation components. Use of a resistor in series with a capacitor creates a compensating zero. A capacitor in parallel to these two components forms the compensating pole. However, calculating the values of these components varies depending on whether the ESR-zero location is above or below the crossover frequency. For ceramic or low-ESR tantalum output capacitors, the zero location is usually above the crossover frequency. For aluminum electrolytic and tantalum capacitors, the modulator zero location is usually lower in frequency than the crossover frequency. For cases where the modulator zero is higher than the crossover frequency (ceramic capacitors), the equations are:

$$R_C = \frac{V_{OUT}}{G_{MOD(f_c)} \times g_{m(EA)} \times V_{REF}} \quad (48)$$

$$C_C = \frac{1}{2\pi \times R_C \times f_{P(mod)}} \quad (49)$$

$$C_f = \frac{C_{OUT} \times R_{ESR}}{R_C} \quad (50)$$

For cases where the modulator zero is less than the crossover frequency (aluminum or tantalum capacitors), the equations are:

$$R_C = \frac{V_{OUT}}{G_{MOD(f_c)} \times f_{Z(mod)} \times g_{m(EA)} \times V_{REF}} \quad (51)$$

$$C_C = \frac{1}{2\pi \times R_C \times f_{P(mod)}} \quad (52)$$

$$C_f = \frac{1}{2\pi \times R_C \times f_{Z(mod)}} \quad (53)$$

For the example problem, the ESR zero is located at a higher frequency compared to the crossover frequency, so Equation 50 through Equation 53 are used to calculate the compensation components. In this example, the calculated components values are:

- $R_C = 76.2 \text{ k}\Omega$
- $C_C = 2710 \text{ pF}$
- $C_f = 6.17 \text{ pF}$

The calculated value of the C_f capacitor is not a standard value, so use a value of 2700 pF. Use 6.8 pF for C_C . The R_C resistor sets the gain of the error amplifier, which determines the crossover frequency. The calculated R_C resistor is not a standard value, so use 76.8 k Ω .

APPLICATION CURVES

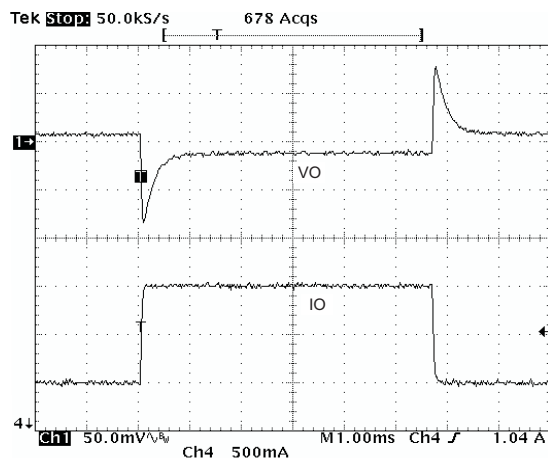


Figure 52. Load Transmit

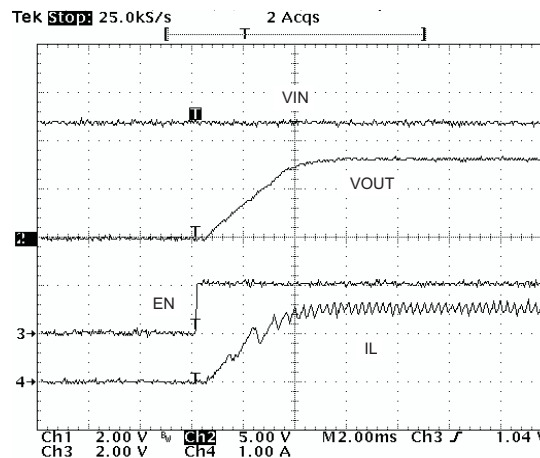


Figure 53. Startup With EN

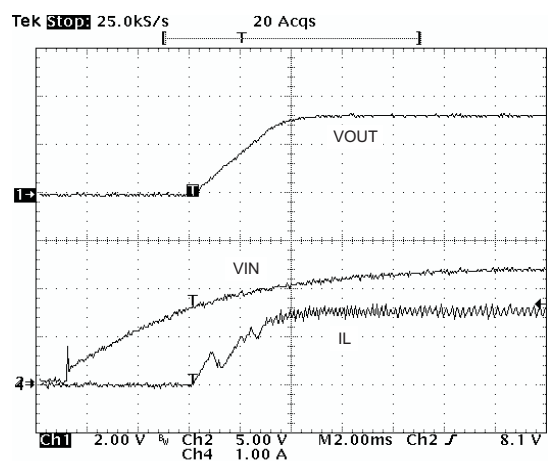


Figure 54. VIN Power Up

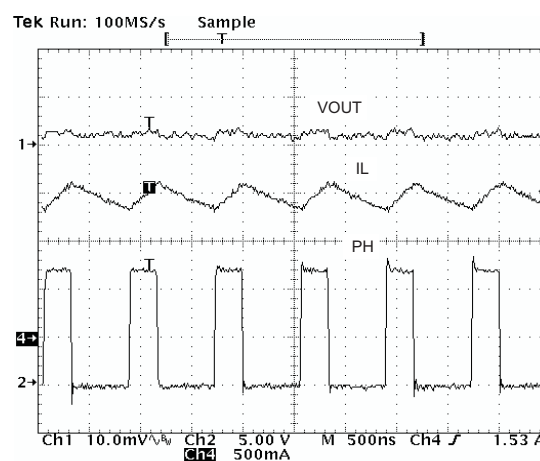


Figure 55. Output Ripple, CCM

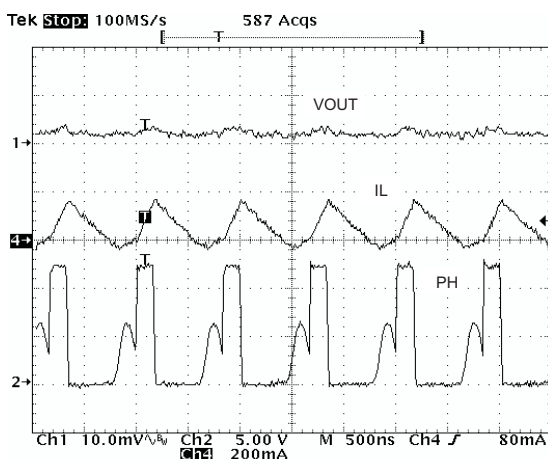


Figure 56. Output Ripple, DCM

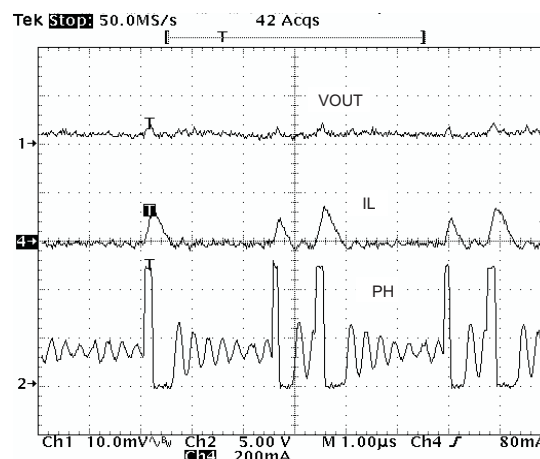


Figure 57. Output Ripple, PSM

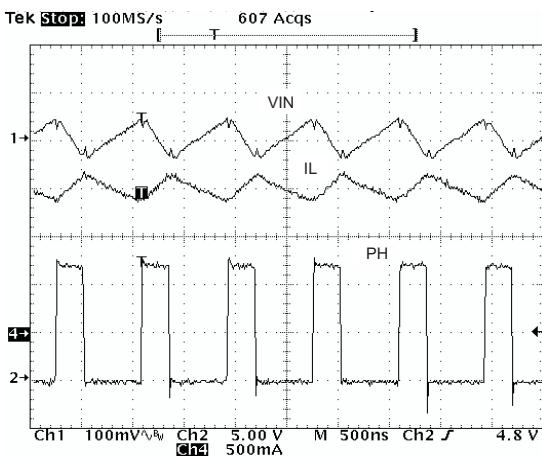


Figure 58. Input Ripple, CCM

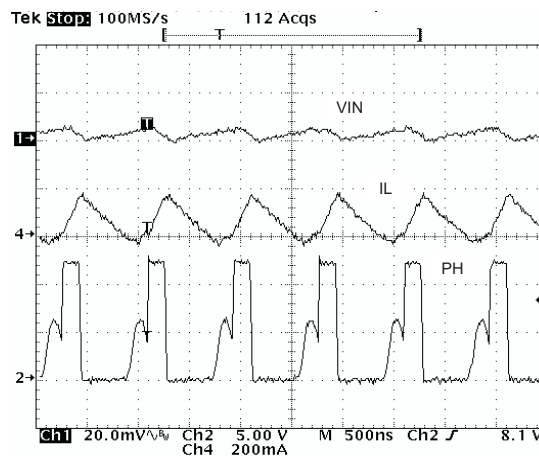


Figure 59. Input Ripple, DCM

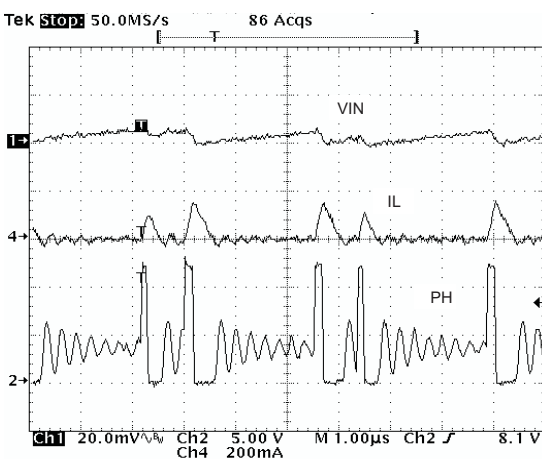


Figure 60. Input Ripple, PSM

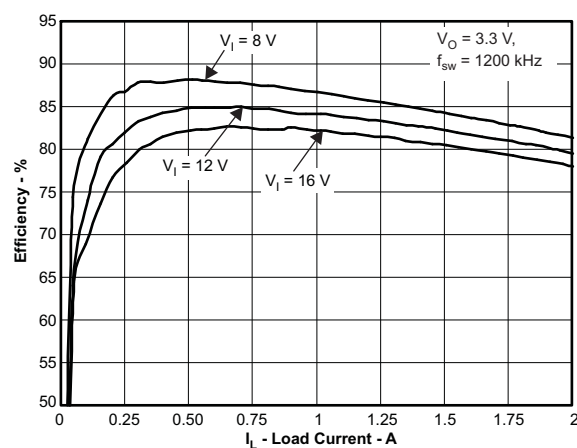


Figure 61. Efficiency versus Load Current

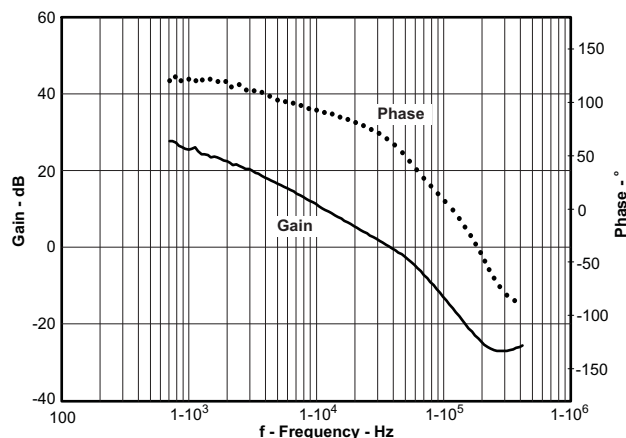


Figure 62. Overall Loop Frequency Response

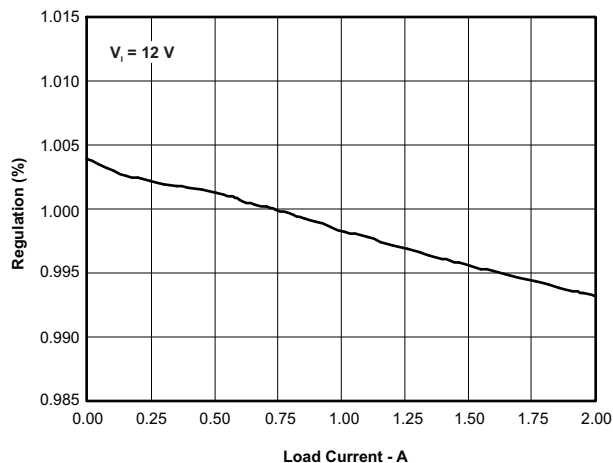
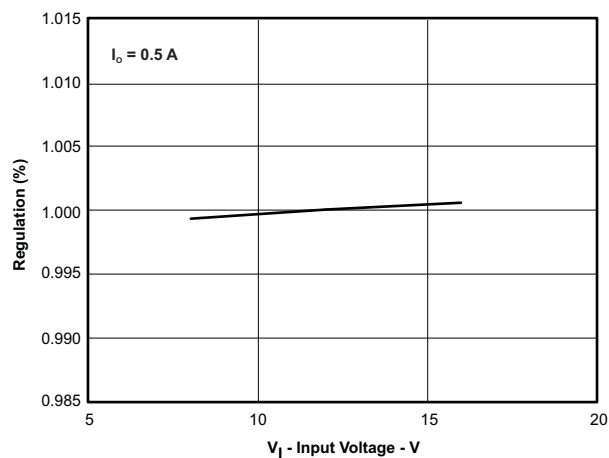


Figure 63. Regulation versus Load Current

**Figure 64. Regulation versus Input Voltage**

Power Dissipation

The following formulas show how to estimate power dissipation under continuous-conduction mode (CCM) operation. Do not use these equations if the device is working in discontinuous-conduction mode (DCM).

The power dissipation of the device includes conduction loss (P_{con}), switching loss (P_{sw}), gate-drive loss (P_{gd}), and supply-current loss (P_q).

$$P_{con} = I_O^2 \times R_{DS(on)} \times (V_{OUT} / V_{IN}) \quad (54)$$

$$P_{sw} = V_{IN}^2 \times f_{sw} \times I_O \times 0.25 \times 10^{-9} \text{sec/V} \quad (55)$$

$$P_{gd} = V_{IN} \times 3 \times 10^{-9} \text{Asec} \times f_{sw} \quad (56)$$

$$P_q = 116 \mu\text{A} \times V_{IN} \quad (57)$$

where:

I_{OUT} is the output current (A).

$r_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω).

V_{OUT} is the output voltage (V).

V_{IN} is the input voltage (V).

f_{sw} is the switching frequency (Hz).

So

$$P_{tot} = P_{con} + P_{sw} + P_{gd} + P_q \quad (58)$$

For a given T_A ,

$$T_J = T_A + \theta_{JA} \times P_{tot} \quad (59)$$

For a given $T_{J(MAX)} = 150^\circ\text{C}$

$$T_{A(MAX)} = T_{J(MAX)} - \theta_{JA} \times P_{tot} \quad (60)$$

where:

P_{tot} is the total device power dissipation (W).

T_A is the ambient temperature ($^\circ\text{C}$).

T_J is the junction temperature ($^\circ\text{C}$).

θ_{JA} is the thermal resistance of the package ($^\circ\text{C/W}$).

$T_{J(MAX)}$ is maximum junction temperature ($^\circ\text{C}$).

$T_{A(MAX)}$ is maximum ambient temperature ($^\circ\text{C}$).

There are additional power losses in the regulator circuit due to the inductor ac and dc losses, the catch diode, and trace resistance that impact the overall efficiency of the regulator.

Layout

Layout is a critical portion of good power-supply design. There are several signals paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, bypass the VIN pin to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric. Take care to minimize the loop area formed by the bypass-capacitor connections, the VIN pin, and the anode of the catch diode. See Figure 65 for a PCB layout example. Tie the GND pin directly to the thermal pad and the IC.

Connect the thermal pad to any internal PCB ground planes using multiple vias directly under the IC. Route the PH pin to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, locate the catch diode and output inductor close to the PH pins, and minimize the area of the PCB conductor to prevent excessive capacitive coupling. For operation at full-rated load, the top-side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise, so locate the RT resistor as close as possible to the IC, and route the traces to minimize their lengths. Place the additional external components approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layout. However, this layout, provided for use as a guideline, produces good results.

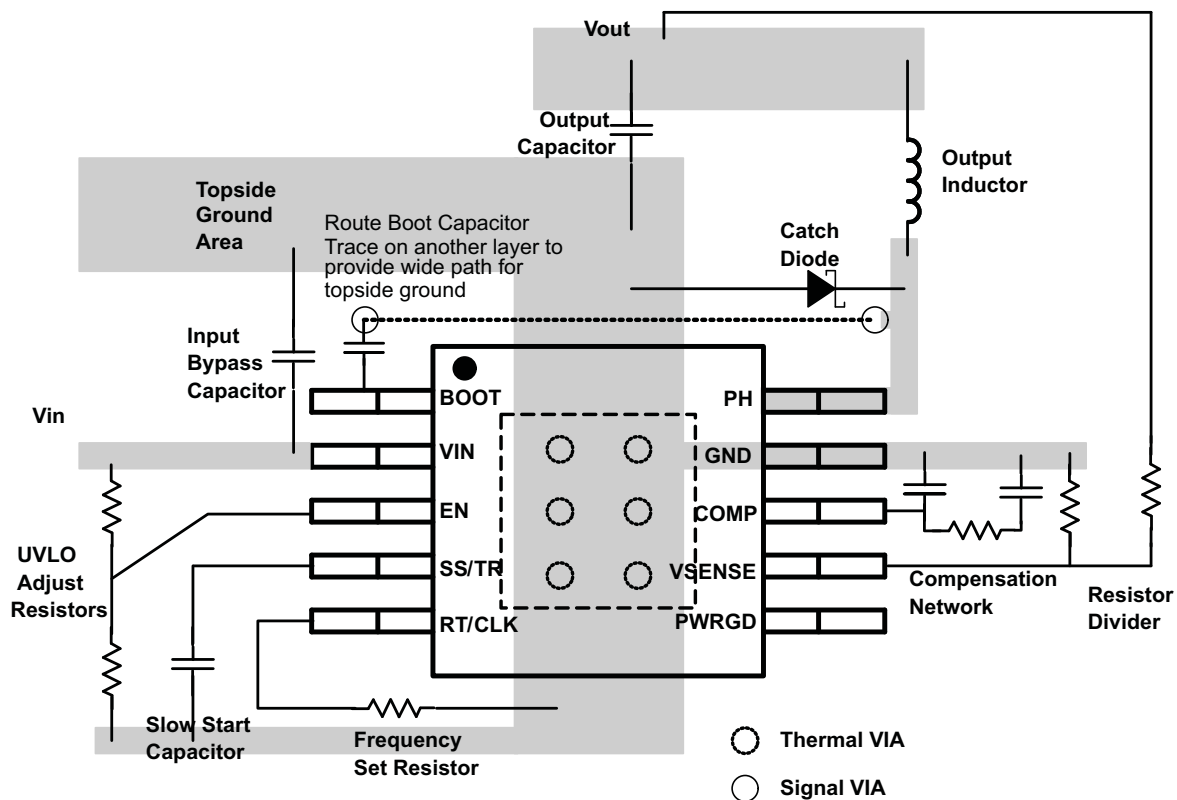


Figure 65. PCB Layout Example

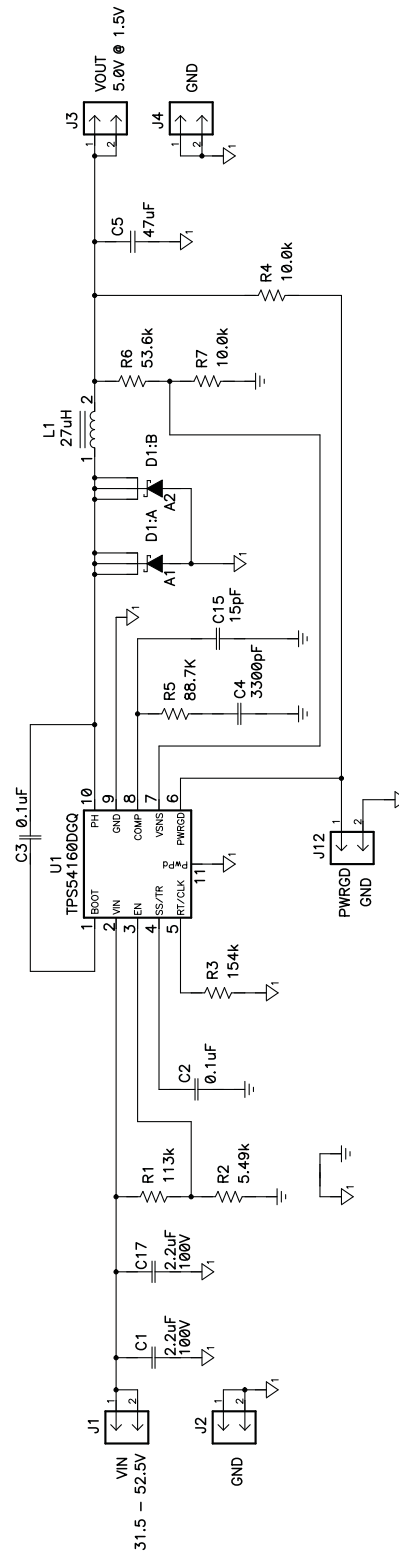


Figure 66. Wide Input Voltage Design

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54160QDGRQ1	LIFEBUY	MSOP- PowerPAD	DGQ	10		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	5416Q	
TPS54160QDRCRQ1	LIFEBUY	VSON	DRC	10		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	5416Q	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS54160-Q1 :

- Catalog: [TPS54160](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54160QDGQRQ1	MSOP-Power PAD	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS54160QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

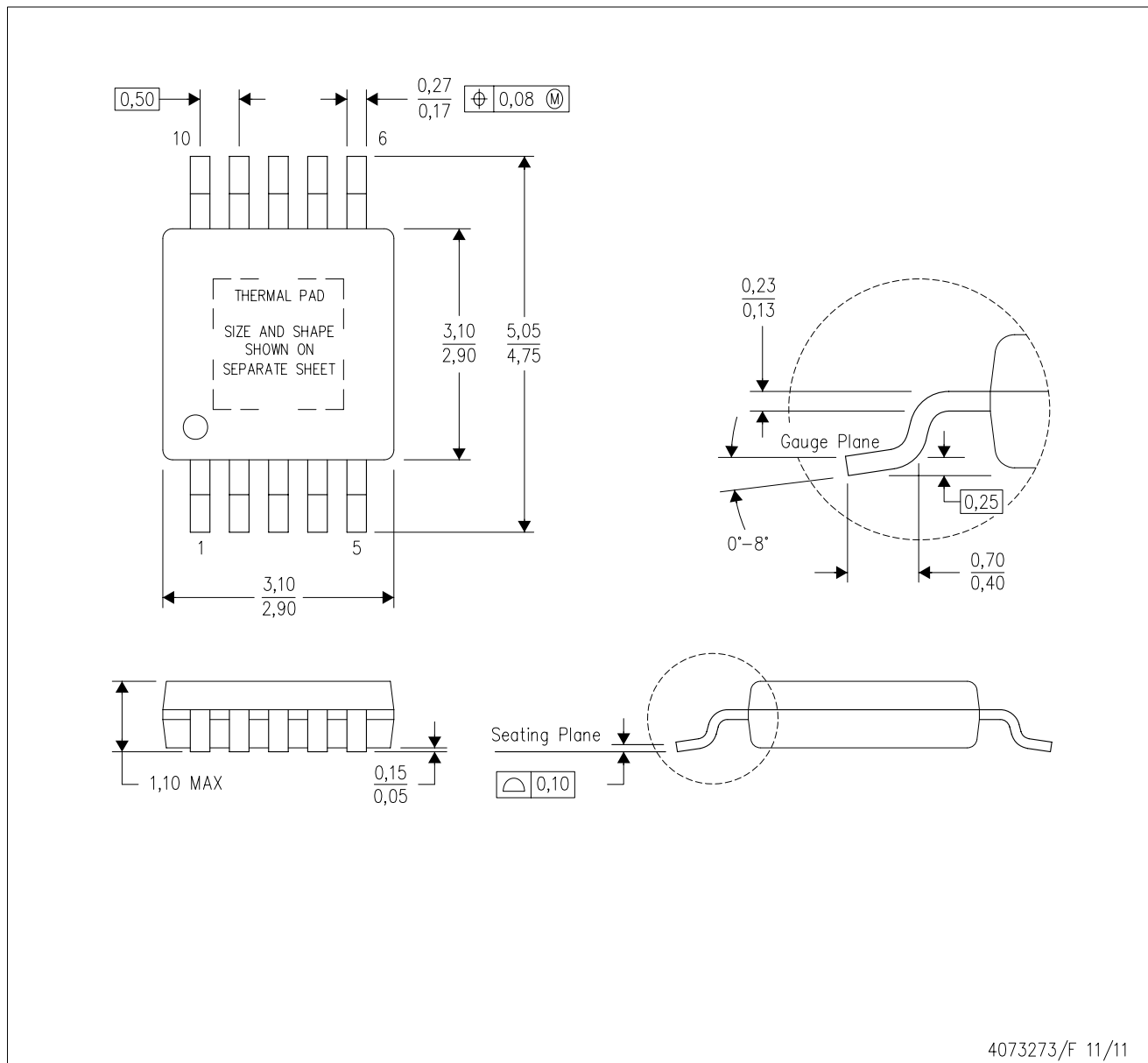


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54160QDGQRQ1	MSOP-PowerPAD	DGQ	10	2500	370.0	355.0	55.0
TPS54160QDRCRQ1	VSON	DRC	10	3000	370.0	355.0	55.0

DGQ (S-PDSO-G10)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-187 variation BA-T.

PowerPAD is a trademark of Texas Instruments.

DGQ (S-PDSO-G10)

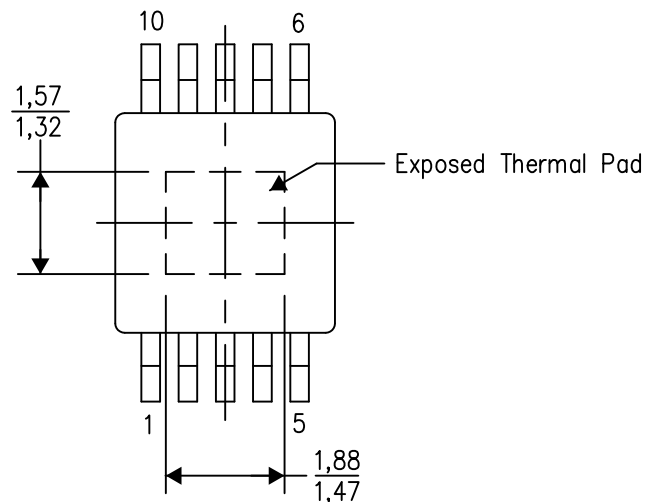
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

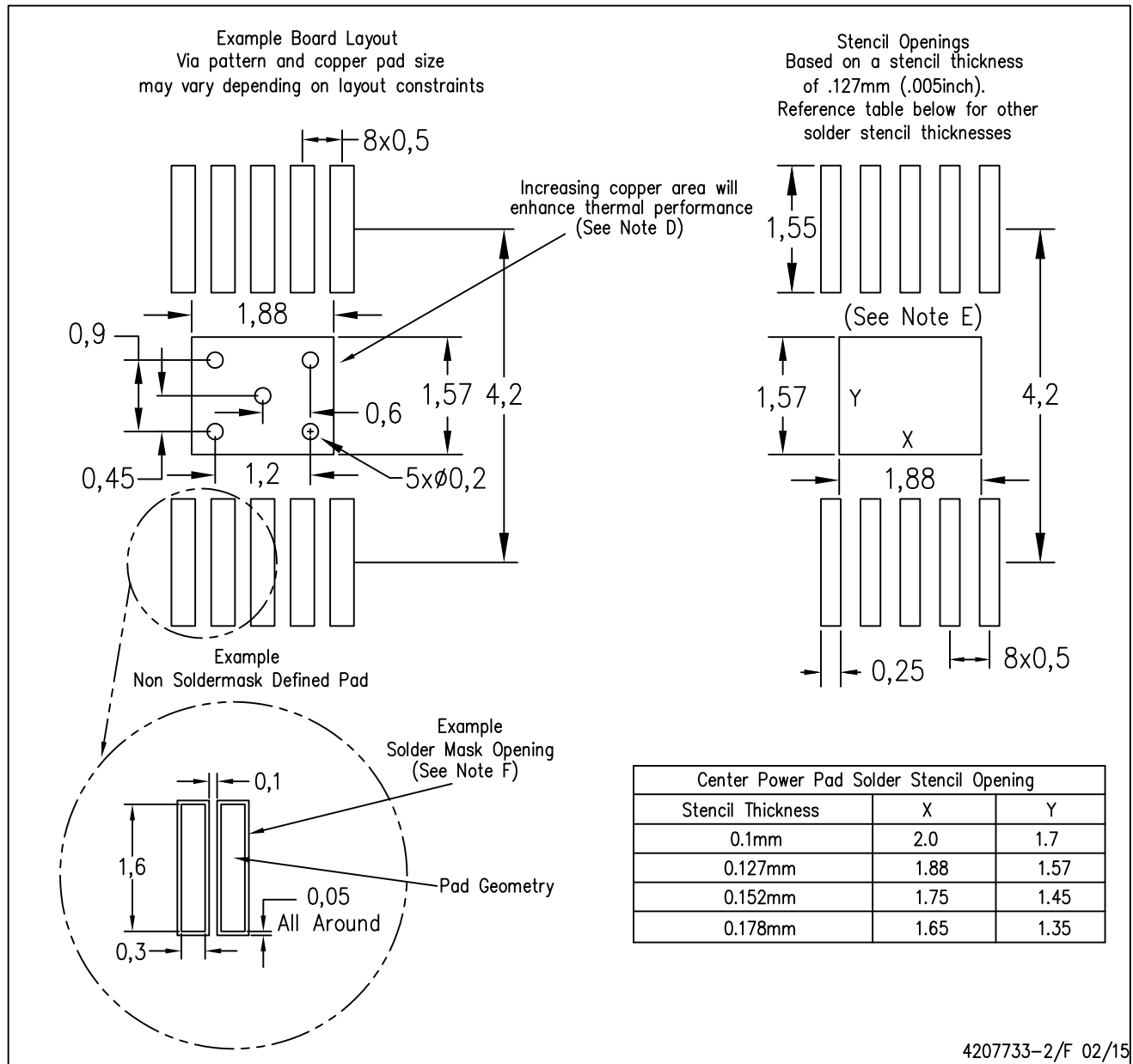
4206324-2/H 12/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGQ (S-PDSO-G10)

PowerPAD™ PLASTIC SMALL OUTLINE

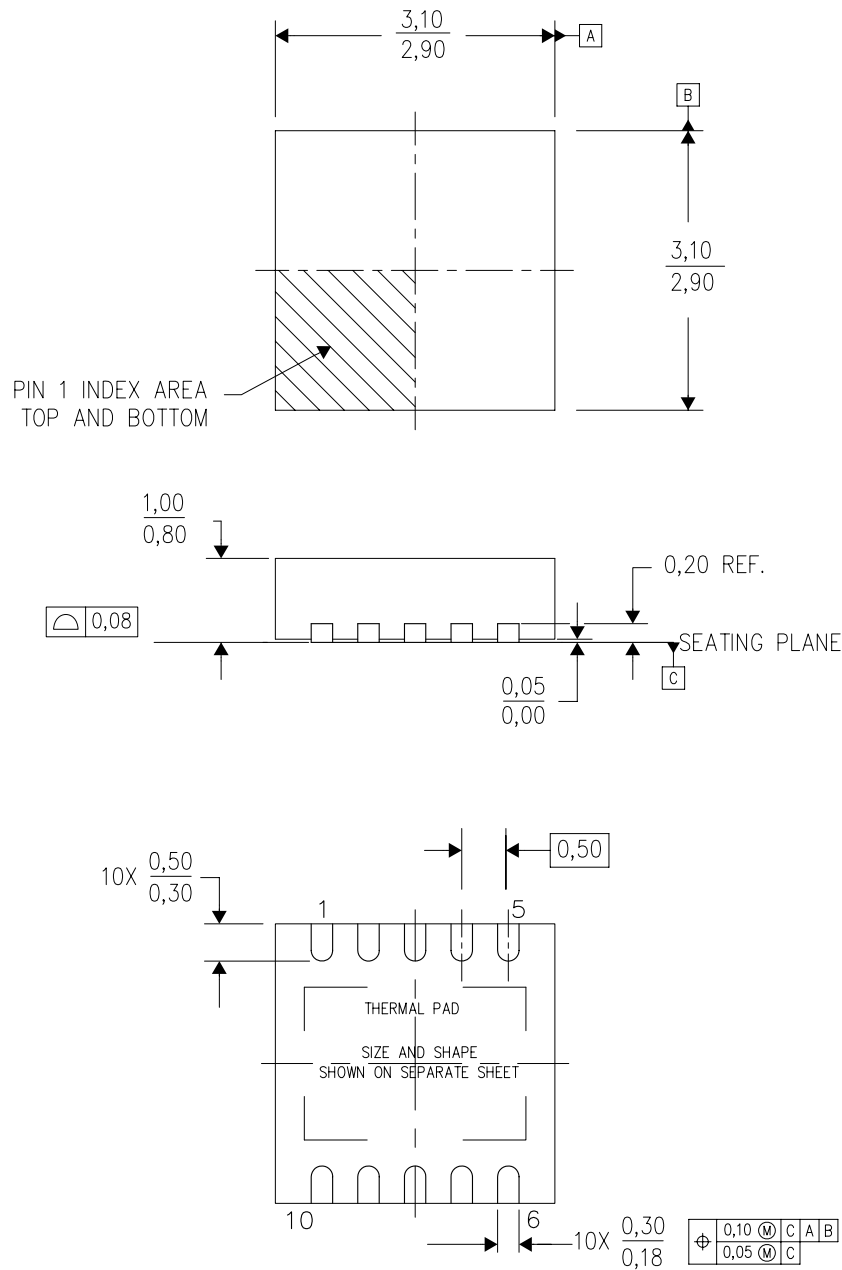


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



4204102-3/L 09/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Small Outline No-Lead (SON) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

DRC (S-PVSON-N10)

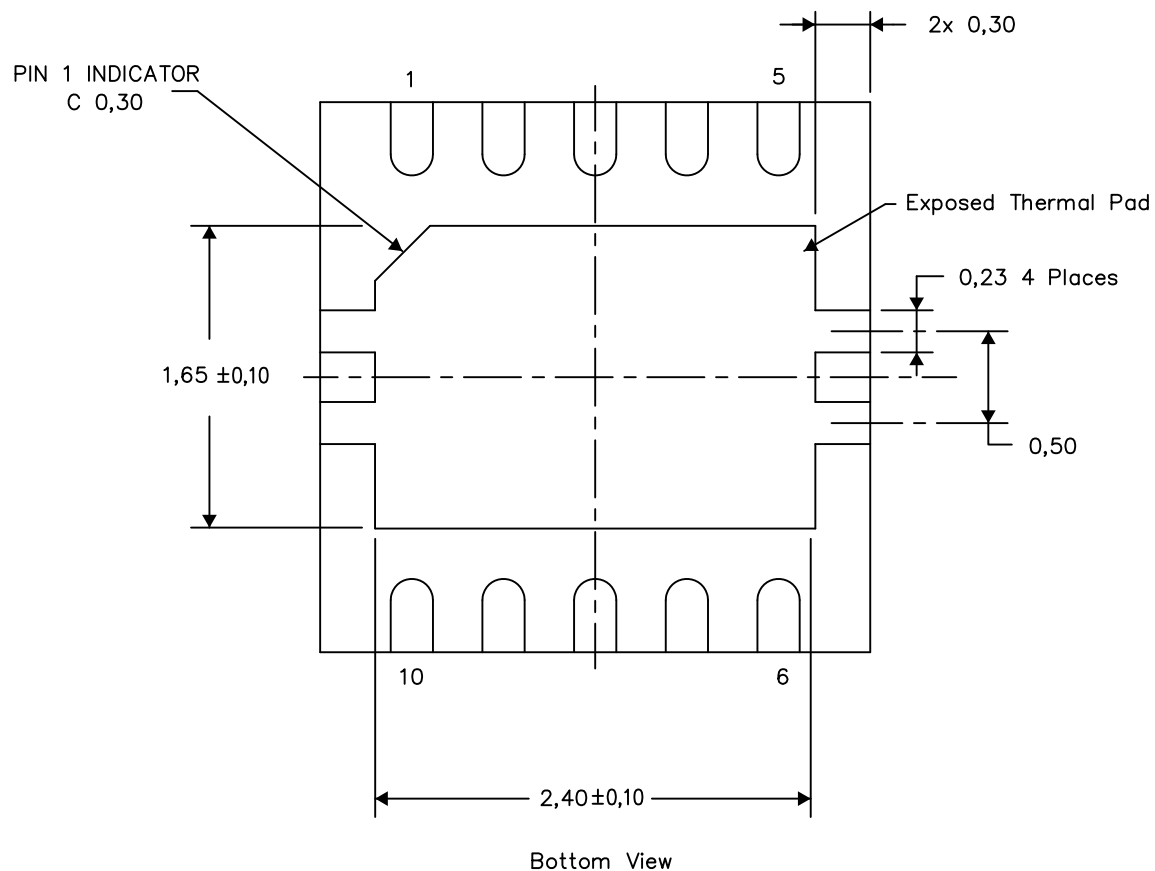
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



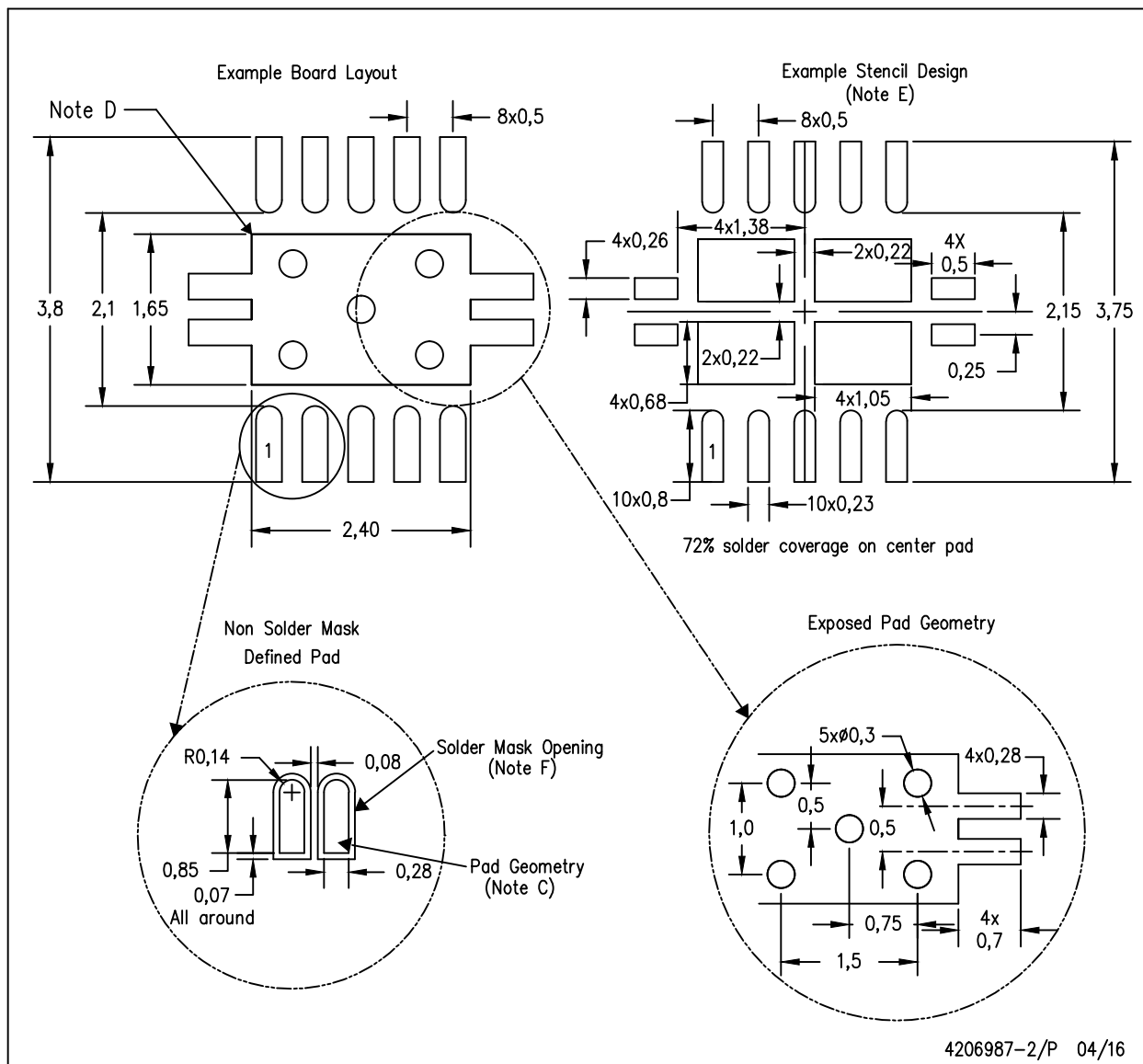
Exposed Thermal Pad Dimensions

4206565-3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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