

## 8k, 16k bit EEPROMs for direct connection to serial ports

### **BR9080AF-W / BR9080ARFV-W / BR9080ARFVM-W / BR9016AF-W / BR9016ARFV-W / BR9016ARFVM-W**

The BR9080A and BR9016A series are serial EEPROMs that can be connected directly to a serial port and can be erased and written electrically. Writing and reading is performed in word units, using four types of operation commands. Communication occurs through  $\overline{CS}$ ,  $\overline{SK}$ , DI, and DO pins.  $\overline{WC}$  pin control is used to initiate a write disabled state, enabling these EEPROMs to be used as one-time ROMs. During writing, operation is checked via the internal status check.

#### ●Applications

Movie, camera, cordless telephones, car stereos, VCRs, TVs, DIP switches, and other battery-powered equipment requiring low voltage and low current

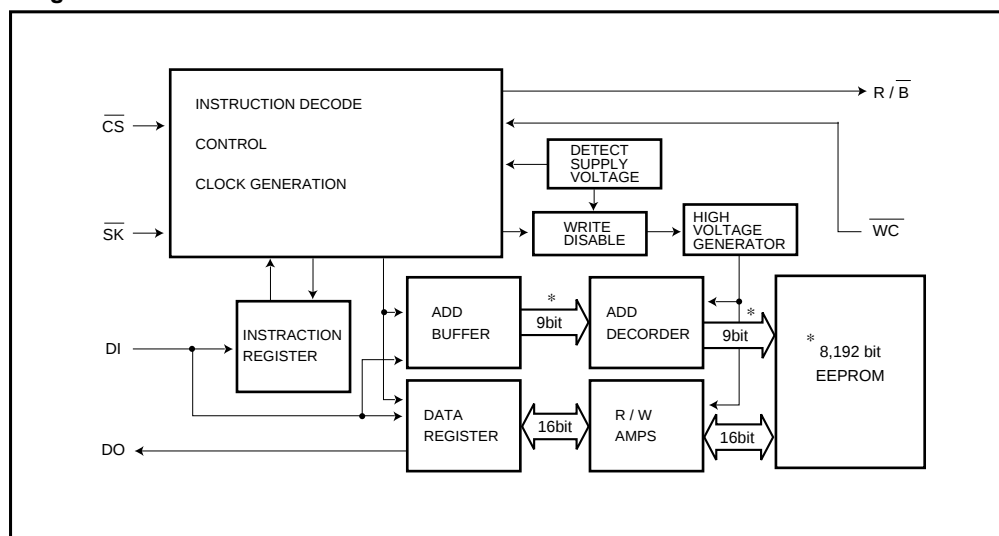
#### ●Features

- 1) BR9080AF-W / ARFV-W / ARFVM-W (8k bit) : 512 words  $\times$  16 bits  
BR9016AF-W / ARFV-W / ARFVM-W (16k bit) : 1024 words  $\times$  16bits
- 2) Single power supply operation
- 3) Serial data input and output
- 4) Automatic erase-before-write
- 5) Low current consumption  
Active (5V) : 5mA (max.)  
Standby (5V) : 3 $\mu$ A (max.)
- 6) Noise filter built into  $\overline{SK}$  pin
- 7) Write protection when  $V_{CC}$  is low  
Inhibition on inadvertant write with the  $\overline{WC}$  pin.
- 8) SOP8 / SSOP-B8 / MSOP8
- 9) High reliability CMOS process
- 10) 100,000 ERASE / WRITE cycles
- 11) 10 years Data Retention

# Memory ICs

## BR9080AF-W / BR9080ARFV-W / BR9080ARFVM-W / BR9016AF-W / BR9016ARFV-W / BR9016ARFVM-W

### ●Block diagram



\* BR9016A is 10bit, 16,384bit  
BR9080A is 9bit, 8,192bit

### ●Pin descriptions

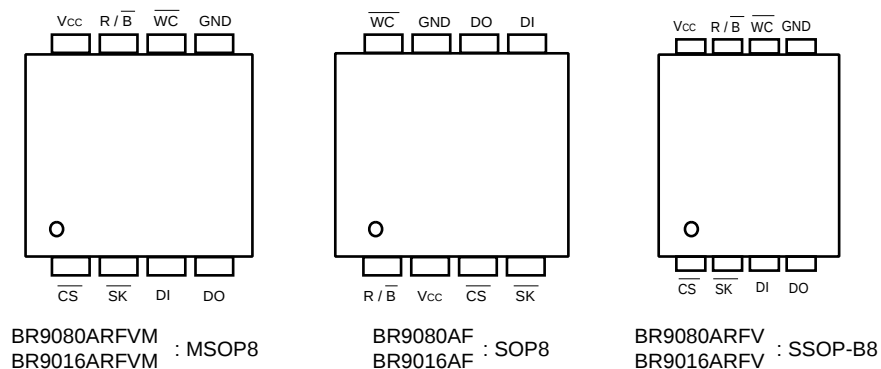


Fig.1

| Pin No.     |     | Pin name         | Function                            |
|-------------|-----|------------------|-------------------------------------|
| MSOP / SSOP | SOP |                  |                                     |
| 1           | 3   | $\overline{CS}$  | Chip Select Control                 |
| 2           | 4   | $\overline{SK}$  | Serial Data Clock Input             |
| 3           | 5   | $DI$             | Op code, address, Serial Data Input |
| 4           | 6   | $DO$             | Serial Data Output                  |
| 5           | 7   | $GND$            | Ground 0V                           |
| 6           | 8   | $\overline{WC}$  | Write Control Input                 |
| 7           | 1   | $R/\overline{B}$ | READY / $\overline{BUSY}$ Output    |
| 8           | 2   | $V_{CC}$         | Power supply                        |

BR9080AF-W / BR9080ARFV-W / BR9080ARFVM-W /  
Memory ICs      BR9016AF-W / BR9016ARFV-W / BR9016ARFVM-W

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●**Absolute maximum ratings** (Ta=25°C)

| Parameter             | Symbol           | Limits                    |                   | Unit |
|-----------------------|------------------|---------------------------|-------------------|------|
| Supply voltage        | V <sub>CC</sub>  | -0.3~+7.0                 |                   | V    |
| Power dissipation     | P <sub>d</sub>   | SOP8                      | 450 <sup>*1</sup> | mW   |
|                       |                  | SSOP-B8                   | 300 <sup>*2</sup> |      |
|                       |                  | MSOP8                     | 310 <sup>*3</sup> |      |
| Storage temperature   | T <sub>stg</sub> | -65~+125                  |                   | °C   |
| Operation temperature | T <sub>opr</sub> | -40~+85                   |                   | °C   |
| Input voltage         | —                | -0.3~V <sub>CC</sub> +0.3 |                   | V    |

\*1 Reduced by 4.5mW for each increase in Ta of 1°C over 25°C.

\*2 Reduced by 3.0mW for each increase in Ta of 1°C over 25°C.

\*3 Reduced by 3.1mW for each increase in Ta of 1°C over 25°C.

●**Recommended operating conditions** (Ta=25°C)

| Parameter            |       | Symbol          | Min. | Typ. | Max.            | Unit |
|----------------------|-------|-----------------|------|------|-----------------|------|
| Power supply voltage | WRITE | V <sub>CC</sub> | 2.7  | —    | 5.5             | V    |
|                      | READ  |                 | 2.7  | —    | 5.5             | V    |
| Input voltage        |       | V <sub>IN</sub> | 0    | —    | V <sub>CC</sub> | V    |

# BR9080AF-W / BR9080ARFV-W / BR9080ARFVM-W / Memory ICs BR9016AF-W / BR9016ARFV-W / BR9016ARFVM-W

## ●Electrical characteristics

BR9080AF-W / ARFV-W / ARFVM-W, BR9016AF-W / ARFV-W / ARFVM-W : 5V

(Unless otherwise noted, Ta=−40–85°C, Vcc=2.7V–5.5V)

| Parameter                        | Symbol           | Min.                 | Typ. | Max.                | Unit | Conditions                                                                                                                         |
|----------------------------------|------------------|----------------------|------|---------------------|------|------------------------------------------------------------------------------------------------------------------------------------|
| Input low level voltage 1        | V <sub>IL1</sub> | –                    | –    | 0.3×V <sub>CC</sub> | V    | DI pin                                                                                                                             |
| Input high level voltage 1       | V <sub>IH1</sub> | 0.7×V <sub>CC</sub>  | –    | –                   | V    | DI pin                                                                                                                             |
| Input low level voltage 2        | V <sub>IL2</sub> | –                    | –    | 0.2×V <sub>CC</sub> | V    | $\overline{\text{CS}}$ , $\overline{\text{SK}}$ , $\overline{\text{WC}}$ pin                                                       |
| Input high level voltage 2       | V <sub>IH2</sub> | 0.8×V <sub>CC</sub>  | –    | –                   | V    | $\overline{\text{CS}}$ , $\overline{\text{SK}}$ , $\overline{\text{WC}}$ pin                                                       |
| Output low level voltage         | V <sub>OL</sub>  | 0                    | –    | 0.4                 | V    | I <sub>OL</sub> =2.1mA                                                                                                             |
| Output high level voltage        | V <sub>OH</sub>  | V <sub>CC</sub> –0.4 | –    | V <sub>CC</sub>     | V    | I <sub>OH</sub> =–0.4mA                                                                                                            |
| Input leak current               | I <sub>LI</sub>  | –1                   | –    | 1                   | μA   | V <sub>IN</sub> =0V–V <sub>CC</sub>                                                                                                |
| Output leak current              | I <sub>LO</sub>  | –1                   | –    | 1                   | μA   | V <sub>OUT</sub> =0V–V <sub>CC</sub> , $\overline{\text{CS}}$ =V <sub>CC</sub>                                                     |
| Operating current                | I <sub>CC1</sub> | –                    | –    | 5                   | mA   | f <sub>SK</sub> =2MHz tE / W=10ms (WRITE)                                                                                          |
|                                  | I <sub>CC2</sub> | –                    | –    | 3                   | mA   | f <sub>SK</sub> =2MHz (READ)                                                                                                       |
| Standby current                  | I <sub>SB</sub>  | –                    | –    | 3                   | μA   | $\overline{\text{CS}}$ / $\overline{\text{SK}}$ / DI / $\overline{\text{WC}}$ =V <sub>CC</sub> DO, R / $\overline{\text{B}}$ =OPEN |
| $\overline{\text{SK}}$ frequency | f <sub>SK</sub>  | –                    | –    | 2                   | MHz  | –                                                                                                                                  |

BR9080AF-W / ARFV-W / ARFVM-W, BR9016AF-W / ARFV-W / ARFVM-W : 3V

(Unless otherwise noted, Ta=−40–85°C, Vcc=2.7V–3.3V)

| Parameter                        | Symbol           | Min.                 | Typ. | Max.                | Unit | Conditions                                                                                                                         |
|----------------------------------|------------------|----------------------|------|---------------------|------|------------------------------------------------------------------------------------------------------------------------------------|
| Input low level voltage 1        | V <sub>IL1</sub> | –                    | –    | 0.3×V <sub>CC</sub> | V    | DI pin                                                                                                                             |
| Input high level voltage 1       | V <sub>IH1</sub> | 0.7×V <sub>CC</sub>  | –    | –                   | V    | DI pin                                                                                                                             |
| Input low level voltage 2        | V <sub>IL2</sub> | –                    | –    | 0.2×V <sub>CC</sub> | V    | $\overline{\text{CS}}$ , $\overline{\text{SK}}$ , $\overline{\text{WC}}$ pin                                                       |
| Input high level voltage 2       | V <sub>IH2</sub> | 0.8×V <sub>CC</sub>  | –    | –                   | V    | $\overline{\text{CS}}$ , $\overline{\text{SK}}$ , $\overline{\text{WC}}$ pin                                                       |
| Output low level voltage         | V <sub>OL</sub>  | 0                    | –    | 0.4                 | V    | I <sub>OL</sub> =100μA                                                                                                             |
| Output high level voltage        | V <sub>OH</sub>  | V <sub>CC</sub> –0.4 | –    | V <sub>CC</sub>     | V    | I <sub>OH</sub> =–100μA                                                                                                            |
| Input leak current               | I <sub>LI</sub>  | –1                   | –    | 1                   | μA   | V <sub>IN</sub> =0V–V <sub>CC</sub>                                                                                                |
| Output leak current              | I <sub>LO</sub>  | –1                   | –    | 1                   | μA   | V <sub>OUT</sub> =0V–V <sub>CC</sub> , $\overline{\text{CS}}$ =V <sub>CC</sub>                                                     |
| Operating current                | I <sub>CC1</sub> | –                    | –    | 3                   | mA   | f <sub>SK</sub> =2MHz tE / W=10ms (WRITE)                                                                                          |
|                                  | I <sub>CC2</sub> | –                    | –    | 0.75                | mA   | f <sub>SK</sub> =2MHz (READ)                                                                                                       |
| Standby current                  | I <sub>SB</sub>  | –                    | –    | 2                   | μA   | $\overline{\text{CS}}$ / $\overline{\text{SK}}$ / DI / $\overline{\text{WC}}$ =V <sub>CC</sub> DO, R / $\overline{\text{B}}$ =OPEN |
| $\overline{\text{SK}}$ frequency | f <sub>SK</sub>  | –                    | –    | 2                   | MHz  | –                                                                                                                                  |

© Not designed for radiation resistance

# BR9080AF-W / BR9080ARFV-W / BR9080ARFVM-W / Memory ICs BR9016AF-W / BR9016ARFV-W / BR9016ARFVM-W

## ●Operating timing characteristics

BR9080AF-W / ARFV-W / ARFVM-W, BR9016AF-W / ARFV-W / ARFVM-W

(Unless otherwise noted,  $T_a = -40 \sim 85^\circ\text{C}$ ,  $V_{CC} = 2.7\text{V} \sim 5.5\text{V}$ )

| Parameter                                              | Symbol           | Min. | Typ. | Max. | Unit |
|--------------------------------------------------------|------------------|------|------|------|------|
| $\overline{\text{CS}}$ setup time                      | $t_{\text{CSS}}$ | 100  | –    | –    | ns   |
| $\overline{\text{CS}}$ hold time                       | $t_{\text{CSH}}$ | 100  | –    | –    | ns   |
| Data setup time                                        | $t_{\text{DIS}}$ | 100  | –    | –    | ns   |
| Data hold time                                         | $t_{\text{DIH}}$ | 100  | –    | –    | ns   |
| DO rise delay time                                     | $t_{\text{PD1}}$ | –    | –    | 150  | ns   |
| DO fall delay time                                     | $t_{\text{PD0}}$ | –    | –    | 150  | ns   |
| Self-timing programming cycle                          | $t_{\text{E/W}}$ | –    | –    | 10   | ms   |
| $\overline{\text{CS}}$ minimum high level time         | $t_{\text{CS}}$  | 250  | –    | –    | ns   |
| READY / BUSY display valid time                        | $t_{\text{SV}}$  | –    | –    | 150  | ns   |
| Time when DO goes HIGH-Z (via $\overline{\text{CS}}$ ) | $t_{\text{OH}}$  | 0    | –    | 150  | ns   |
| Data clock high level time                             | $t_{\text{WH}}$  | 230  | –    | –    | ns   |
| Data clock low level time                              | $t_{\text{WL}}$  | 230  | –    | –    | ns   |
| Write control setup time                               | $t_{\text{WCS}}$ | 0    | –    | –    | ns   |
| Write control hold time                                | $t_{\text{WCH}}$ | 0    | –    | –    | ns   |

## ●Timing chart

Synchronous Data Input Output Timing

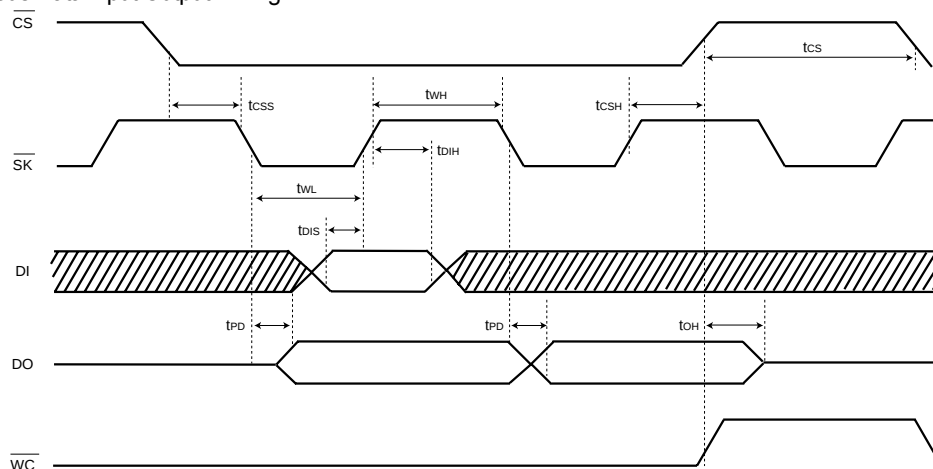


Fig.2

- Input data are clocked in to DI at the rising edge of the clock ( $\overline{\text{SK}}$ ).
- Output data will toggle on the falling edge of the  $\overline{\text{SK}}$  clock.
- The WC pin does not have any effect on the READ, EWEN and EWDS operations.

# BR9080AF-W / BR9080ARFV-W / BR9080ARFVM-W / Memory ICs BR9016AF-W / BR9016ARFV-W / BR9016ARFVM-W

## ●Circuit operation

### (1) Command mode

#### BR9080A

| Instruction         | Start Bit | Op Code | Address                 | Data            |
|---------------------|-----------|---------|-------------------------|-----------------|
| Read (READ)         | 1010      | 100 A0  | A1 A2 A3 A4 A5 A6 A7 A8 |                 |
| Write (WRITE)       | 1010      | 010 A0  | A1 A2 A3 A4 A5 A6 A7 A8 | D0 D1 – D14 D15 |
| Write enable (WEN)  | 1010      | 0011    | * * * * * * * *         |                 |
| Write disable (WDS) | 1010      | 0000    | * * * * * * * *         |                 |

\* : Means either V<sub>IH</sub> or V<sub>IL</sub>  
Address and data are transferred from LSB.

#### BR9016A

| Instruction         | Start Bit | Op Code  | Address                 | Data            |
|---------------------|-----------|----------|-------------------------|-----------------|
| Read (READ)         | 1010      | 10 A0 A1 | A2 A3 A4 A5 A6 A7 A8 A9 |                 |
| Write (WRITE)       | 1010      | 01 A0 A1 | A2 A3 A4 A5 A6 A7 A8 A9 | D0 D1 – D14 D15 |
| Write enable (WEN)  | 1010      | 0011     | * * * * * * * *         |                 |
| Write disable (WDS) | 1010      | 0000     | * * * * * * * *         |                 |

\* : Means either V<sub>IH</sub> or V<sub>IL</sub>  
Address and data are transferred from LSB.

### (2) Writing enabled / disabled

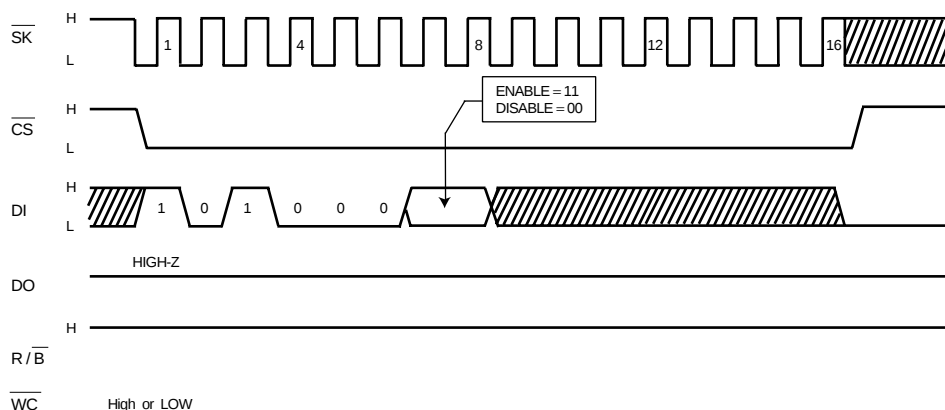


Fig.3

1) When  $\overline{CS}$  is "HIGH" during power up, BR9080AF-W / ARFV-W / ARFVM-W, BR9016AF-W / ARFV-W / ARFVM-W comes up in the write disabled (WDS) state. In order to be programmable, it must receive a write enable (WEN) instruction.

The device remains programmable until a disable (WDS) instruction is entered, or until it is powered down.

2) It is unnecessary to add the clock after 16th clock.

# BR9080AF-W / BR9080ARFV-W / BR9080ARFVM-W / Memory ICs BR9016AF-W / BR9016ARFV-W / BR9016ARFVM-W

## (3) Read cycle

BR9080AF-W / ARFV-W / ARFVM-W

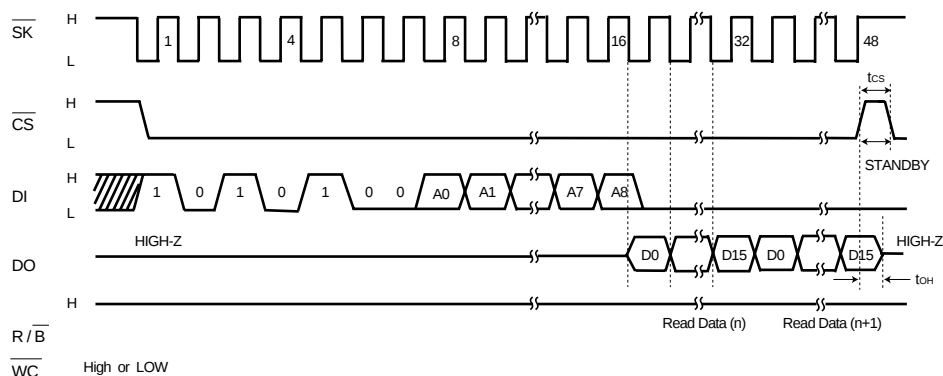


Fig.4 BR9080AF-W / ARFV-W / ARFVM-W

BR9016 AF-W / ARFV-W / ARFVM-W

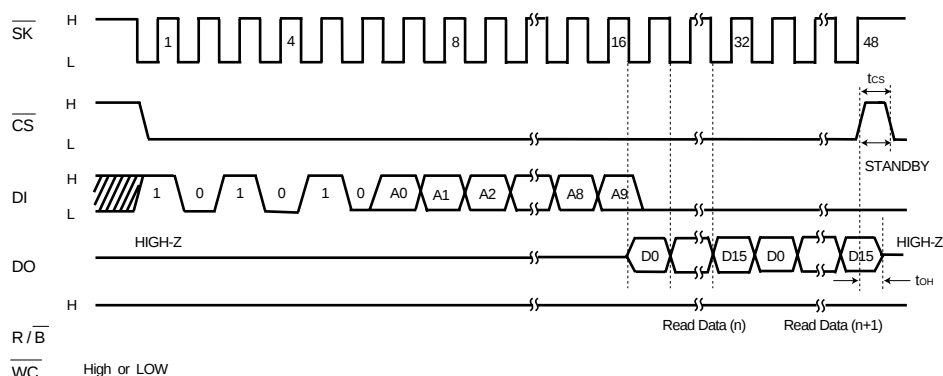


Fig.5 BR9016AF-W / ARFV-W / ARFVM-W

- 1) After the fall of the 16th clock pulse, 16-bit data is output from the DO pin in synchronization with the falling edge of the SK signal.  
(DO output changes at a time lag of  $t_{PD0}$ ,  $t_{PD1}$  because of internal circuit delay following the falling edge of the SK signal. During the  $t_{PD0}$  and  $t_{PD1}$  timing, the  $t_{PD}$  time should be assured before data is read, to avoid the previous data being lost. See the synchronized data input / output timing chart in Fig.2.)
- 2) The data stored in the next address is clocked out of the device on the falling edge of 32nd clock. The data stored in the upper address every 16 clocks is output sequentially by the continual SK input. Also the read operation is reset by CS High.

**BR9080AF-W / BR9080ARFV-W / BR9080ARFVM-W /  
Memory ICs      BR9016AF-W / BR9016ARFV-W / BR9016ARFVM-W**

**(4) Write cycle**

**BR9080AF-W / ARFV-W / ARFVM-W**

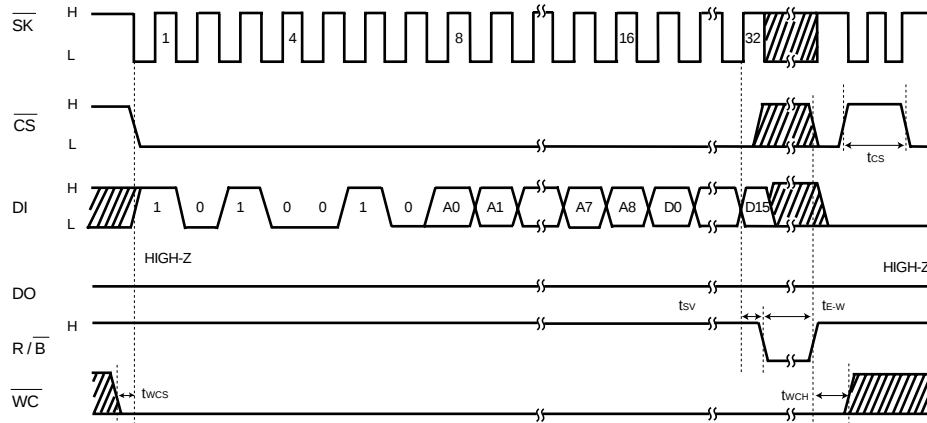


Fig.6 BR9080AF-W / ARFV-W / ARFVM-W

**BR9016 AF-W / ARFV-W / ARFVM-W**

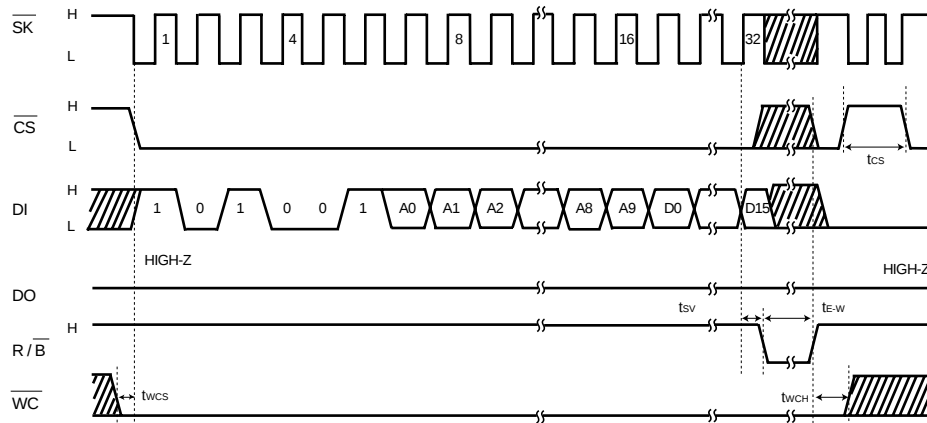


Fig.7 BR9016AF-W / ARFV-W / ARFVM-W

- 1) At the rising edge of 32nd clock,  $\overline{R/B}$  pin will be come out "LOW" after the specified time delay ( $t_{SV}$ ).
- 2) From above edge  $\overline{R/B}$  will indicate the ready / busy status of the chip: "LOW" indicated programming is all in progress: "HIGH" indicates the write cycle is complete and this part is ready for another instruction.
- 3) During the input of Write command,  $\overline{CS}$  must be "LOW". However, once the write operation started,  $\overline{CS}$  could be either "HIGH" or "LOW".
- 4) If  $\overline{WC}$  becomes "HIGH" during Write Cycle, the write operation is halted. In this case, the address data in writing is no guaranteed. It is necessary to rewrite it.

**BR9080AF-W / BR9080ARFV-W / BR9080ARFVM-W /  
Memory ICs      BR9016AF-W / BR9016ARFV-W / BR9016ARFVM-W**

(5)  $\overline{\text{READY}} / \overline{\text{BUSY}}$  display

( $\text{R} / \overline{\text{B}}$  pin and DO pin: BR9080AF-W / ARFV-W / ARFVM-W, BR9016AF-W / ARFV-W / ARFVM-W)

- 1) This display outputs the internal status signal; the  $\text{R} / \overline{\text{B}}$  pin outputs the HIGH or LOW status at all times. The display can also be output from the DO pin. Following completion of the writing command, if  $\overline{\text{CS}}$  falls while  $\overline{\text{SK}}$  is LOW, either HIGH or LOW is output. (The display can also be output without using the  $\text{R} / \overline{\text{B}}$  pin, leaving it open.)
- 2) When writing data to a memory cell, the  $\overline{\text{READY}} / \overline{\text{BUSY}}$  display is output from the rise of the 32nd clock pulse of the  $\overline{\text{SK}}$  signal after tSV, from the  $\text{R} / \overline{\text{B}}$  pin.

$\text{R} / \overline{\text{B}}$  display = LOW: writing in progress

(The internal timer circuit is activated, and after the tE / W timing has been created, the timer circuit stops automatically. Writing of data to the memory cell is done during the tE / W timing, during which time other commands cannot be received.)

$\text{R} / \overline{\text{B}}$  display = HIGH: command standby state

(Writing of data to the memory cell has been completed and the next command can be received.)

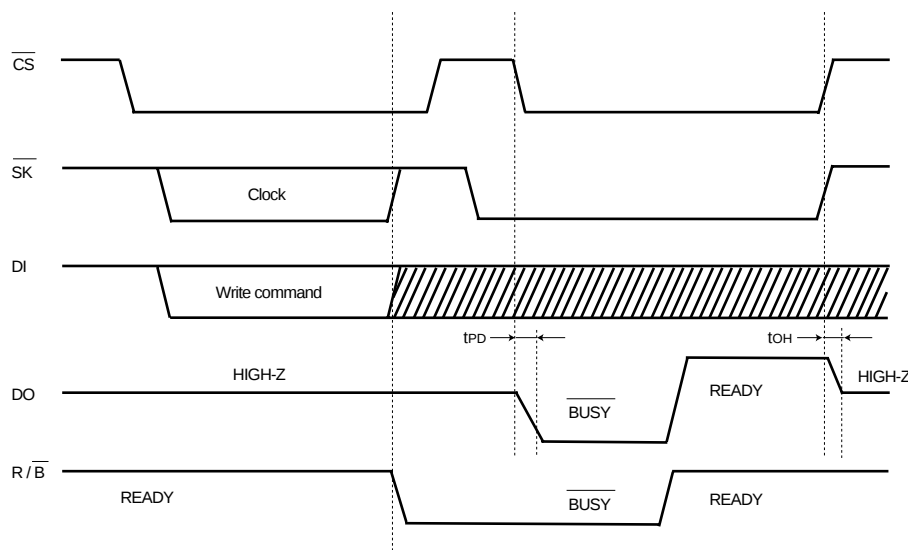


Fig.8  $\text{R} / \overline{\text{B}}$  Status Output timing chart

- 1) DO will output  $\text{R} / \overline{\text{B}}$  status after  $\overline{\text{CS}}$  is held low during  $\overline{\text{SK}}=\text{L}$ , until  $\overline{\text{CS}}$  is held high.

Note : The document may be strategic technical data subject to COCOM regulations.

●Operation notes

(1) Turning the power supply on and off

1) When the power supply is turned on and off,  $\overline{CS}$  should be set to HIGH ( $=V_{CC}$ ).

2) When  $\overline{CS}$  is LOW, the command input reception state (active) is entered. If the power supply is turned on in this state, erroneous operations and erroneous writing can occur because of noise and other factors. To avoid this, make sure  $\overline{CS}$  is set to HIGH ( $=V_{CC}$ ) before turning on the power supply.

(Good example) Here, the  $\overline{CS}$  pin is pulled up to  $V_{CC}$ .

When turning off the power supply, wait at least 10msec before turning it on again. Failing to observe this condition can result in the internal circuit failing to be reset when the power supply is turned on.

(Bad example)  $\overline{CS}$  is LOW when the power supply is turned on or off.

In this case, because  $\overline{CS}$  remains LOW, the EEPROM may perform erroneous operations or write erroneous data because of noise or other factors.

\* Please be aware that the case shown in this example can also occur if  $\overline{CS}$  input is HIGH-Z.

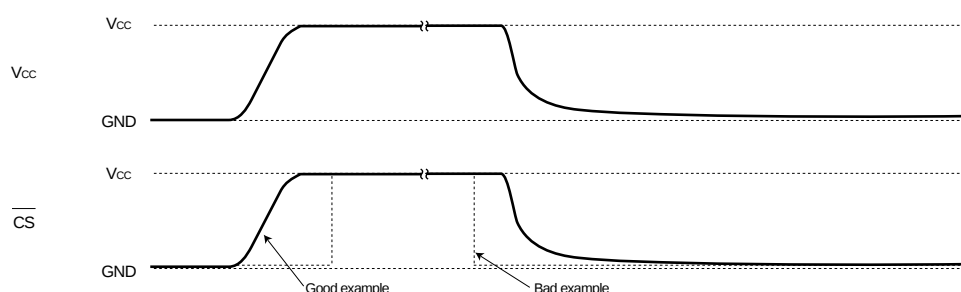


Fig.9

(2) Noise countermeasures

1)  $\overline{SK}$  noise

If noise occurs at the rise of the  $\overline{SK}$  clock input, the clock is assumed to be excessive, and this can cause malfunction because the bits are out of alignment.

2)  $\overline{WC}$  noise

During a writing operation, noise at the  $\overline{WC}$  pin can be erroneously judged to be data, and this can cause writing to be forcibly interrupted.

3)  $V_{CC}$  noise

Noise and surges on the power supply line can cause malfunction. We recommend installing a bypass capacitor between the power supply and ground to eliminate this problem.

(3) Canceling modes

1) Read commands

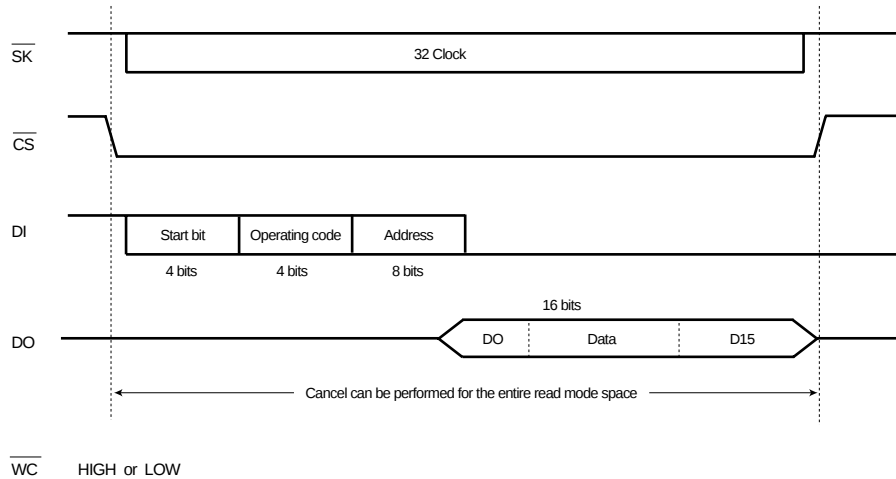


Fig.10

Cancellation method:  $\overline{\text{CS}}$  HIGH

2) Write commands

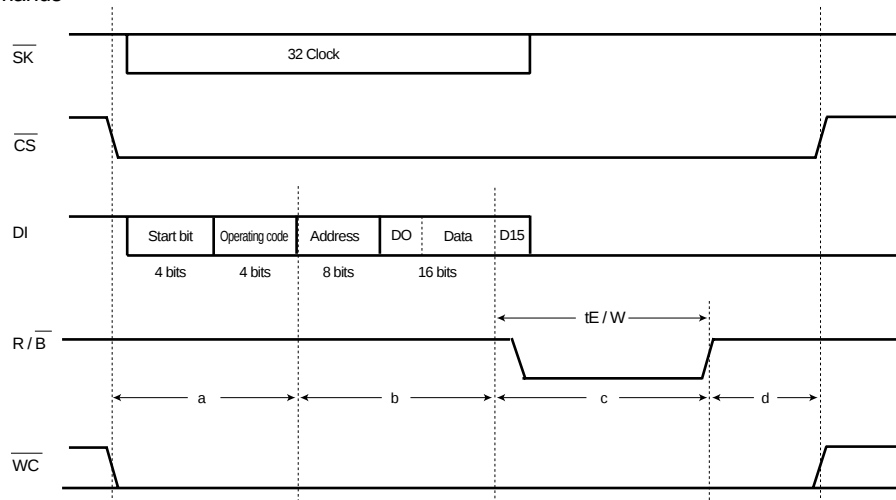


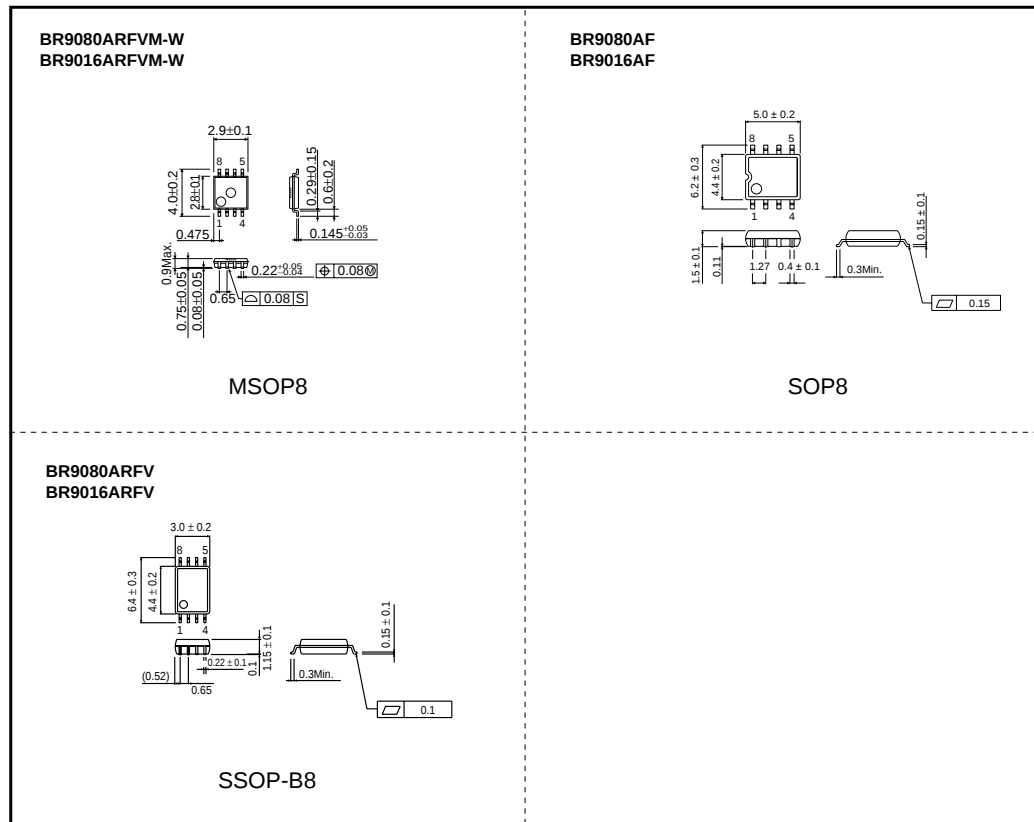
Fig.11

Canceling methods

- a : Canceled by setting  $\overline{\text{CS}}$  HIGH. The  $\overline{\text{WC}}$  pin is not involved.
- b : If the  $\overline{\text{WC}}$  pin goes HIGH for even a second, writing is forcibly interrupted. Cancellation occurs even if the  $\overline{\text{CS}}$  pin is HIGH. At this point, data has not been written to the memory, so the data in the designated address has not yet been changed.
- c : The operation is forcibly canceled by setting the  $\overline{\text{WC}}$  pin to HIGH or turning off the power supply (although we do not recommend using this method). The data in the designated address is not guaranteed and should be written once again.
- d : If  $\overline{\text{CS}}$  is set to HIGH while the  $\overline{\text{R/B}}$  signal is HIGH (following the  $t_E / W$  timing), the IC is reset internally, and waits for the next command to be input.

BR9080AF-W / BR9080ARFV-W / BR9080ARFVM-W /  
Memory ICs BR9016AF-W / BR9016ARFV-W / BR9016ARFVM-W

●External dimension (Units : mm)



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#### About Export Control Order in Japan

Products described herein are the objects of controlled goods in Annex 1 (Item 16) of Export Trade Control Order in Japan.

In case of export from Japan, please confirm if it applies to "objective" criteria or an "informed" (by MITI clause) on the basis of "catch all controls for Non-Proliferation of Weapons of Mass Destruction.