

## Automotive-grade N-channel 40 V, 1.27 mΩ typ., 120 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 DSC

Datasheet - production data

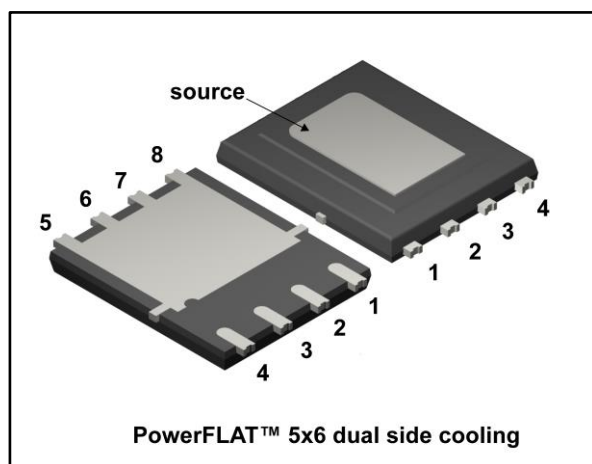


Figure 1: Internal schematic diagram

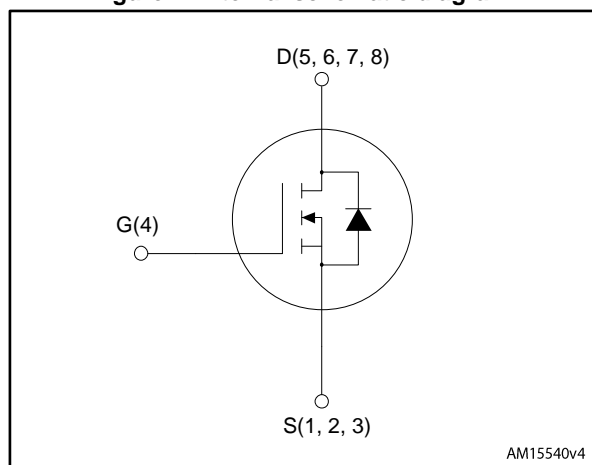


Table 1: Device summary

Order code	Marking	Package	Packaging
STLD200N4F6AG	200	PowerFLAT™ 5x6 dual side cooling	Tape and reel

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STLD200N4F6AG	40 V	1.50 mΩ	120 A

- AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package



### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)(2)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	120	A
$I_D^{(1)(2)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	120	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	480	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	158	W
$T_J$	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

**Notes:**<sup>(1)</sup>Limited by package<sup>(2)</sup>The value is rated according to  $R_{thj-c}$  bottom side.<sup>(3)</sup>Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-c}$ top side	Thermal resistance junction-case top side	2.90	$^\circ\text{C/W}$
$R_{thj-c}$ bottom side	Thermal resistance junction-case bottom side	0.95	
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

**Notes:**<sup>(1)</sup>When mounted on 1 inch<sup>2</sup> 2 Oz. Cu board,  $t \leq 10\text{ s}$ 

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AV}$	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	90	A
$E_{AS}$	Single pulse avalanche energy ( $T_J = 25\text{ }^\circ\text{C}$ , $I_C = I_{AV}$ , $V_{DD} = 16\text{ V}$ )	400	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 5: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	40			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 16\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 16\text{ V}$ , $T_J = 125\text{ }^{\circ}\text{C}$ <sup>(1)</sup>			10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2.5		3.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 75\text{ A}$		1.27	1.50	$\text{m}\Omega$
		$V_{GS} = 6.5\text{ V}$ , $I_D = 75\text{ A}$		1.48	2.00	

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 10\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	10700	-	pF
$C_{oss}$	Output capacitance		-	1530	-	pF
$C_{rss}$	Reverse transfer capacitance		-	1100	-	pF
$Q_g$	Total gate charge	$V_{DD} = 32\text{ V}$ , $I_D = 90\text{ A}$ , $V_{GS} = 0$ to $10\text{ V}$ (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	172	-	nC
$Q_{gs}$	Gate-source charge		-	56	-	nC
$Q_{gd}$	Gate-drain charge		-	48	-	nC

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$ , $I_D = 75\text{ A}$ $R_G = 30\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	150	-	ns
$t_r$	Rise time		-	440	-	ns
$t_{d(off)}$	Turn-off-delay time		-	600	-	ns
$t_f$	Fall time		-	410	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		120	A
$I_{SDM}^{(1)(2)}$	Source-drain current (pulsed)		-		480	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 90\text{ A}$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 90\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 20\text{ V}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	40		ns
$Q_{rr}$	Reverse recovery charge		-	53		nC
$I_{RRM}$	Reverse recovery current		-	2.5		A

**Notes:**

(1)Limited by package.

(2)Pulse width is limited by safe operating area.

(3)Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

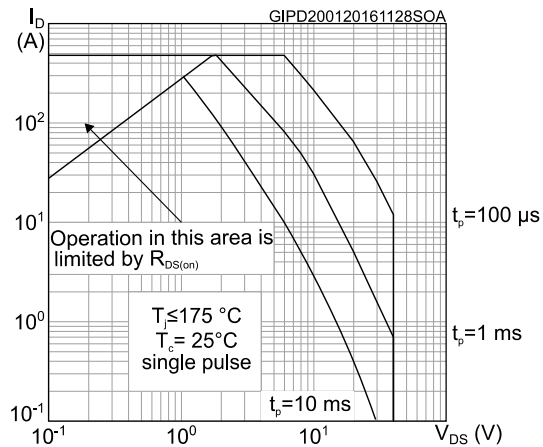


Figure 3: Thermal impedance

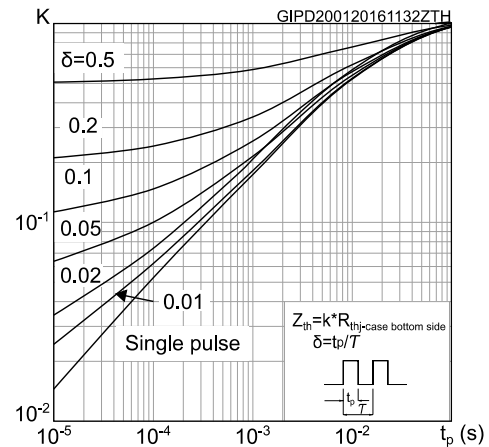


Figure 4: Output characteristics

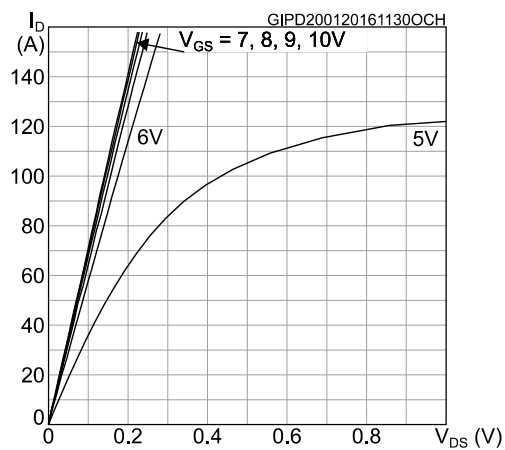


Figure 5: Transfer characteristics

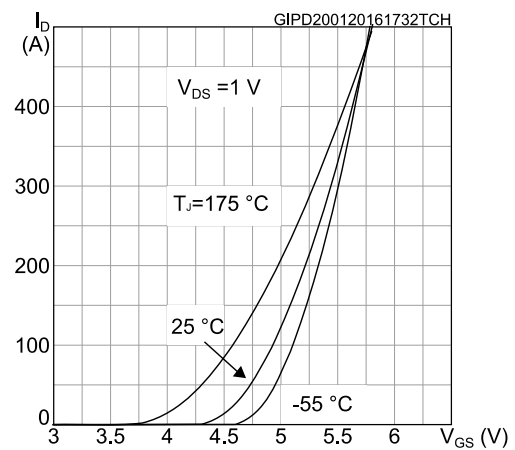


Figure 6: Gate charge vs gate-source voltage

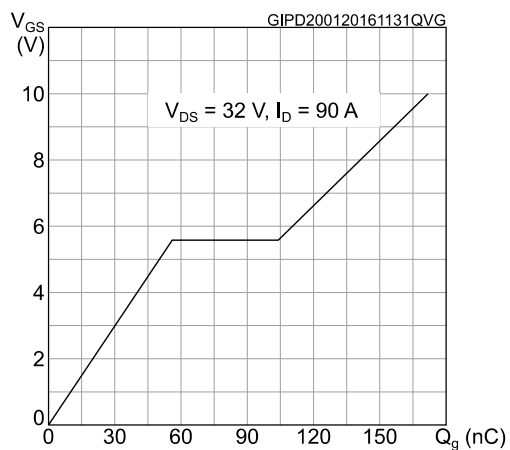


Figure 7: Static drain-source on-resistance

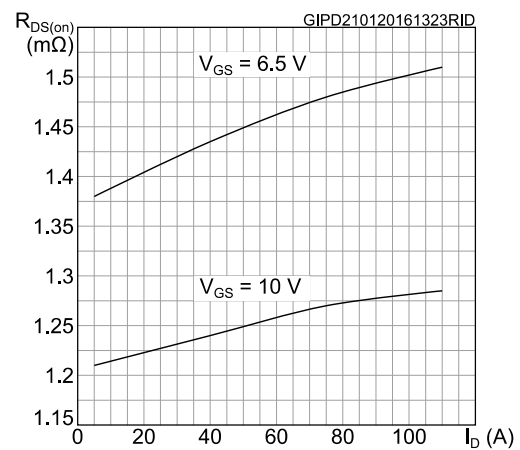


Figure 8: Capacitance variations

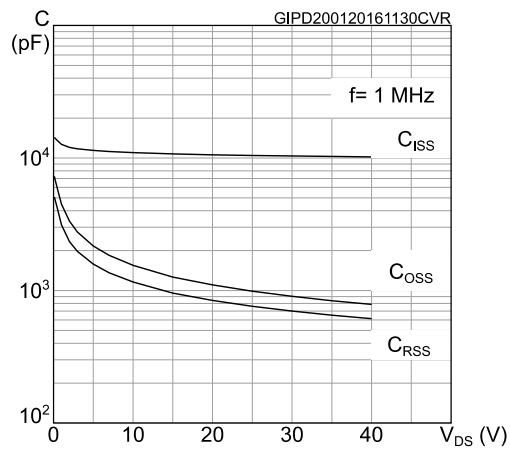


Figure 9: Normalized gate threshold voltage vs temperature

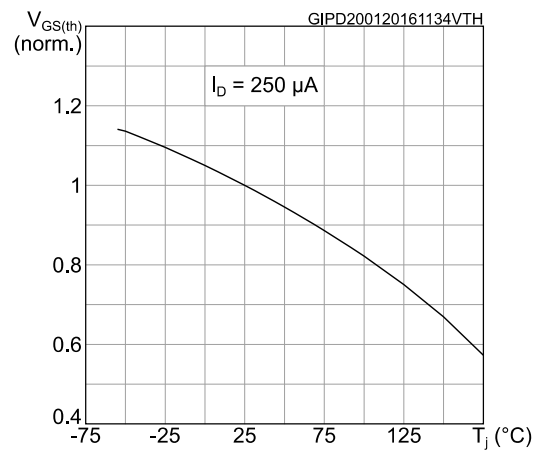


Figure 10: Normalized on-resistance vs temperature

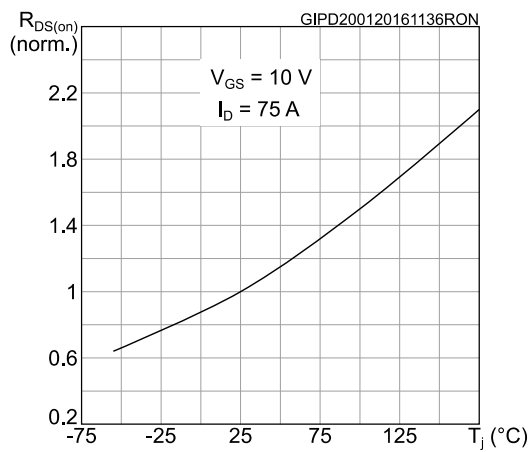
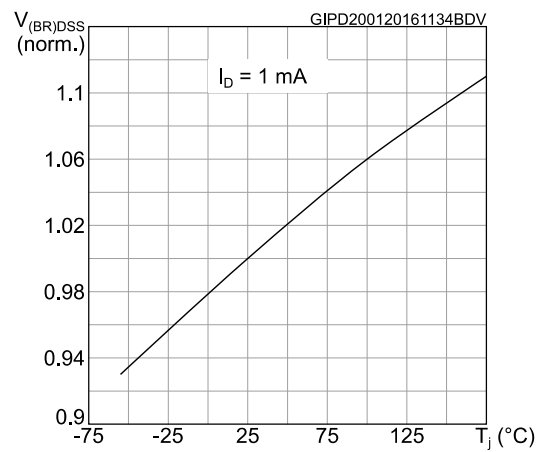
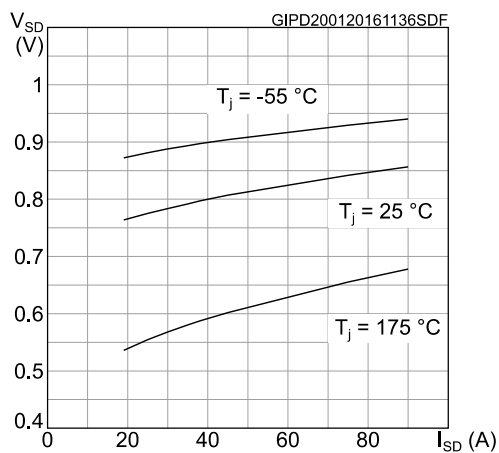
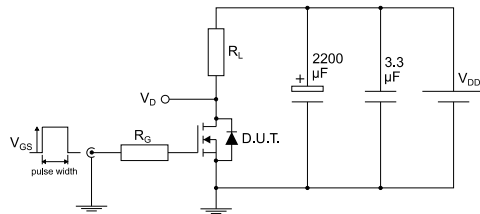
Figure 11: Normalized  $V_{(BR)DSS}$  vs temperature

Figure 12: Source-drain diode forward characteristics



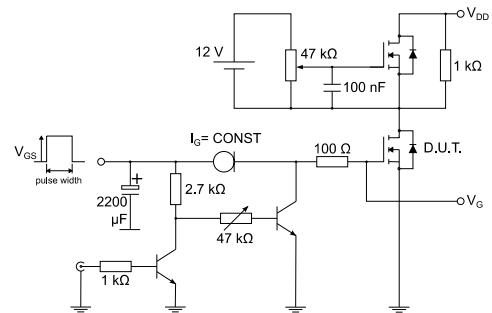
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



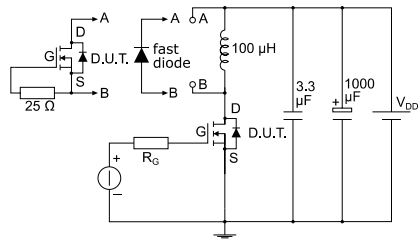
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**Figure 14: Test circuit for gate charge behavior**



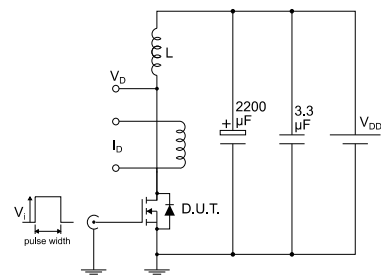
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



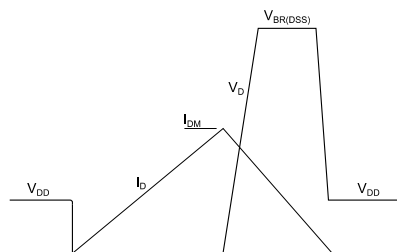
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**Figure 16: Unclamped inductive load test circuit**



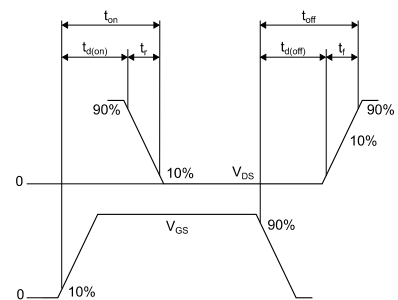
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**Figure 17: Unclamped inductive waveform**



AM01472v1

**Figure 18: Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT™ 5x6 dual side cooling package information

Figure 19: PowerFLAT™ 5x6 dual side cooling package outline

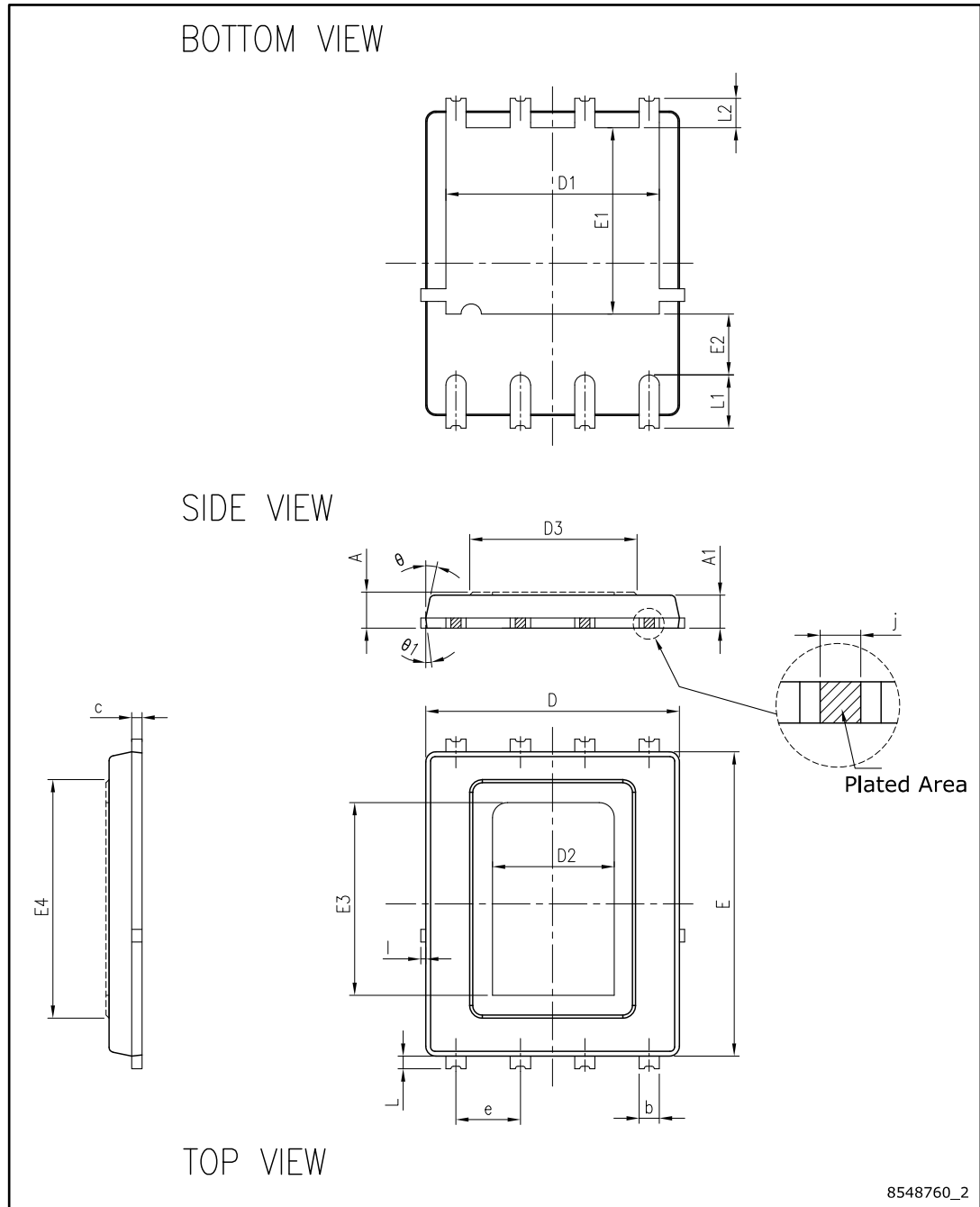
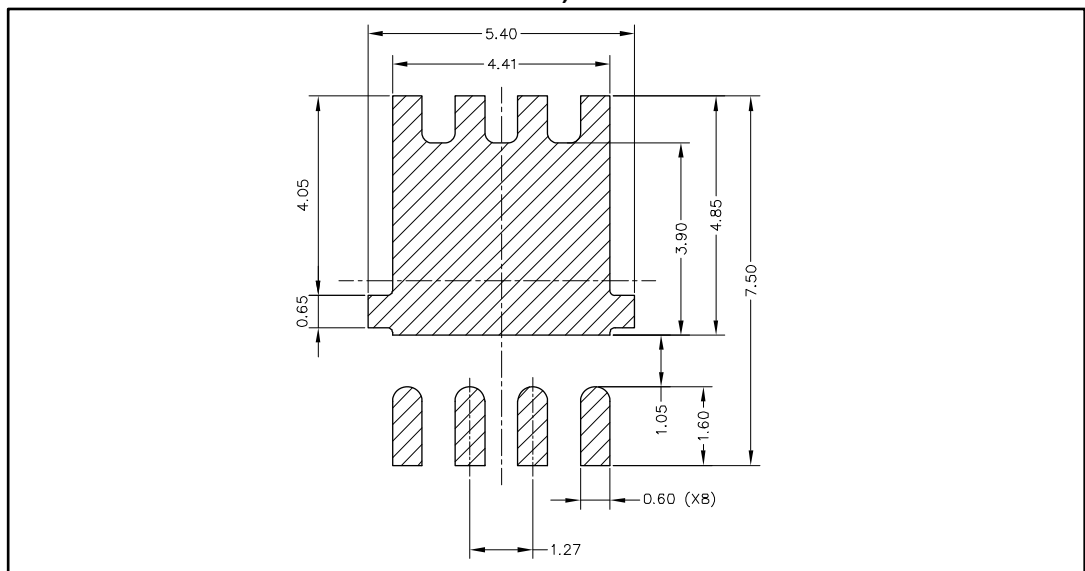


Table 9: PowerFLAT™ 5x6 dual side cooling mechanical data

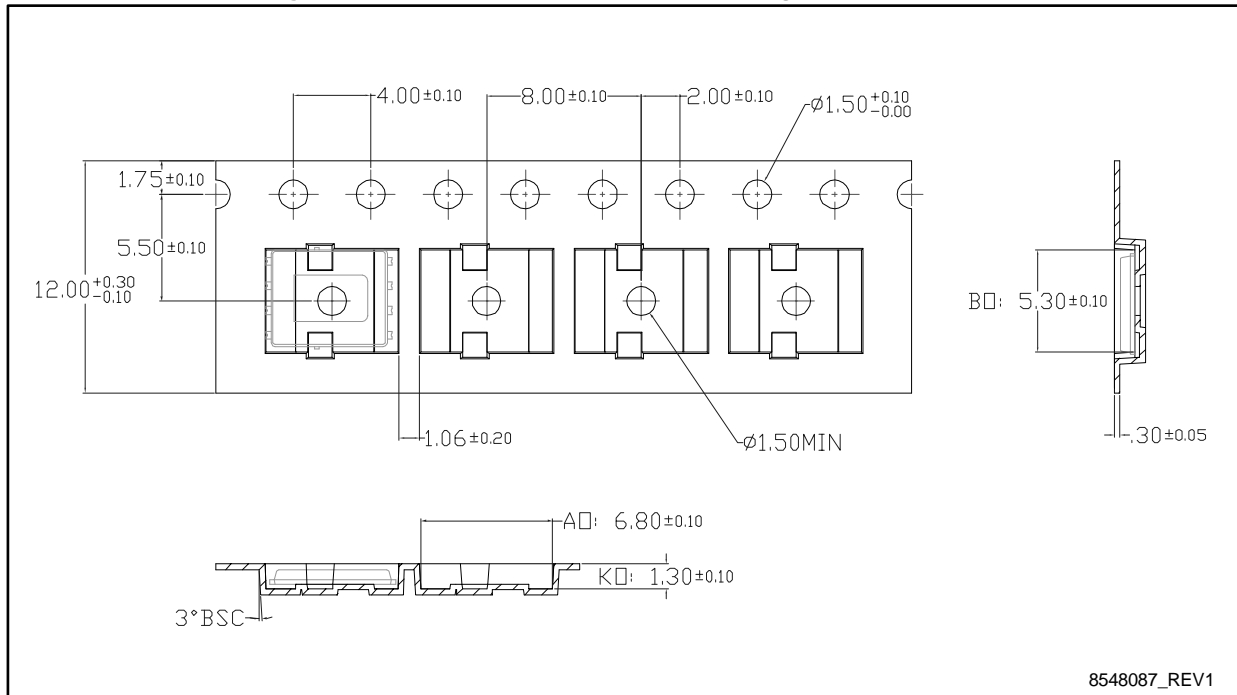
Dim.	mm		
	Min.	Typ.	Max.
A	0.66	0.71	0.76
A1	0.60		0.75
b	0.33	0.43	0.53
c	0.15	0.203	0.30
D	5.00 BSC		
D1	4.06	4.21	4.36
D2	2.40 BSC		
D3	2.80	3.30	3.80
E	6.00 BSC		
E1	3.525	3.675	3.825
E2	1.05	1.20	1.35
E3	3.80 BSC		
E4	4.20	4.70	5.20
e	1.27 BSC		
l			0.15
L	0.15	0.25	0.35
L1	0.925	1.05	1.175
L2	0.45	0.575	0.70
ϑ	12° BSC		
ϑ1	7° BSC		
j	0.20 BSC		

Figure 20: PowerFLAT™ 5x6 dual side cooling recommended footprint (dimensions are in mm)



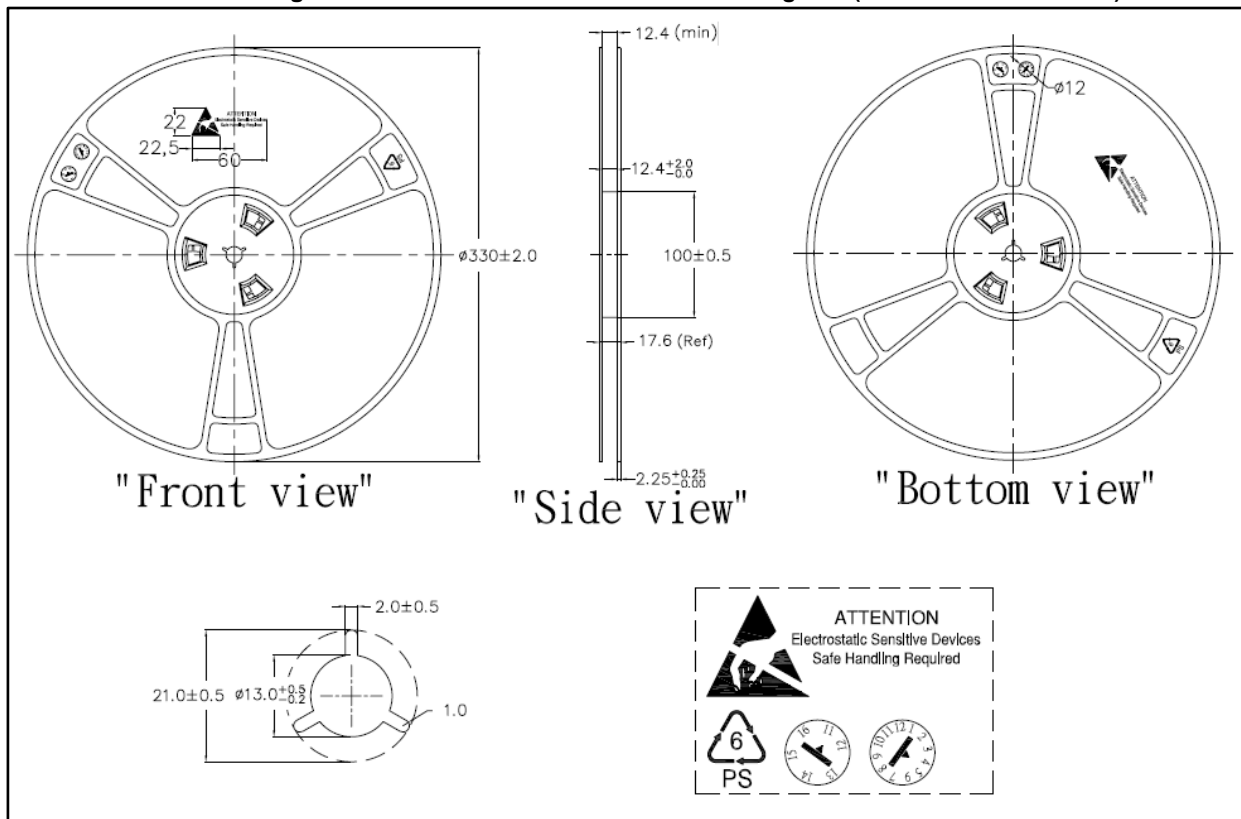
## 4.2 PowerFLAT™ 5x6 dual side cooling packing information

Figure 21: PowerFLAT™ 5x6 dual side cooling tape (dimensions are in mm)



8548087\_REV1

Figure 22: PowerFLAT™ 5x6 dual side cooling reel (dimensions are in mm)



## 5 Revision history

**Table 10: Document revision history**

Date	Revision	Changes
19-Jan-2016	1	First release
07-Feb-2017	2	Document status promoted from preliminary to production data. Updated <i>Table 3: "Thermal data"</i> and <i>Table 5: "On/off states"</i> . Minor text changes
23-Feb-2017	3	Updated features on cover page. Updated <i>Table 5: "On/off states"</i> and <i>Figure 9: "Normalized gate threshold voltage vs temperature"</i> Minor text changes
04-Apr-2017	4	Updated test conditions in <i>Table 7: "Switching times"</i> .
12-Jul-2017	5	Added <a href="#">Section 4.2: "PowerFLAT™ 5x6 dual side cooling packing information"</a> .

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