

## GENERAL DESCRIPTION

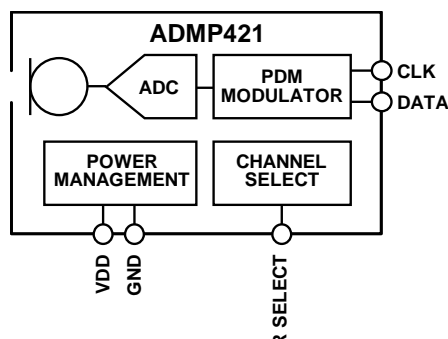
The ADMP421 is a high performance, low power, digital output bottom-ported omnidirectional MEMS microphone. The ADMP421 consists of a MEMS microphone element and an impedance converter amplifier followed by a fourth-order  $\Sigma$ - $\Delta$  modulator. The digital interface allows for the pulse density modulated (PDM) output of two microphones to be time-multiplexed on a single data line using a single clock.

The ADMP421 has a flat wideband frequency response, resulting in natural sound with high intelligibility. Low current consumption and a sleep mode enable long battery life for portable applications. A built-in particle filter provides high reliability. The ADMP421 complies with the TIA-920 *Telecommunications Telephone Terminal Equipment Transmission Requirements for Wideband Digital Wireline Telephones* standard.

The ADMP421 is available in a thin 3 × 4 × 1 mm surface-mount package. It is reflow solder compatible with no sensitivity degradation. The ADMP421 is halide free

*\*Protected by U.S. Patents 7,449,356; 7,825,484; 7,885,423; and 7,961,897. Other patents are pending.*

## FUNCTIONAL BLOCK DIAGRAM



## APPLICATIONS

- Feature Phones
- Tablet Computers
- Teleconferencing Systems
- Digital Still and Video Cameras
- Bluetooth Headsets
- Notebook PCs
- Security and Surveillance

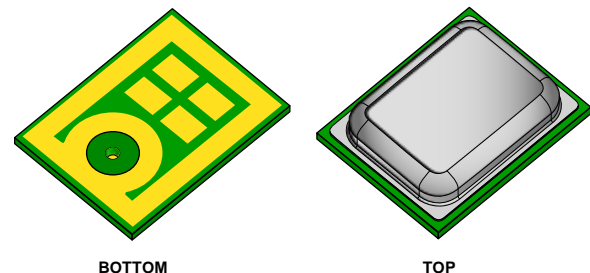
## FEATURES

- Small and Thin 3 × 4 × 1 mm Surface-Mount Package
- SNR of 61 dBA
- Sensitivity of -26 dBFS
- Flat Frequency Response from 100 Hz to 15 kHz
- Low Current Consumption: <650  $\mu$ A
- Sleep Mode for Extended Battery Life
- High PSR of 80 dBFS
- Fourth-Order  $\Sigma$ - $\Delta$  Modulator
- Digital PDM Output
- Compatible with Sn/Pb and Pb-Free Solder Processes
- RoHS/WEEE Compliant

## ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
ADMP421ACEZ-RL	-40°C to +85°C*	CE-5-1
ADMP421ACEZ-RL7	-40°C to +85°C†	CE-5-1
EVAL-ADMP421Z	—	—
EVAL-ADMP421Z-FLEX	—	—

\* – 13" Tape and Reel † – 7" Tape and Reel



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## SPECIFICATIONS

**TABLE 1. ELECTRICAL CHARACTERISTICS**

( $T_A = -40$  to  $85^\circ\text{C}$ ,  $V_{DD} = 1.8$  to  $3.3$  V,  $\text{CLK} = 2.4$  MHz,  $C_{LOAD} = 30$  pF, unless otherwise noted. All minimum and maximum specifications are guaranteed across temperature, voltage, and clock frequency specified in Table 1, unless otherwise noted. Typical specifications are not guaranteed.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
<b>PERFORMANCE</b>							
Directionality				Omni			
Sensitivity		1 kHz, 94 dB SPL	-29	-26	-23	dBFS	1
Signal-to-Noise Ratio (SNR)		20 Hz to 20 kHz, A-weighted		61		dBA	
Equivalent Input Noise (EIN)		20 Hz to 20 kHz, A-weighted		33		dBA SPL	
Dynamic Range		Derived from EIN and maximum acoustic input		87		dB	
Frequency Response		Low frequency -3 dB point		100		Hz	2
		High frequency -3 dB point		15		kHz	
Total Harmonic Distortion (THD)		105 dB SPL			3	%	
Power-Supply Rejection (PSR)		217 Hz, 100 mVp-p square wave superimposed on $V_{DD} = 1.8$ V		-80		dBV	
Maximum Acoustic Input		Peak		120		dB SPL	
<b>POWER SUPPLY</b>							
Supply Voltage ( $V_{DD}$ )			1.62		3.63	V	
Supply Current ( $I_S$ )							
$V_{DD} = 1.8$ V	Normal Mode				650	$\mu\text{A}$	
	Sleep Mode				50	$\mu\text{A}$	3
<b>DIGITAL INPUT/OUTPUT CHARACTERISTICS</b>							
Input Voltage High ( $V_{IH}$ )			$0.65 \times V_{DD}$			V	
Input Voltage Low ( $V_{IL}$ )					$0.35 \times V_{DD}$	V	
Output Voltage High ( $V_{OH}$ )		$I_{LOAD} = 0.5$ mA	$0.7 \times V_{DD}$	$V_{DD}$		V	
Output Voltage Low ( $V_{OL}$ )		$I_{LOAD} = 0.5$ mA		0	$0.3 \times V_{DD}$	V	
Latency				<30		$\mu\text{s}$	
Noise Floor		20 Hz to 20 kHz, A-weighted		-87		dBFS	

**Note 1:** Relative to the RMS level of sine wave with positive amplitude equal to 100% logical 1s density and negative amplitude equal to 0% logical 1s density.

**Note 2:** See Figure 4 and Figure 5.

**Note 3:** The microphone enters sleep mode when the clock frequency is less than 1 kHz.

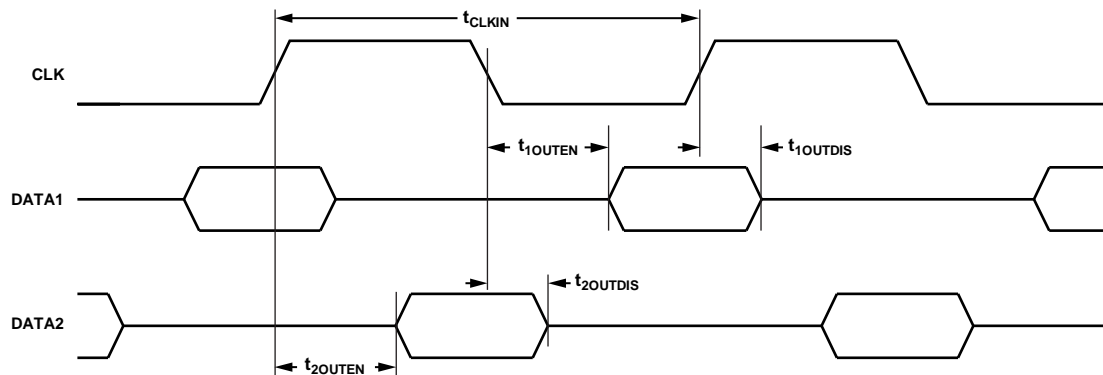
**TABLE 2. TIMING CHARACTERISTICS**

$T_A = -40$  to  $85^\circ\text{C}$ ,  $V_{DD} = 1.8$  to  $3.3$  V,  $\text{CLK} = 2.4$  MHz,  $C_{\text{LOAD}} = 30$  pF, unless otherwise noted. All minimum and maximum specifications are guaranteed. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
<b>SLEEP MODE</b>						
Wake-Up Time	Time from CLK rising ( $f_{\text{CLK}} > 1$ kHz), power on		10		ms	1
<b>INPUT</b>						
$t_{\text{CLKIN}}$	Input clock period	310		1000	ns	
Clock Frequency (CLK)		1.0	2.4	3.3	MHz	1
Clock Duty Cycle		40		60	%	
<b>OUTPUT</b>						
$T_{1\text{OUTEN}}$	DATA1 (right) driven after falling clock edge	30			ns	
$T_{1\text{OUTDIS}}$	DATA1 (right) disabled after rising clock edge			20	ns	
$T_{2\text{OUTEN}}$	DATA2 (left) driven after rising clock edge	30			ns	
$T_{2\text{OUTDIS}}$	DATA2 (left) disabled after falling clock edge			20	ns	

**Note 1:** The microphone operates at any clock frequency between 1.0 MHz and 3.3 MHz. Some specifications may not be guaranteed at frequencies other than 2.4 MHz.

## TIMING DIAGRAM


**Figure 1. Pulse Density Modulated Output Timing**

## ABSOLUTE MAXIMUM RATINGS

Stress above those listed as Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

**TABLE 3. ABSOLUTE MAXIMUM RATINGS**

PARAMETER	RATING
Supply Voltage ( $V_{DD}$ )	-0.3 V to +3.63 V
Digital Pin Input Voltage	-0.3 V to $V_{DD} + 0.3$ V or 3.63 V, whichever is less
Sound Pressure Level	160 dB
Mechanical Shock	10,000 <i>g</i>
Vibration	Per MIL-STD-883 Method 2007, Test Condition B
Temperature Range	
Biased	-40°C to +85°C
Storage	-55°C to +150°C

### ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## SOLDERING PROFILE

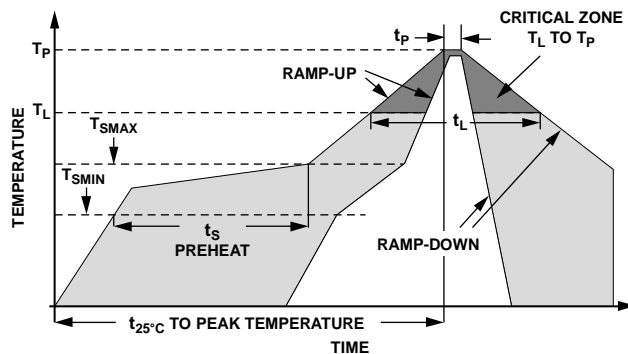


Figure 2. Recommended Soldering Profile Limits

TABLE 4. RECOMMENDED SOLDERING PROFILE

PROFILE FEATURE		Sn63/Pb37	Pb-Free
Average Ramp Rate (T <sub>L</sub> to T <sub>P</sub> )		1.25°C/sec max	1.25°C/sec max
Preheat	Minimum Temperature (T <sub>SMIN</sub> )	100°C	100°C
	Minimum Temperature (T <sub>SMIN</sub> )	150°C	200°C
	Time (T <sub>SMIN</sub> to T <sub>SMAX</sub> ), t <sub>S</sub>	60 sec to 75 sec	60 sec to 75 sec
Ramp-Up Rate (T <sub>SMAX</sub> to T <sub>L</sub> )		1.25°C/sec	1.25°C/sec
Time Maintained Above Liquidous (t <sub>L</sub> )		45 sec to 75 sec	~50 sec
Liquidous Temperature (T <sub>L</sub> )		183°C	217°C
Peak Temperature (T <sub>P</sub> )		215°C +3°C/-3°C	260°C +0°C/-5°C
Time Within +5°C of Actual Peak Temperature (t <sub>P</sub> )		20 sec to 30 sec	20 sec to 30 sec
Ramp-Down Rate		3°C/sec max	3°C/sec max
Time +25°C (t <sub>25°C</sub> ) to Peak Temperature		5 min max	5 min max

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

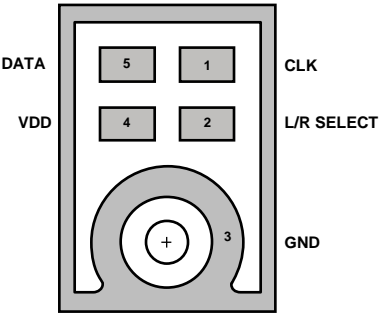


Figure 3. Pin Configuration

TABLE 5. PIN FUNCTION DESCRIPTIONS

PIN	NAME	FUNCTION
1	CLK	Clock Input to Microphone
2	L/R SELECT	Left Channel or Right Channel Select: DATA 1 (right): L/R SELECT tied to GND DATA 2 (left): L/R SELECT tied to VDD
3	GND	Ground
4	VDD	Power Supply. For best performance and to avoid potential parasitic artifacts, place a 0.1 $\mu$ F (100 nF) ceramic type X7R capacitor between Pin 4 (VDD) and ground. Place the capacitor as close to Pin 4 as possible.
5	DATA	Digital Output Signal (DATA1 or DATA2)



TYPICAL PERFORMANCE CHARACTERISTICS

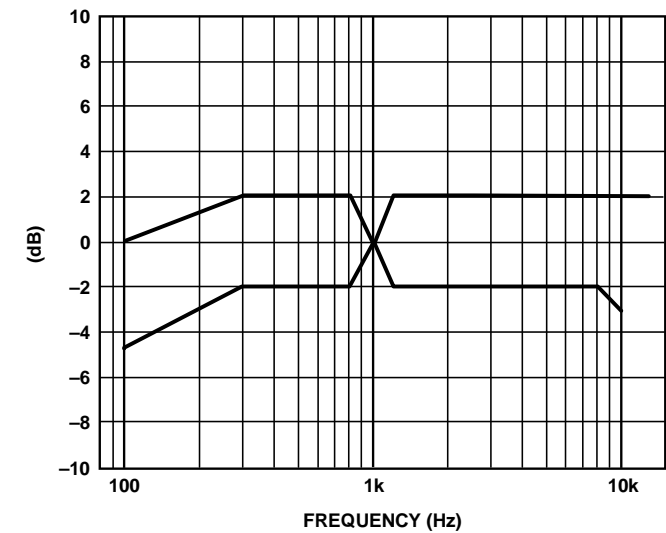


Figure 4. Frequency Response Mask

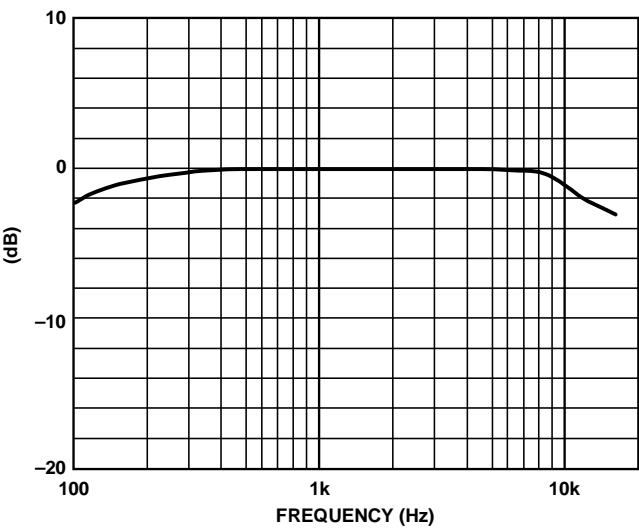


Figure 5. Typical Frequency Response (Measured)

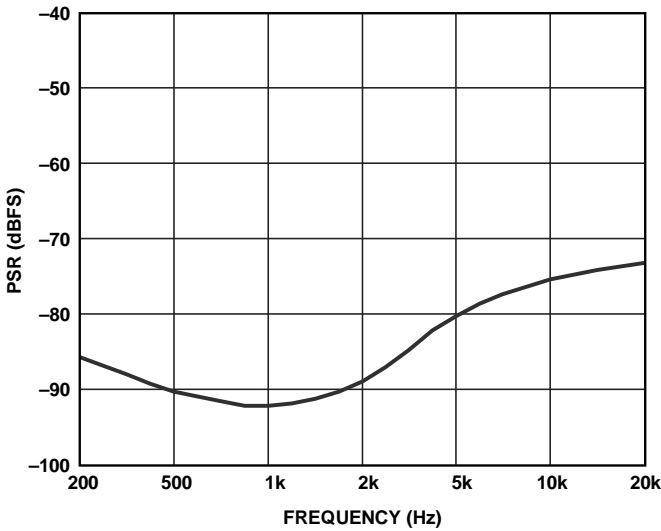


Figure 6. Power-Supply Rejection (PSR) vs. Frequency

THEORY OF OPERATION

PDM DATA FORMAT

The output from the DATA pin of the ADMP421 is in PDM format. This data is the 1-bit output of a fourth-order  $\Sigma$ - $\Delta$  modulator. The data is encoded so that the left channel is clocked on the falling edge of CLK and the right channel is clocked on the rising edge of CLK.

After driving the DATA signal high or low in the appropriate half frame of the CLK signal, the DATA driver of the microphone is tristated. In this way, two microphones—one set to the left channel and the other to the right channel—can drive a single DATA line.

Figure 1 shows a timing diagram of the PDM data format; the DATA1 and DATA2 lines shown in Figure 1 are two halves of the single physical DATA signal. Figure 7 shows a diagram of the two stereo channels sharing a common DATA line.

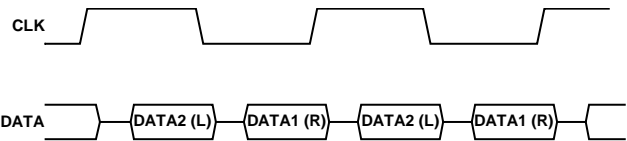


Figure 7. Stereo PDM Format

If only one microphone is connected to the DATA signal, the output is clocked on a single edge only (See Figure 8.)

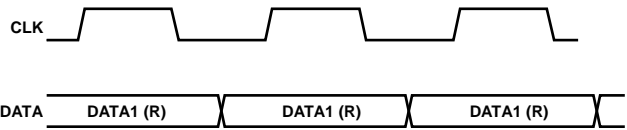


Figure 8. Mono PDM Format

For example, a left channel microphone is never clocked on the rising edge of CLK. In a single microphone application, each bit of the DATA signal is typically held for the full CLK period until the next transition of the CLK signal because the leakage of the DATA line is not sufficient to discharge the line while the driver is tristated.

The channel assignments are determined by the logic level on the L/R SELECT pin (see Table 6.)

TABLE 6. ADMP421 CHANNEL SETTING

L/R SELECT Pin Setting	Channel
Low (tie to GND)	Right (DATA1)
High (tie to VDD)	Left (DATA2)

For PDM data, the density of the pulses indicates the signal amplitude. A high density of high pulses indicates a signal near positive full scale, and a high density of low pulses indicates a signal near negative full scale. A perfect zero (DC) audio signal is indicated by an alternating pattern of high and low pulses.

The output PDM data signal has a small DC offset of approximately 5% of full scale. A high-pass filter in the codec that is connected to the digital microphone typically removes this DC signal and does not affect the performance of the microphone.

### PDM MICROPHONE SENSITIVITY

The sensitivity of a PDM output microphone is specified in units of dBFS (decibels relative to a full-scale digital output). A 0 dBFS sine wave is defined as a signal whose peak just touches the full-scale code of the digital word (see Figure 9). This measurement convention means that signals with a different crest factor may have an RMS level higher than 0dBFS. For example, a full-scale square wave has an RMS level of 3dBFS.

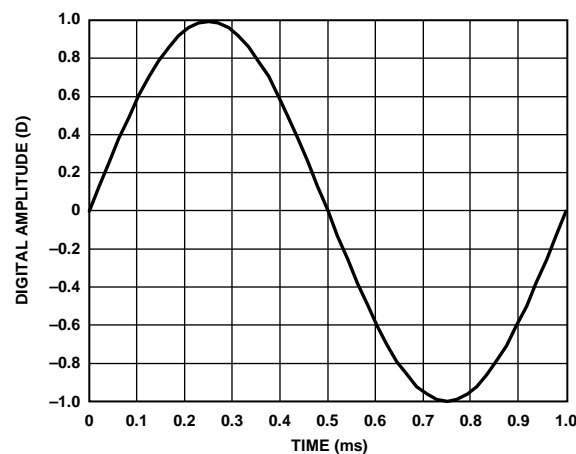


Figure 9. 1 kHz, 0 dBFS Sine Wave

The definition of a 0 dBFS signal must be understood when measuring the sensitivity of the ADMP421. An acoustic input signal of a 1 kHz sine wave at 94 dB SPL applied to the ADMP421 results in an output signal with a -26 dBFS level. This means that the output digital word peaks at -26 dB below the digital full-scale level. A common misunderstanding is that the output has an RMS level of -29 dBFS; however, this is not the case because of the definition of a 0 dBFS sine wave.

There is no commonly accepted unit of measurement to express the instantaneous level of a digital signal output from the microphone, as opposed to the RMS level of the signal. Some measurement systems express the instantaneous level of an individual sample in units of D, where 1.0 D is digital full scale (see Figure 9). In this case, a -26 dBFS sine wave has peaks at 0.05 D.

For more information about digital microphone sensitivity, see the AN-1112 Application Note, *Microphone Specifications Explained*.

## CONNECTING PDM MICROPHONES

A PDM output microphone is typically connected to a codec with a dedicated PDM input. This codec separately decodes the left and right channels and filters the high sample rate modulated data back to the audio frequency band. The codec also generates the clock for the PDM microphones or is synchronous with the source that generates the clock.

Figure 10 and Figure 11 show mono and stereo connections between the ADMP421 and a codec. The mono connection shows an ADMP421 set to output data on the right channel. To output data on the left channel, tie the L/R SELECT pin to VDD instead of GND.

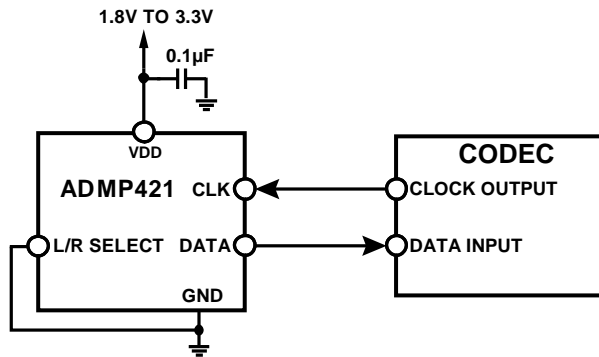


Figure 10. Mono PDM Microphone (Right Channel) Connection to Codec

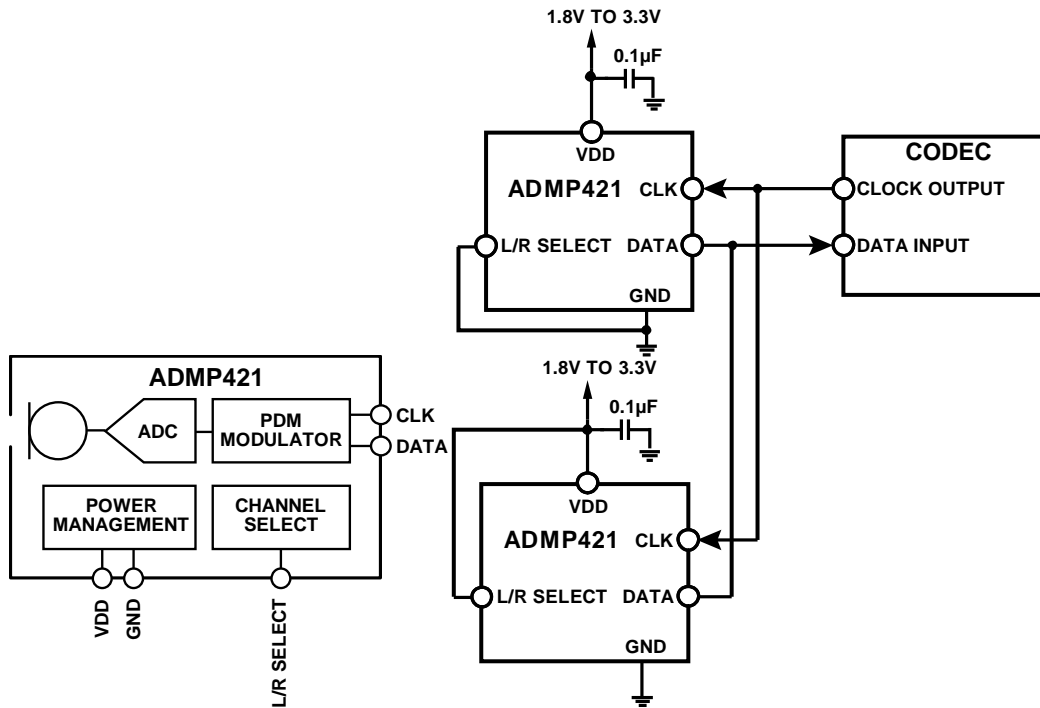


Figure 11. Stereo PDM Microphone Connection to Codec

Decouple the VDD pin of the ADMP421 to GND with a 0.1  $\mu$ F capacitor. Place this capacitor as close to  $V_{DD}$  as the printed circuit board (PCB) layout allows.

Do not use a pull-up or pull-down resistor on the PDM data signal line because the resistor can pull the signal to an incorrect state during the period that the signal line is tristated.

The DATA signal does not need to be buffered in normal use when the ADMP421 microphones are placed close to the codec on the PCB. If the ADMP421 must drive the DATA signal over a long cable (>15 cm) or other large capacitive load, a digital buffer may be needed. Use a signal buffer on the DATA line only when one microphone is in use or after the point where two microphones are connected (see Figure 12.)

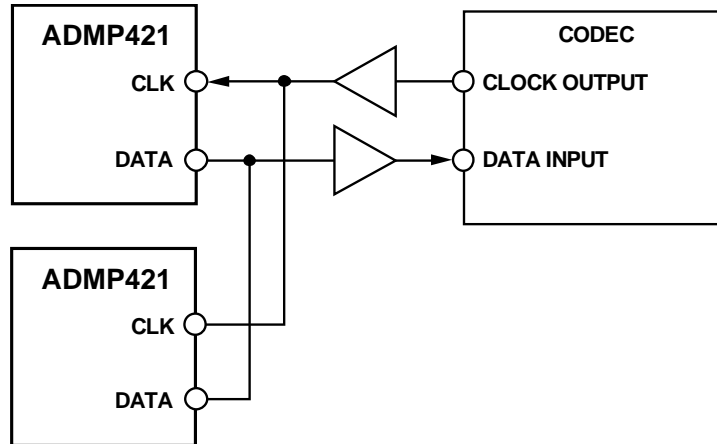


Figure 12. Buffered Connection Between Stereo ADMP421 Devices and a Codec

The DATA output of each microphone in a stereo configuration cannot be individually buffered because the two buffer outputs cannot drive a single signal line. If a buffer is used, take care to select a buffer with low propagation delay so that the timing of the data connected to the codec is not corrupted.

When long wires are used to connect the codec to the ADMP421, a 100  $\Omega$  source termination resistor can be used on the clock output of the codec instead of a buffer to minimize signal over-shoot or ringing. Depending on the drive capability of the codec clock output, a buffer may still be needed, as shown in Figure 13.

## SLEEP MODE

The microphone enters sleep mode when the clock is turned off or the clock frequency falls below 1 kHz. In sleep mode, the microphone data output is in high impedance state and the current consumption is less than 50  $\mu$ A.

## POWER SAVINGS WHEN DISABLING ONE MICROPHONE IN A MULTIMICROPHONE APPLICATION

The ADMP421 has a unique power-saving feature when used in systems where two or more microphones share the same clock and/or data lines. The microphone is designed to present high impedance on both the clock and data pins when the power supply ( $V_{DD}$ ) pin is at 0 V or floating. This disabled microphone presents no load to and consumes no power from other active microphones.

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## **SUPPORTING DOCUMENTS**

For additional information, see the following documents.

### **EVALUATION BOARD USER GUIDE**

[UG-183](#), EVAL-ADMP421Z Bottom Port Digital Output MEMS Microphone Evaluation Board

[UG-326](#), PDM Digital Output MEMS Microphone Evaluation Board

### **CIRCUIT NOTE**

[CN-0078](#), High Performance Digital MEMS Microphone Simple Interface to a SigmaDSP Audio Codec

### **APPLICATION NOTES**

[AN-1003](#), Recommendations for Mounting and Connecting the Invensense, Inc., Bottom-Ported MEMS Microphones

[AN-1068](#), Reflow Soldering of the MEMS Microphone

[AN-1112](#), Microphone Specifications Explained

[AN-1124](#), Recommendations for Sealing Invensense, Inc., Bottom-Port MEMS Microphones from Dust and Liquid Ingress

[AN-1140](#), Microphone Array Beamforming

## PCB DESIGN AND LAND PATTERN LAYOUT

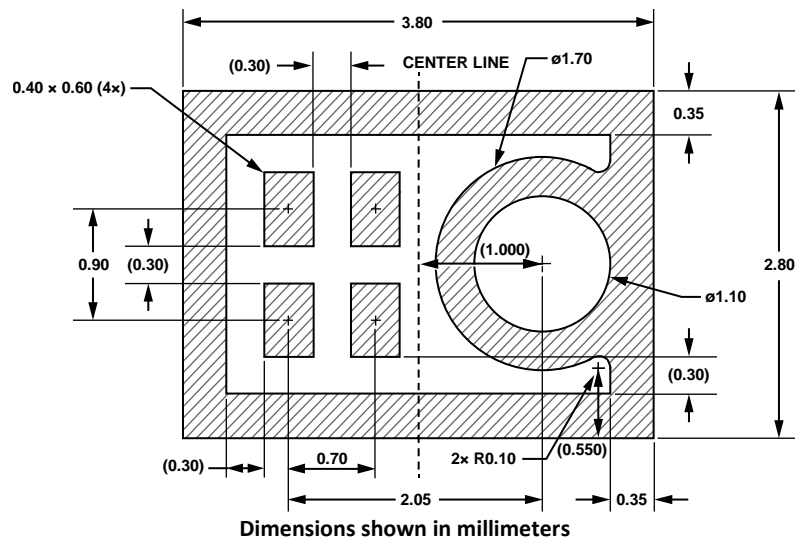
Lay out the PCB land pattern for the ADMP421 at a 1:1 ratio to the solder pads on the microphone package (see Dimensions shown in millimeters)

Figure 13.) Take care to avoid applying solder paste to the sound hole in the PCB. Dimensions shown in millimeters

Figure 14 shows a suggested solder paste stencil pattern layout.

The response of the ADMP421 is not affected by the PCB hole size, as long as the hole is not smaller than the sound port of the microphone (0.25 mm, or 0.010 inch, in diameter). A 0.5 mm to 1 mm (0.020 inch to 0.040 inch) diameter for the hole is recommended.

Align the hole in the microphone package with the hole in the PCB. The exact degree of the alignment does not affect the performance of the microphone as long as the holes are not partially or completely blocked.



**Figure 13. Suggested PCB Land Pattern Layout**

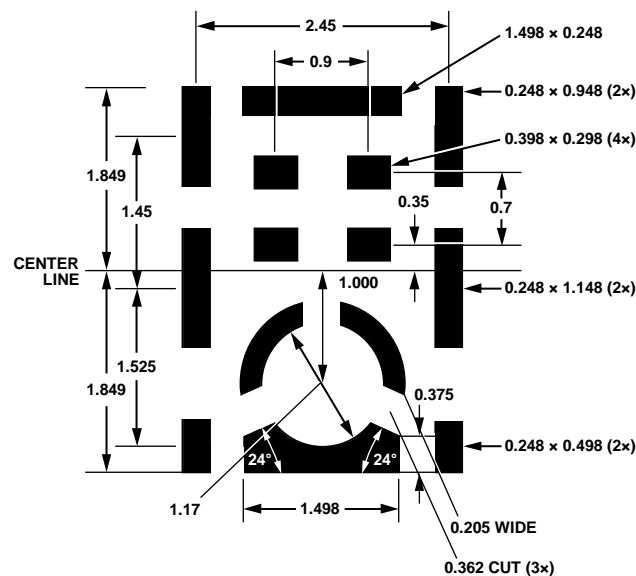


Figure 14. Suggested Solder Paste Stencil Pattern Layout



### ALTERNATIVE PCB LAND PATTERNS

The standard PCB land pattern of the ADMP421 has a solid rectangle around the edge of the footprint (see Figure 14). In some board designs, this rectangle can make routing the microphone signals more difficult. The rectangle is used to improve the RF immunity performance of the ADMP421; however, it is not necessary to have the full rectangle connected for electrical functionality. If a design can tolerate reduced RF immunity, this ring can either be broken or removed completely from the PCB footprint.

Figure 15 shows an example PCB land pattern with no enclosing rectangle around the edge of the part.

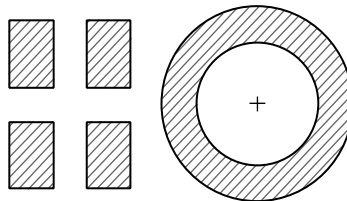


Figure 15. Example PCB Land Pattern with No Enclosing Rectangle

Figure 16 shows an example PCB land pattern with the rectangle broken on two sides so that the inner pads can be more easily routed on the PCB.

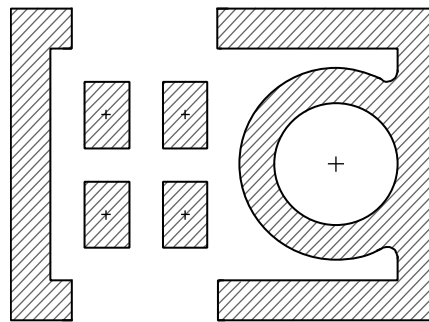


Figure 16. Example PCB Land Pattern with Broken Enclosing Rectangle

Note that in both of these patterns, the solid ring around the sound port is still present; this ring is needed to ground the microphone and for acoustic performance. The pad on the package connected to this ring is ground and still needs a solid electrical connection to the PCB ground.

If a land pattern similar to Figure 15 or Figure 16 is used on a PCB, make sure that the unconnected ring on the bottom of the ADMP421 is not placed directly over any exposed copper. The rectangle on the microphone is still at ground, and any PCB traces routed beneath it must be properly masked to avoid short circuits.

### PCB MATERIAL AND THICKNESS

The performance of the ADMP421 is not affected by PCB thickness. The ADMP421 can be mounted on either a rigid or flexible PCB. A flexible PCB with the microphone can be attached directly to the device housing with an adhesive layer. This mounting method offers a reliable seal around the sound port while providing the shortest acoustic path for good sound quality.

## **HANDLING INSTRUCTIONS**

### **PICK AND PLACE EQUIPMENT**

The MEMS microphone can be handled using standard pick-and-place and chip shooting equipment. Take care to avoid damage to the MEMS microphone structure as follows:

- Use a standard pickup tool to handle the microphone. Because the microphone hole is on the bottom of the package, the pickup tool can make contact with any part of the lid surface.
- Do not pick up the microphone with a vacuum tool that makes contact with the bottom side of the microphone.  
Do not pull air out of or blow air into the microphone port.
- Do not use excessive force to place the microphone on the PCB.

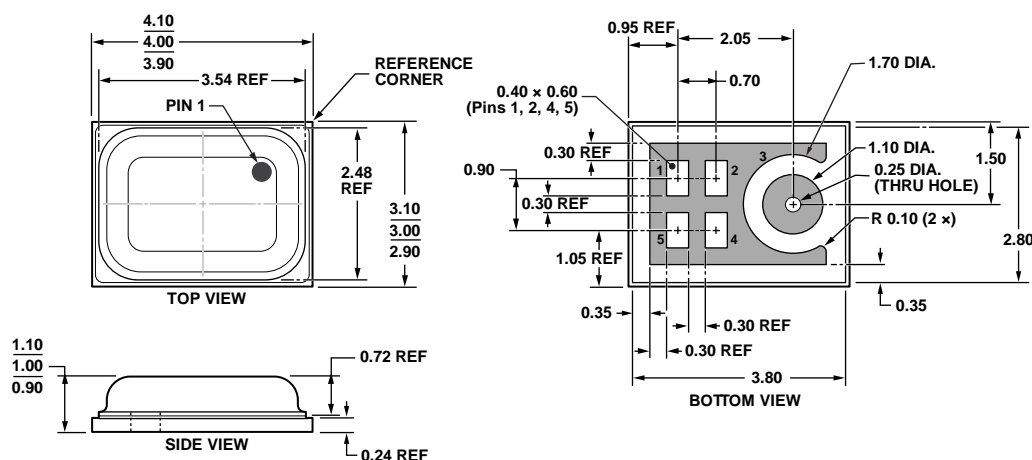
### **REFLOW SOLDER**

For best results, the soldering profile must be in accordance with the recommendations of the manufacturer of the solder paste used to attach the MEMS microphone to the PCB. It is recommended that the solder reflow profile not exceed the limit conditions specified in Figure 2 and Table 4.

### **BOARD WASH**

When washing the PCB, ensure that water does not make contact with the microphone port. Do not use blow-off procedures or ultrasonic cleaning.

## OUTLINE DIMENSIONS



04-19-2012-G

Figure 17. 5-Terminal Chip Array Small Outline No Lead Cavity [LGA\_CAV]  
 4 × 3 × 1 mm Body  
 (CE-5-1)  
 Dimensions shown in millimeters

## ORDERING GUIDE

PART	TEMP RANGE	PACKAGE	PACKAGE OPTION	QUANTITY
ADMP421ACEZ-RL	-40°C to +85°C	5-Terminal LGA_CAV*	CE-5-1	5,000
ADMP421ACEZ-RL7	-40°C to +85°C	5-Terminal LGA_CAV†	CE-5-1	1,000
EVAL-ADMP421Z-FLEX	—	Flexible Evaluation Board	—	—
EVAL-ADMP421Z	—	Evaluation Board	—	—

\* – 13" Tape and Reel

† – 7" Tape and Reel

## REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
11/25/2013	1.0	Initial Release

**Compliance Declaration Disclaimer:**

InvenSense believes this compliance information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense

**Environmental Declaration Disclaimer:**

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