



Rev. 1.0

AS7C316096A

2048K X 8 BIT HIGH SPEED CMOS SRAM

REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issued	Oct. 26. 2012

FEATURES

- Fast access time : 10ns
- **low power consumption:**
Operating current:
90mA (Icc1 typical)
Standby current:
4mA(Typical)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 48-pin 12mm x 20mm TSOP-I

GENERAL DESCRIPTION

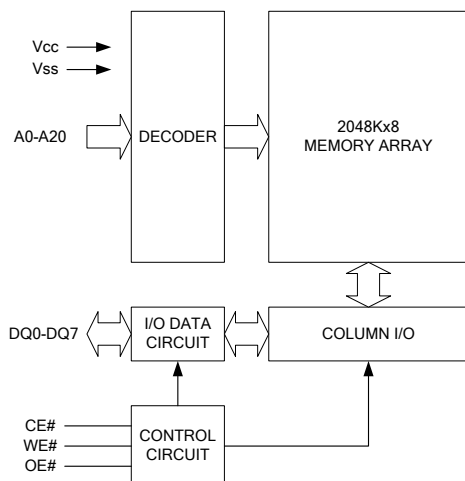
The AS7C316096A is a 16M-bit high speed CMOS static random access memory organized as 2048K words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C316096A operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,TYP.)	Operating(I _{CC1} ,TYP.)
AS7C316096A(I)	-40 ~ 85°C	2.7 ~ 3.6V	10	4mA	90mA

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A20	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground

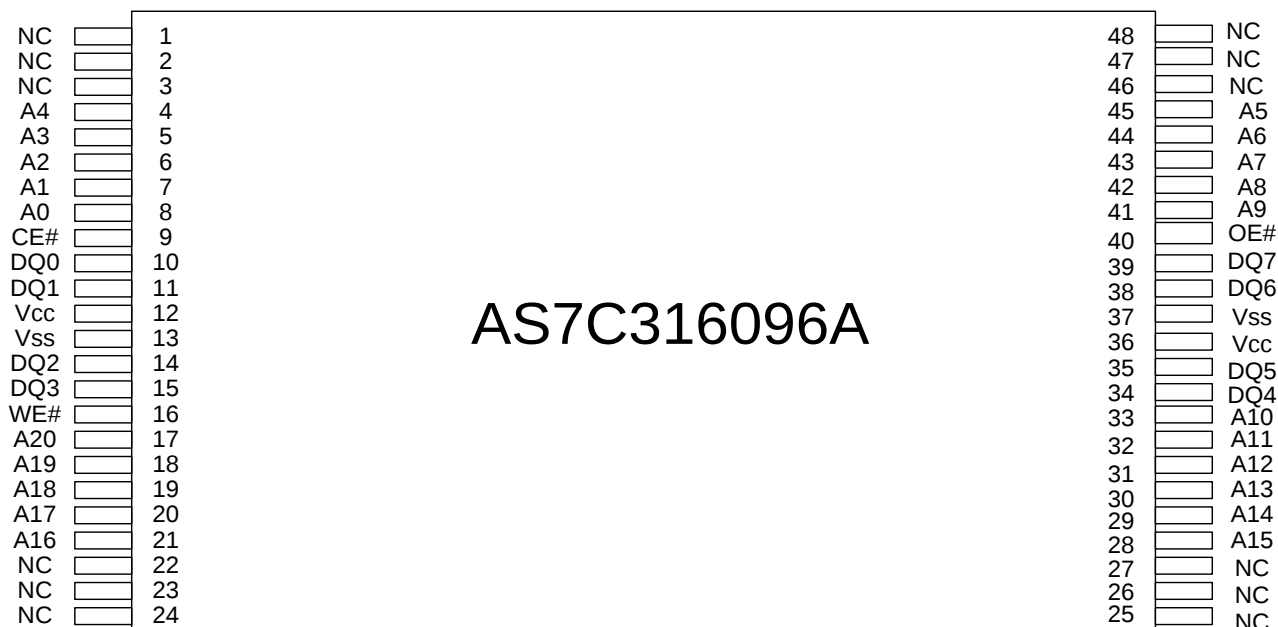


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PIN CONFIGURATION



TSOP-I

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to Vcc+0.5	V
Operating Temperature	T _A	-40 to 85(l grade)	°C
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	High-Z	I _{CC} , I _{CC1}
Read	L	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ^{*4}	MAX.	UNIT
Supply Voltage	V _{CC}		2.7	3.3	3.6	V
Input High Voltage	V _{IH} ^{*1}		2.2	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL} ^{*2}		- 0.3	-	0.8	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -8mA	2.4	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 4mA	-	-	0.4	V
Average Operating Power supply Current	I _{CC}	CE# = V _{IL} , I _{I/O} = 0mA ;f=max	-10	-	110	mA
	I _{CC1}	CE# ≤ 0.2, Other pin is at 0.2V or V _{CC} -0.2V I _{I/O} = 0mA;f=max	-10	-	90	mA
Standby Power Supply Current	I _{SB}	CE# ≥ V _{IH} Other pin is at V _{IL} or V _{IH}	-	-	80	mA
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} - 0.2V; Other pin is at 0.2V or V _{CC} -0.2V	-	4	40	mA

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C



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CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	8	pF
Input/Output Capacitance	C _{I/O}	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

speed	10ns
Input Pulse Levels	0.2V to V _{CC} -0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	V _{CC} /2
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -8mA/4mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS7C316096A -10		UNIT
		MIN.	MAX.	
Read Cycle Time	t _{RC}	10	-	ns
Address Access Time	t _{AA}	-	10	ns
Chip Enable Access Time	t _{ACE}	-	10	ns
Output Enable Access Time	t _{OE}	-	4.5	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	2	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	0	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	4	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	4	ns
Output Hold from Address Change	t _{OH}	2	-	ns

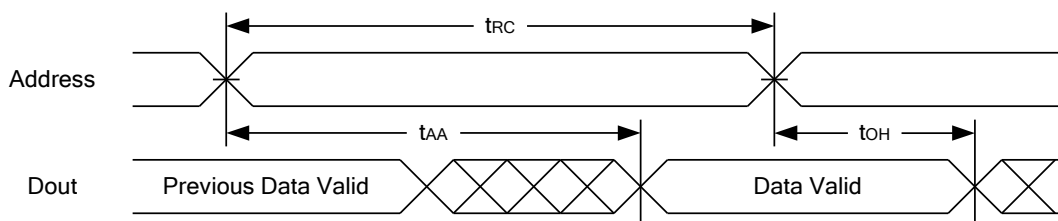
(2) WRITE CYCLE

PARAMETER	SYM.	AS7C316096A -10		UNIT
		MIN.	MAX.	
Read Cycle Time	t _{RC}	10	-	ns
Address Access Time	t _{AA}	-	10	ns
Chip Enable Access Time	t _{ACE}	-	10	ns
Output Enable Access Time	t _{OE}	-	4.5	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	2	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	0	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	4	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	4	ns
Output Hold from Address Change	t _{OH}	2	-	ns

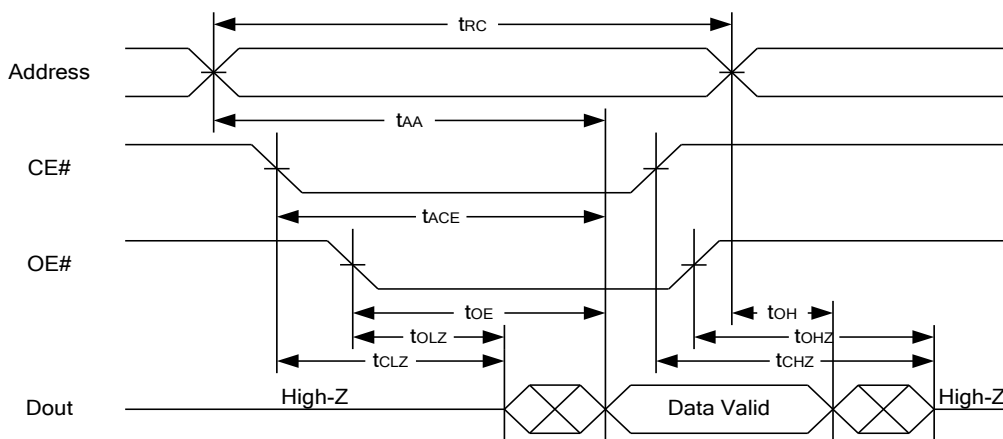
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



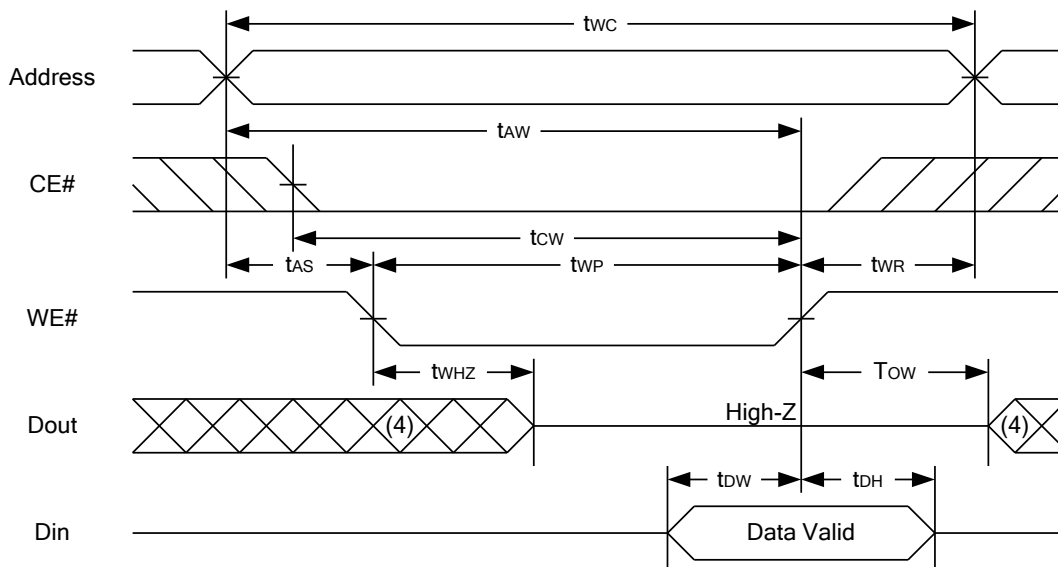
READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



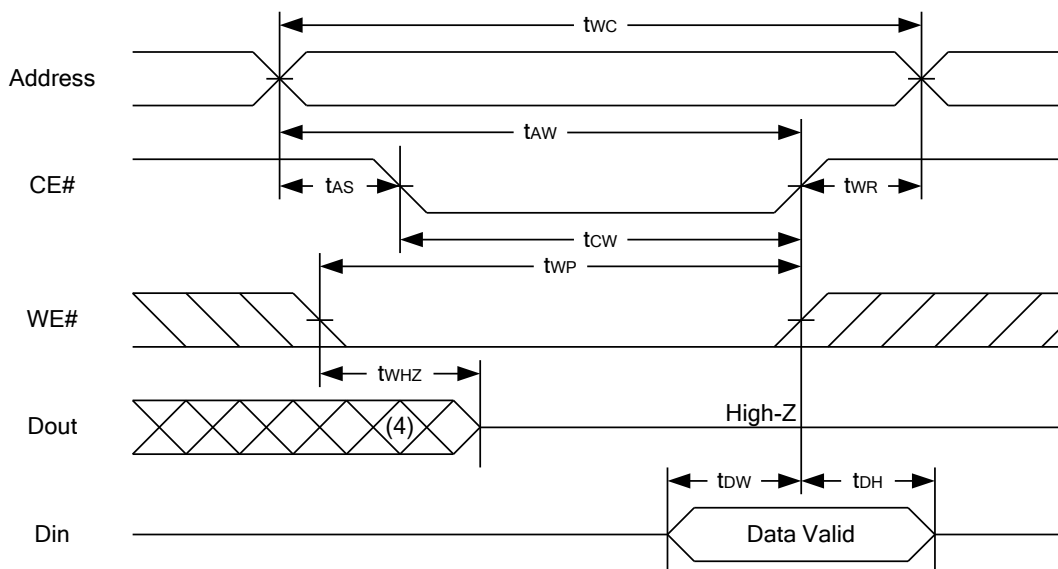
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low,; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



Notes :

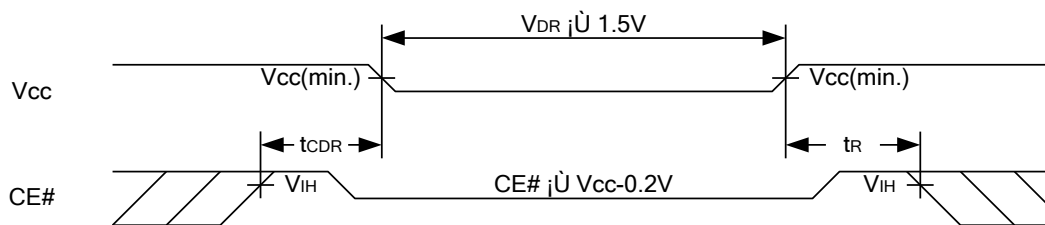
1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tOW and tWHZ are specified with CL = 5pF. Transition is measured $\pm 500\text{mV}$ from steady state.

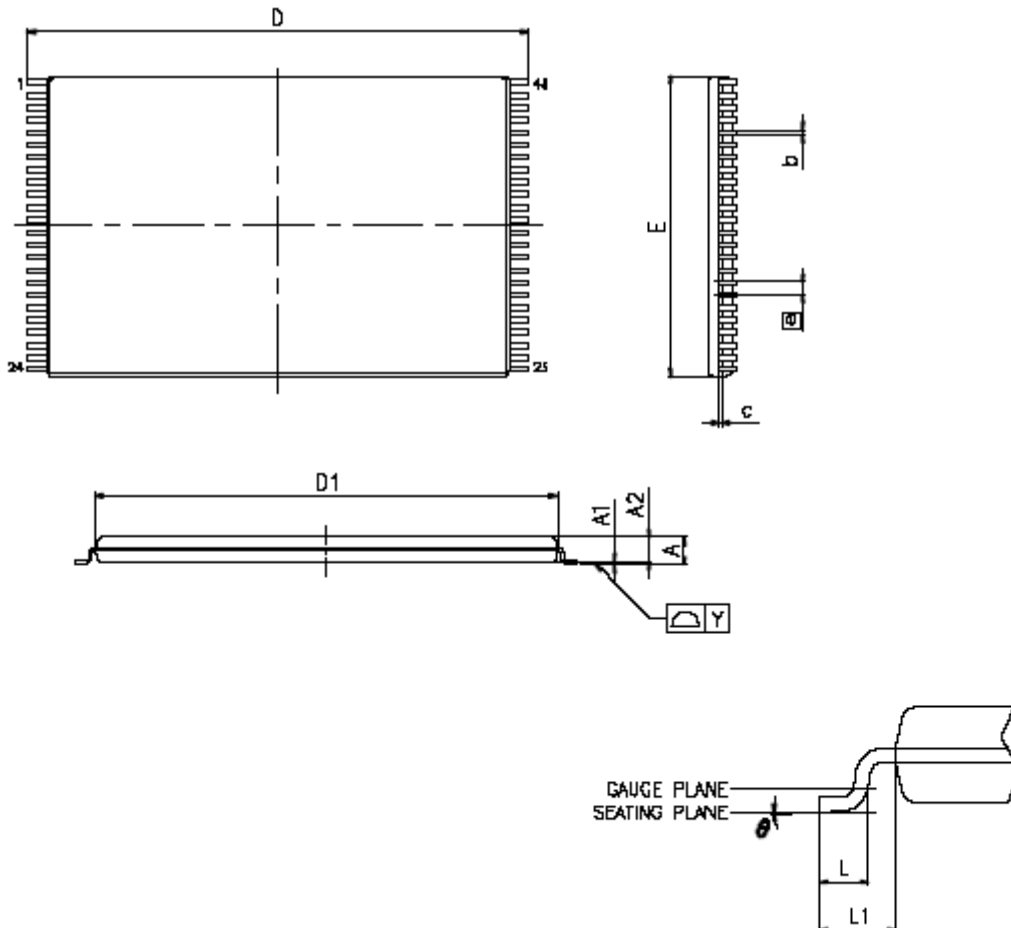
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VCC for Data Retention	V _{DR}	CE# $\geq$ V _{CC} - 0.2V	1.5	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# $\geq$ V _{CC} - 0.2V; Other pin is at 0.2V or V _{CC} -0.2V	-	4	40	mA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM



PACKAGE OUTLINE DIMENSION
48-pin 12mm x 20mm TSOP-I Package Outline Dimension

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

	SYMBOLS	MIN.	NOM.	MAX
	A	—	—	1.20
	A1	0.05	—	0.15
	A2	0.95	1.00	1.05
	b	0.17	0.22	0.27
	c	0.10	—	0.21
▲	D	19.80	20.00	20.20
▲	D1	18.30	18.40	18.50
▲	E	11.90	12.00	12.10
	e	0.50 BASIC		
	L	0.50	0.60	0.70
▲	L1	—	0.80	—
▲	Y	—	—	0.10
▲	θ	0°	—	5°

NOTES:

1 JEDEC OUTLINE : MO-142 DD

2. PROFILE TOLERANCE ZONES FOR D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.

3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.



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ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Temperature Range(°C)	Packing Type	Alliance Memory Item No.
48-pin(12mmx20mm) TSOP-I	10	-40°C~85°C	Tray	AS7C316096A -10TIN
			Tape Reel	AS7C316096A -10TINTR



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