NVT4857UK

SD 3.0-SDR104 compliant integrated auto-direction control memory card voltage level translator with EMI filter and ESD protection

Rev. 2 — 6 June 2018 Product data sheet

1. General description

The device is an SD 3.0-compliant bidirectional dual voltage level translator with auto-direction control. It is designed to interface between a memory card operating at 1.8 V or 3.0 V signal levels and a host with a nominal supply voltage of 1.2 V to 1.8 V. The device supports SD 3.0 SDR104, SDR50, DDR50, SDR25, SDR12 and SD 2.0 High-Speed (50 MHz) and Default-Speed (25 MHz) modes. The device has an integrated voltage selectable low dropout regulator to supply the card-side I/Os, an auto-enable/disable function connected to the V_{SD} supply pin, built-in EMI filters and robust ESD protections (IEC 61000-4-2, level 4).

2. Features and benefits

- Supports up to 208 MHz clock rate
- SD 3.0 specification-compliant voltage translation to support SDR104, SDR50, DDR50, SDR25, SDR12, High-Speed and Default-Speed modes
- 1.2 V to 1.8 V host side interface voltage support
- Feedback channel for clock synchronization
- 100 mA Low dropout voltage regulator to supply the card-side I/Os
- Low power consumption by push-pull output stage with break-before-make architecture
- Automatic enable and disable through V_{SD}
- Integrated pull-up and pull-down resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Integrated 8 kV ESD protection according to IEC 61000-4-2, level 4 on card side
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- 20-ball WLCSP; pitch 0.4 mm

3. Applications

- Smart phones
- Mobile handsets
- Digital cameras
- Tablet PCs
- Laptop computers
- SD, MMC or microSD card readers

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
NVT4857UK	N4857	WLCSP20	wafer level chip-size package; 20 bumps (5 × 4), size 1.7 x 2.1 x 0.49 mm, 0.4 mm pitch	NVT4857

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NVT4857UK	NVT4857UKZ	WLCSP20	REEL 7" Q1/T1 *SPECIAL MARK CHIPS DP	500	T_{amb} = −40 °C to +85 °C
NVT4857UK	NVT4857UKAZ	WLCSP20	REEL 13" Q1/T1 *SPECIAL MARK CHIPS DP	10000	T_{amb} = −40 °C to +85 °C

5. Block diagram

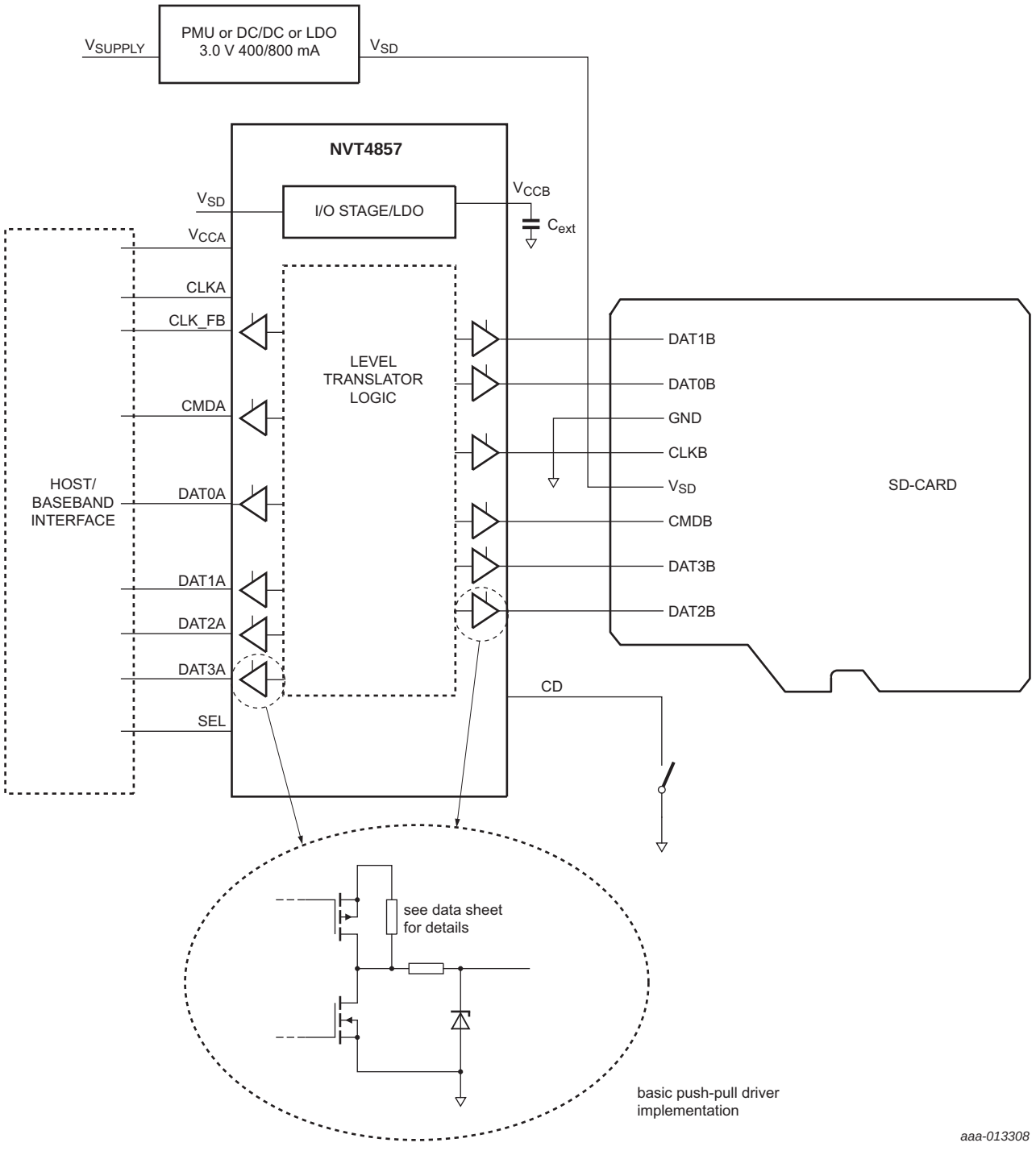


Fig 1. Application diagram

6. Functional diagram

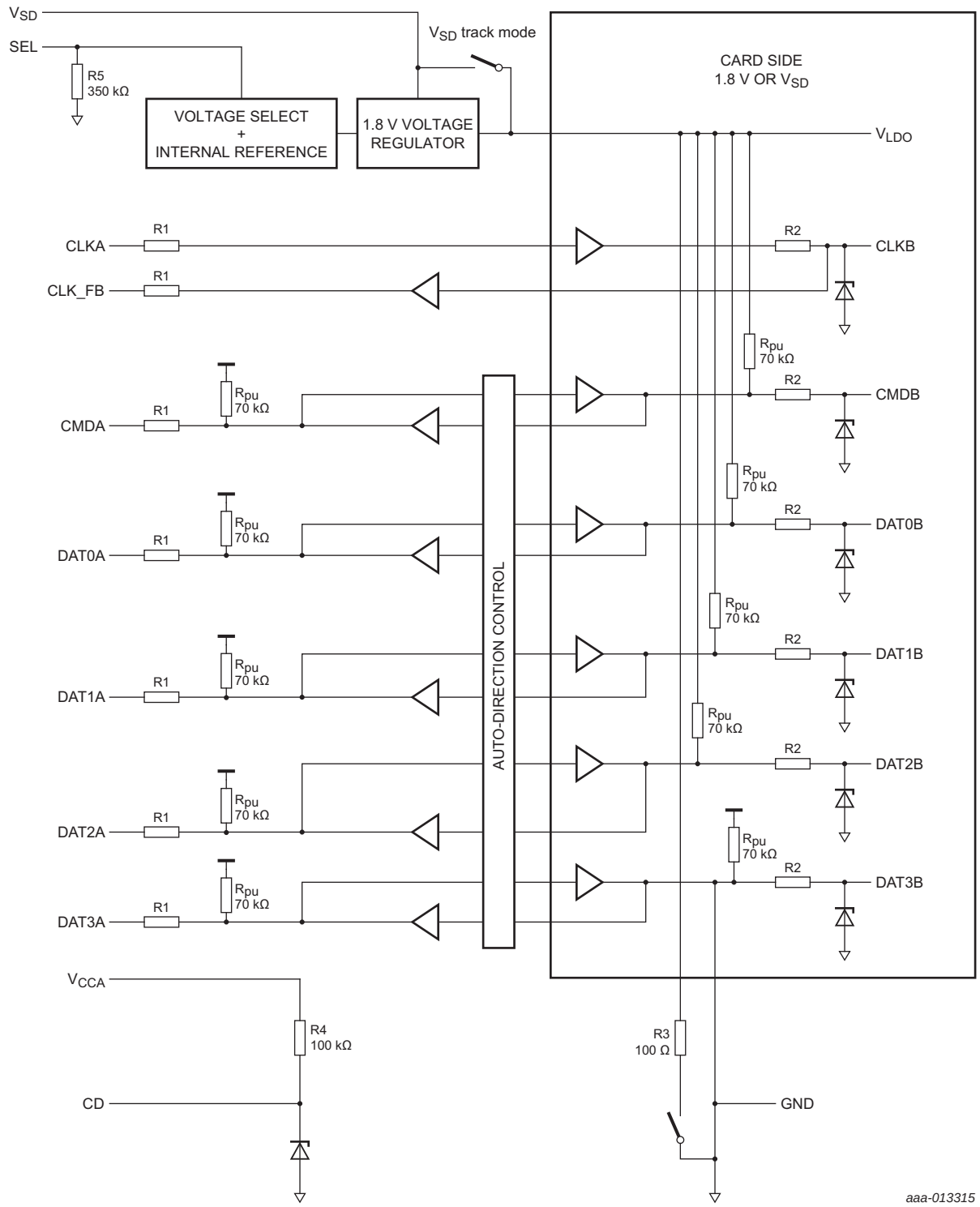


Fig 2. Functional diagram

7. Pinning information

7.1 Pinning

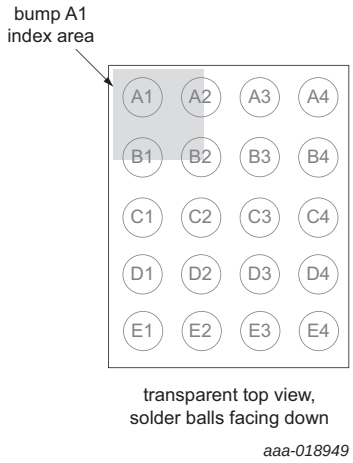


Fig 3. Pin configuration WLCSP20

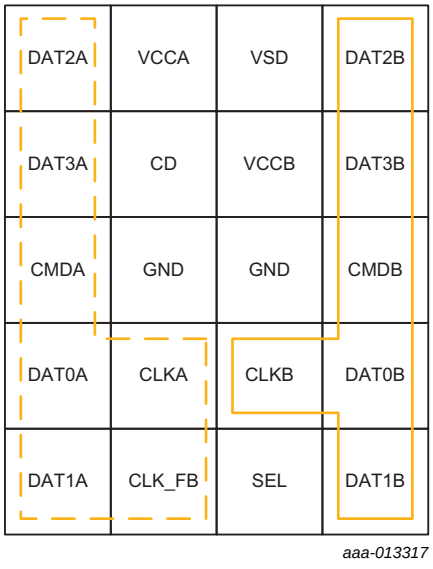


Fig 4. NVT4857UK pinout transparent top view

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
A1	DAT2A	A2	V_{CCA}	A3	V_{SD}	A4	DAT2B
B1	DAT3A	B2	CD	B3	V_{CCB}	B4	DAT3B
C1	CMDA	C2	GND	C3	GND	C4	CMDB
D1	DAT0A	D2	CLKA	D3	CLKB	D4	DAT0B
E1	DAT1A	E2	CLK_FB	E3	SEL	E4	DAT1B

7.2 Pin description

Table 4. Pin description

Symbol [1]	Pin	Type [2]	Description
DAT2A	A1	I/O	data 2 input or output on host side
V_{CCA}	A2	S	supply voltage from host side
V_{SD}	A3	S	supply voltage
DAT2B	A4	I/O	data 2 input or output on memory card side
DAT3A	B1	I/O	data 3 input or output on host side
CD	B2	O	card detect switch biasing output
V_{CCB}	B3	S	internal supply decoupling (V_{LDO})
DAT3B	B4	I/O	data 3 input or output on memory card side
CMDA	C1	I/O	command input or output on host side
GND	C2	S	supply ground
GND	C3	S	supply ground
CMDB	C4	I/O	command input or output on memory card side
DAT0A	D1	I/O	data 0 input or output on host side
CLKA	D2	I	clock signal input on host side
CLKB	D3	O	clock signal output on memory card side
DAT0B	D4	I/O	data 0 input or output on memory card side
DAT1A	E1	I/O	data 1 input or output on host side
CLK_FB	E2	O	clock feedback output on host side
SEL	E3	I	card side I/O voltage level select
DAT1B	E4	I/O	data 1 input or output on memory card side

[1] The pin names relate particularly to SD memory cards, but also apply to microSD and MMC memory cards.

[2] I = input, O = output, I/O = input and output, S = power supply

8. Functional description

8.1 Level translator

The bidirectional level translator shifts the data between the I/O supply levels of the host and the memory card. The voltage translator has to support several clock and data transfer rates at the signaling levels specified in the SD 3.0 standard specification.

Table 5. Supported modes

Bus speed mode	Signal level (V)	Clock rate (MHz)	Data rate (MB/s)
Default-Speed	3.3	25	12.5
High-Speed	3.3	50	25
SDR12	1.8	25	12.5
SDR25	1.8	50	25
SDR50	1.8	100	50
SDR104	1.8	208	104
DDR50	1.8	50	50

8.2 Enable and direction control

The device contains an auto-enable feature. If V_{SD} rises above 2.65 V, the LDO and the level translator logic is enabled automatically. As soon as V_{SD} drops below the $V_{SDdisable}$, as specified in Table 10, the LDO and the card side drivers and the level translator logic is disabled. All host side pins excluding CLKA[1] are configured as inputs with a 70 kΩ resistor pulled up to V_{CCA}.

8.3 Integrated voltage regulator

The low dropout voltage regulator delivers supply voltage for the voltage translators and the card-side input/output stages. It has to support 1.8 V and 3 V signaling modes as stipulated in the SD 3.0 specification. The switching time between the two output voltage modes is compliant with SD 3.0 specification. Depending on the signaling level at pin SEL, the regulator delivers 1.8 V (SEL = HIGH) or 3.0 V (SEL = LOW).

Table 6. SD card side voltage level control signal truth table

Input	Output		
SEL[1]	**V_{CCB}**	**Pin[2]**	**Function**
H	1.8 V	DAT0B to DAT3B, CLKB	low supply voltage level (1.8 V_{typ})
L	tracking V_{SD}	DAT0B to DAT3B, CLKB	high supply voltage level (tracking V_{SD})

[1] H = HIGH; L = LOW; X = don't care

[2] Host-side pins are not influenced by SEL.

An external capacitor is needed between the regulator output pin V_{CCB} and ground for proper operation of the integrated voltage regulator. See Table 8 for recommended capacitance and equivalent series resistance. It is recommended to place the capacitor close to the V_{SD} and V_{CCB} pin and maintain short connections of both to ground.

1. CLKA is a pure high-ohmic input. Please refer to Figure 2 "Functional diagram" for more detail.

8.4 Feedback clock channel

The clock is transmitted from the host to the memory card side. The voltage translator and the Printed-Circuit Board (PCB) tracks introduce some amount of delay. It reduces timing margin for data read back from memory card, especially at higher data rates. Therefore, a feedback path is provided to compensate the delay. The reasoning behind this approach is the fact that the clock is always delivered by the host, while the data in the timing critical read mode comes from the card.

8.5 EMI filter

All input/output driver stages are equipped with EMI filters to reduce interferences towards sensitive mobile communication.

8.6 ESD protection

The device has robust ESD protections on all memory card pins as well as on the V_{SD} pin. The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground.

Pin Card Detection (CD) might be pulled down by the memory card which has to be detected by the host. The pin is equipped with International Electrotechnical Commission (IEC) system-level ESD protection and pull-up resistor connected to the host supply V_{CCA}.

9. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	4 ms transient			
		on pin V_{SD}	–0.5	+4.6	V
		on pin V_{CCA}	–0.5	+4.6	V
V_I	input voltage	4 ms transient at I/O pins	–0.5	+4.6	V
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C	-	1000	mW
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4, all memory card-side pins, V_{SD} and CD to ground [1]			
		contact discharge	–8	+8	kV
		air discharge	–15	+15	kV
		Human Body Model (HBM) JEDEC JESD22-A114F; all pins	–2000	+2000	V
		Charge Device Model (CDM) JEDEC JESD22-C101E; all pins	–500	+500	V
$I_{lu(IO)}$	input/output latch-up current	JESD 78B: $-0.5 \times V_{CC} < V_I < 1.5 \times V_{CC}$; T_j < 125 °C	–100	+100	mA

[1] All system level tests are performed with the application-specific capacitors connected to the supply pins V_{SUPPLY}, V_{LDO} and V_{CCA}.

10. Recommended operating conditions

Table 8. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	on pin V_{SD}	[1]	2.9	-	3.6	V
		on pin V_{CCA}		1.1	-	2.0	V
V_I	input voltage	host side	[2]	–0.3	-	V_{CCA} + 0.3	V
		memory card side		–0.3	-	$V_{O(LDO)}$ + 0.3	V
C_{ext}	external capacitance	recommended capacitor at pin V_{CCB}		-	2.2	-	µF
ESR	equivalent series resistance	at pin V_{LDO}		0	-	50	mΩ
C_{ext}	external capacitance	recommended capacitor at pin V_{SD}		-	0.1	-	µF
		recommended capacitor at pin V_{CCA}		-	0.1	-	µF

[1] By minimum value the device is still fully functional, but the voltage on pin V_{LDO} might drop below the recommended memory card supply voltage.

[2] The voltage must not exceed 3.6 V.

Table 9. Integrated resistors

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{pd}	pull-down resistance	R3; tolerance ±30 %		70	100	130	Ω
		R5		200	350	500	kΩ
R_{pu}	pull-up resistance	all data lines and CMDx		49	70	91	kΩ
		R4		70	100	130	kΩ
R_S	series resistance	host side; R1; tolerance ±30 %	[1]	-	22.5	-	Ω
		card side; R2; tolerance ±30 %	[1]	-	15	-	Ω

[1] Guaranteed by design.

11. Static characteristics

Table 10. Static characteristics

At recommended operating conditions; T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); C_{ext} = 2.2 µF at pin V_{CCB}; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
Automatic enable feature: V_{SD}						
V_{SDen}	device enable voltage level	$V_{CCA} \geq 1.0$ V, V_{SD} rising edge	2.25	2.45	2.65	V
$V_{SDdisable}$	device disable voltage level	$V_{CCA} \geq 1.0$ V, V_{SD} falling edge	2.2	2.4	2.6	V
ΔV_{SDen}	V_{SDen} hysteresis voltage		-	50	-	mV
Supply voltage regulator for card-side I/O pin: V_{CCB}						
$V_{O(LDO)}$	regulator/switch output voltage	SEL = LOW;3.0 V ≤ V_{SD} ≤ 3.6 V; I_O < 100 mA	V_{SD}-0.2	V_{SD}-0.1	V_{SD}	V
		SEL = HIGH; $V_{SD} \geq 2.9$ V; I_O < 100 mA	1.7	1.8	1.95	V
$I_{O(LDO)}$	regulator/switch output current		-	-	100	mA
Host-side input signals: CMDA and DAT0A to DAT3A, CLKA; 1.1 V ≤ V_{CCA} ≤ 2.0 V						
V_{IH}	HIGH-level input voltage		0.75 × V_{CCA}	-	V_{CCA} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	0.25 × V_{CCA}	V
Host-side control signals; 1.1 V ≤ V_{CCA} ≤ 2.0 V						
SEL						
V_{IH}	HIGH-level input voltage		0.75 × V_{CCA}	-	V_{CCA} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	0.25 × V_{CCA}	V
Host-side output signals: CLK_FB, CMDA and DAT0A to DAT3A; 1.1 V ≤ V_{CCA} ≤ 2.0 V						
V_{OH}	HIGH-level output voltage for CLK_FB	I_O = 2 mA; $V_I = V_{IH}$ (card side)	0.8 × V_{CCA}	-	-	V
	HIGH-level output voltage for CMDA, DATxA	I_O = 2 µA; $V_I = V_{IH}$ (card side)	0.8 × V_{CCA}	-	-	V
V_{OL}	LOW-level output voltage	I_O = −2 mA; $V_I = V_{IL}$ (card side)	-	-	0.15 × V_{CCA}	V

Table 10. Static characteristics *...continued*

At recommended operating conditions; T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); C_{ext} = 2.2 µF at pin V_{CCB}; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
Card-side input signals: CMDB and DAT0B to DAT3B						
V_{IH}	HIGH-level input voltage	SEL = LOW (3.0 V card interface)	0.625 × $V_{O(LDO)}$	-	$V_{O(LDO)}$ + 0.3	V
		SEL = HIGH (1.8 V card interface)	0.625 × $V_{O(LDO)}$	-	$V_{O(LDO)}$ + 0.3	V
V_{IL}	LOW-level input voltage	SEL = LOW (3.0 V card interface)	−0.3	-	0.3 × $V_{O(LDO)}$	V
		SEL = HIGH (1.8 V card interface)	−0.3	-	0.35 × $V_{O(LDO)}$	V
Card-side output signal						
CMDB and DAT0B to DAT3B, CLKB						
V_{OH}	HIGH-level output voltage for CLKB only	I_O = 4 mA; V_I = V_{IH} (host side); SEL = LOW (3.0 V card interface)	0.85 × $V_{O(LDO)}$	-	$V_{O(LDO)}$ + 0.3	V
		I_O = 2 mA; V_I = V_{IH} (host side); SEL = HIGH (1.8 V card interface)	0.85 × $V_{O(LDO)}$	-	2.0	V
	HIGH-level output voltage for CMDB, DATxB	I_O = 2 µA; V_I = V_{IH} (host side); SEL = HIGH (1.8 V card interface)	0.85 × $V_{O(LDO)}$	-	2.0	V
V_{OL}	LOW-level output voltage	I_O = −4 mA; V_I = V_{IL} (host side); SEL = LOW (2.9 V card interface)	−0.3	-	0.125 × $V_{O(LDO)}$	V
		I_O = −2 mA; V_I = $V_{I\ card\ L}$ (host side); SEL = HIGH (1.8 V interface)	−0.3	-	0.125 × $V_{O(LDO)}$	V
Bus signal equivalent capacitance						
C_{ch}	channel capacitance	V_I = 0 V; f_i = 1 MHz; V_{SD} = 3.0 V; V_{CCA} = 1.8 V [3]				
		host side	-	7	-	pF
		card side	-	15	-	pF
Current consumption						
$I_{CC(stat)}$	static supply current	$V_{SD} \geq V_{SDen}$ (active mode); all inputs = HIGH;				
		SEL = LOW (3.0 V card interface)	-	-	100	µA
		SEL = HIGH (1.8 V card interface)	-	-	100	µA
$I_{CC(stb)}$	standby supply current	$V_{SD} \leq V_{SDen}$ and $V_{CCA} \geq$ 1.0 V (inactive mode); all host side inputs = HIGH	-	-	7	µA

[1] Guaranteed by design and characterization.

[2] Typical values are measured at T_{amb} = 25 °C.

[3] EMI filter line capacitance per data channel from I/O driver to pin; C_{ch} is guaranteed by design.

12. Dynamic characteristics

12.1 Voltage regulator

Table 11. Voltage regulator

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage regulator output pin: V_{CCB}						
$t_{startup(LDO)}$	regulator start-up time	V_{CCA} = 1.8 V; V_{SD} = 3.0 V; C_{ext} = 2.2 µF; see Figure 6	-	-	400	µs
$t_{f(o)}$	output fall time	$V_{O(LDO)}$ = 3.0 V to 1.8 V; SEL = LOW to HIGH; see Figure 5	-	-	1	ms
$t_{r(o)}$	output rise time	$V_{O(LDO)}$ = 1.8 V to 3.0 V; SEL = HIGH to LOW; see Figure 5	-	-	100	µs

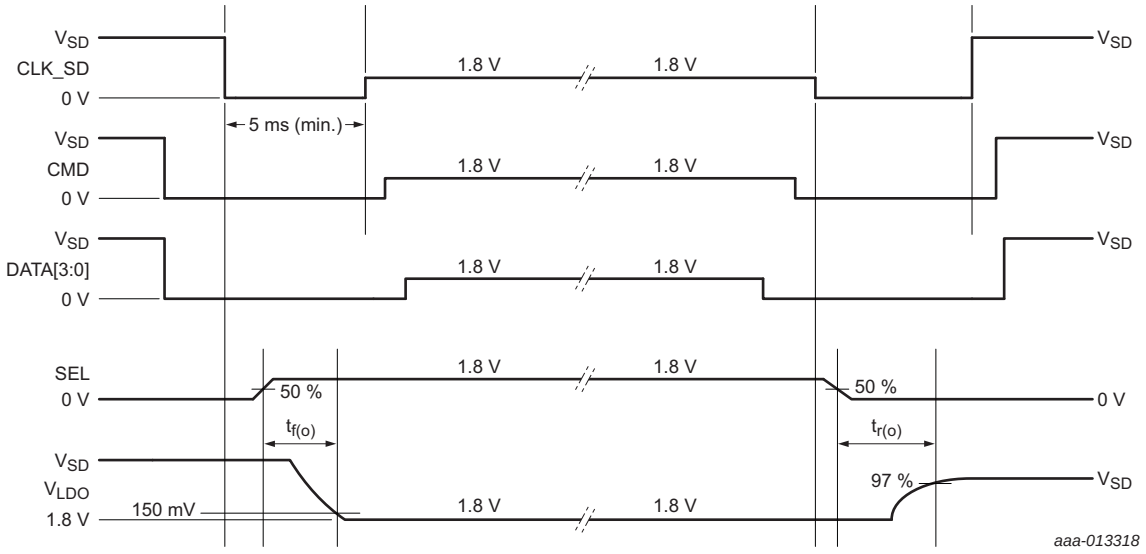
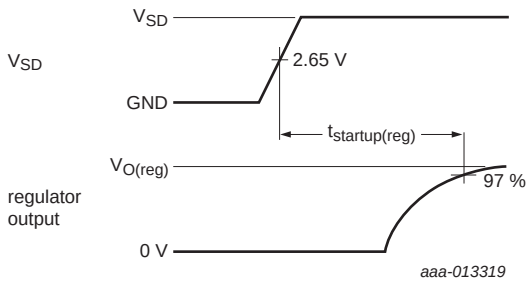


Fig 5. Regulator mode change timing



Measuring points: V_{SD} signal at 2.65 V and regulator output signal at 0.97 $V_{O(LDO)}$.

Fig 6. Regulator start-up time

12.2 Level translator

Table 12. Level translator dynamic characteristics

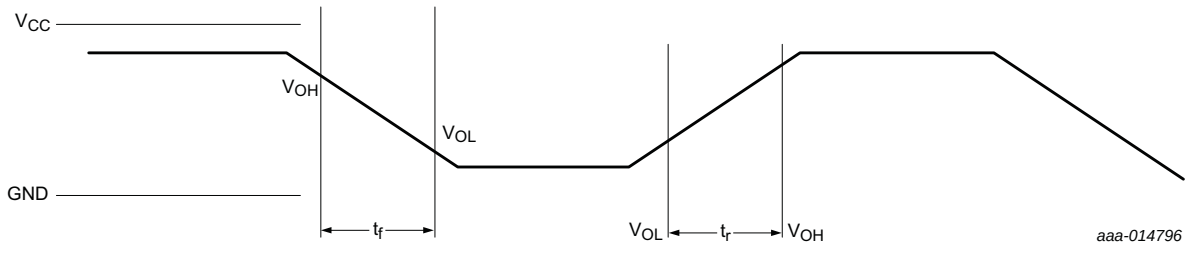
At recommended operating conditions; V_{CCA} = 1.2 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Host side transition times							
t_r	rise time	SEL = HIGH (1.8 V card interface); V_{CCA} = 1.8 V	[1]	-	0.4	1.0	ns
t_f	fall time		[1]	-	0.4	1.0	ns
t_r	rise time	SEL = HIGH (1.8 V card interface); V_{CCA} = 1.2 V	[1]	-	0.4	1.0	ns
t_f	fall time		[1]	-	0.4	1.0	ns
Card side transition times							
t_r	rise time	SEL = HIGH (1.8 V card interface); −40 °C ≤ T_{amb} ≤ +85 °C	[2]	0.4	0.88	1.32	ns
t_f	fall time		[2]	0.4	0.88	1.32	ns
Card input transition times							
t_r	rise time	SEL = HIGH (1.8 V card interface); −40 °C ≤ T_{amb} ≤ +85 °C	[3]	0.2	0.5	0.96	ns
t_f	fall time		[3]	0.2	0.45	0.96	ns
Host to card propoagation delay							
DATxA to DATxB, CMDA to CMDB, CLKA to CLKB							
t_{pd}	propagation delay	SEL = HIGH (1.8 V card interface); V_{CCA} = 1.2 V		-	3.0	5.5	ns
CLKA to CLK_FB							
t_{pd}	propagation delay	SEL = HIGH (1.8 V card interface); V_{CCA} = 1.2 V		-	5.5	10.0	ns
Card to host propagation delay							
DATxB to DATxA, CMDB to CMDA							
t_{pd}	propagation delay	SEL = HIGH (1.8 V card interface); V_{CCA} = 1.2 V		-	2.5	4.5	ns

[1] transition between V_{OL} = 0.35 * V_{CCA} and V_{OH} = 0.65 * V_{CCA}

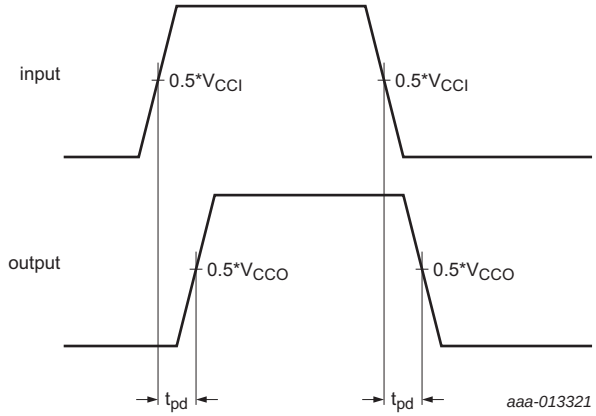
[2] transition between V_{OL} = 0.45 V and V_{OH} = 1.4 V

[3] Guaranteed by design; transition between V_{IL} = 0.58 V and V_{IH} = 1.27 V with C_{trace} = 3.5 pF and $C_{card+CRADLE}$ = 12 pF, trace length = 11 mm



V_{OH} and V_{OL} are specified in Table 12 as Table note [1] and Table note [2]

Fig 7. Output rise and fall times



Output delay is for every single channel, from input to output, 0.5*V_{CCI} to 0.5*V_{CCO}, in which V_{CCI} and V_{CCO} are the input and output voltage domain.

Fig 8. Output delay timing

12.3 ESD characteristic of pin card detect

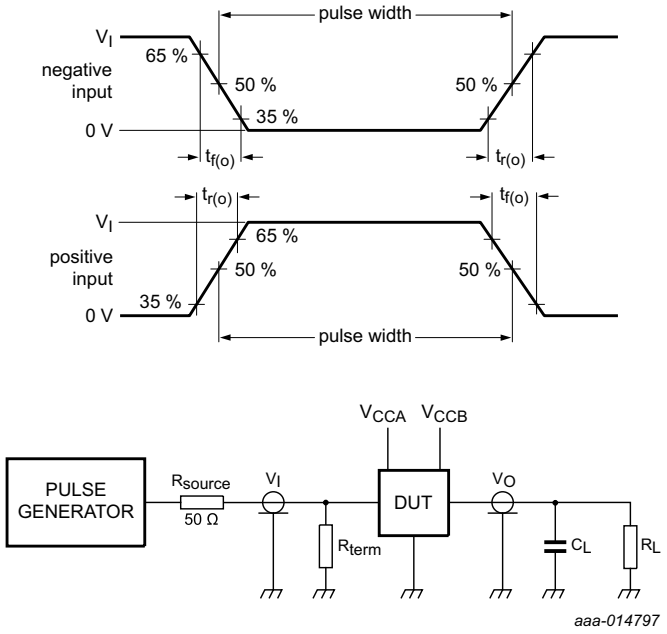
Table 13. ESD characteristic of card detect

At recommended operating conditions; T_{amb} = +25 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ESD protection pins: CD							
V_{BR}	breakdown voltage	TLP; I = 1 mA		-	8	-	V
r_{dyn}	dynamic resistance	positive transient	[1]	-	0.5	-	Ω
		negative transient	[1]	-	0.5	-	Ω

[1] TLP according to ANSI-ESD STM5.5.1/IEC 62615 Z_o = 50 Ω; pulse width = 100 ns; rise time = 200 ps; averaging window = 50 ns to 80 ns

13. Test information



Definitions test circuit:

R_{source} = source resistance of pulse generator.

R_{term} = termination resistance should be equal to output impedance Z_o of pulse generator.

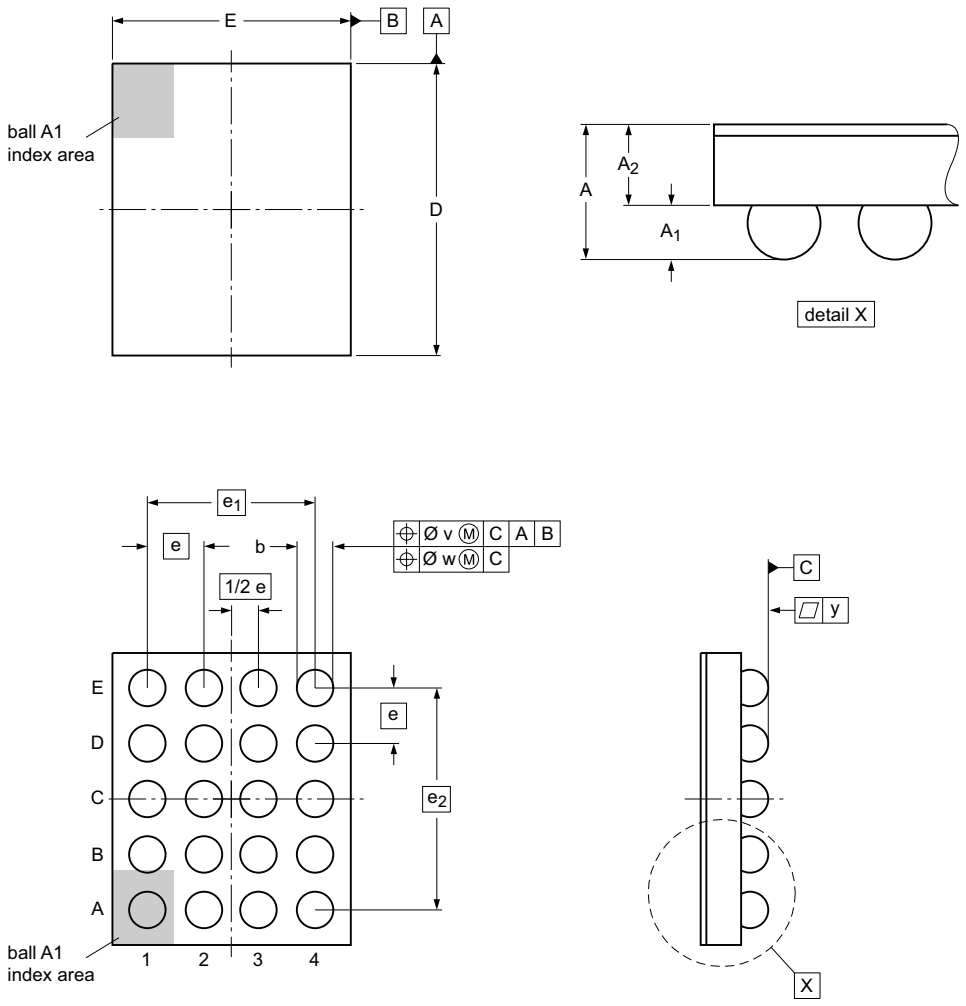
C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

Fig 9. Load circuitry for measuring switching time

14. Package outline

WLCSP20: wafer level chip-scale package; 20 bumps; 2.1 x 1.7 x 0.49 mm (Backside coating included) **NVT4857**



Dimensions (mm are the original dimensions)

Unit	A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
max	0.53	0.23	0.315	0.29	2.13	1.73						
mm nom	0.49	0.20	0.290	0.26	2.10	1.70	0.4	1.2	1.6	0.15	0.05	0.05
min	0.45	0.17	0.265	0.23	2.07	1.67						

Note: Backside coating 40 µm

wlcsp20_nvt4857_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
NVT4857						~~15-06-03~~ 15-07-21

Fig 10. Package outline NVT4857UK (WLCSP20)

15. Packing information

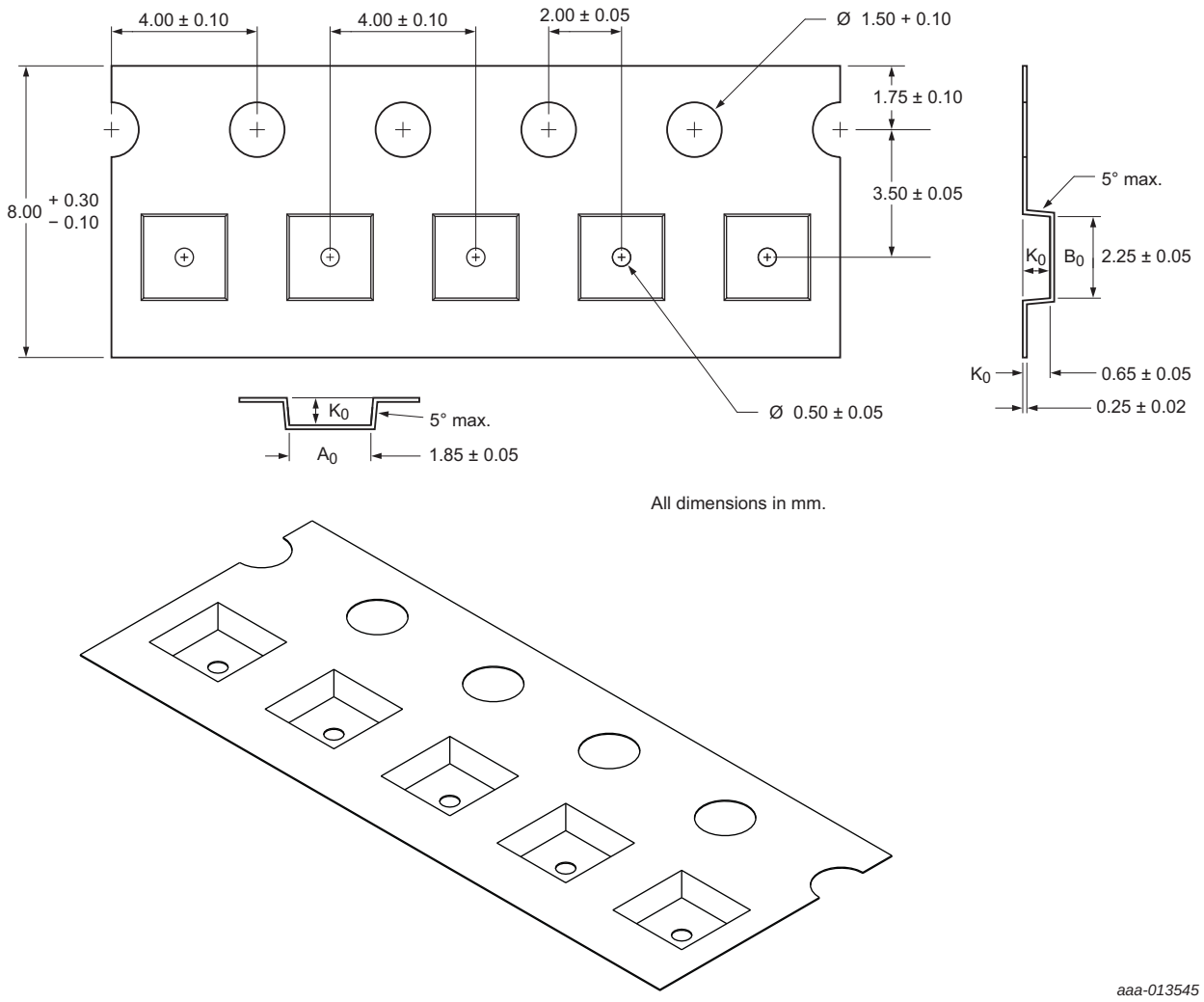


Fig 11. Carrier tape

16. Soldering of WLCSP packages

16.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

16.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

16.3 Reflow soldering

Key characteristics in reflow soldering are:

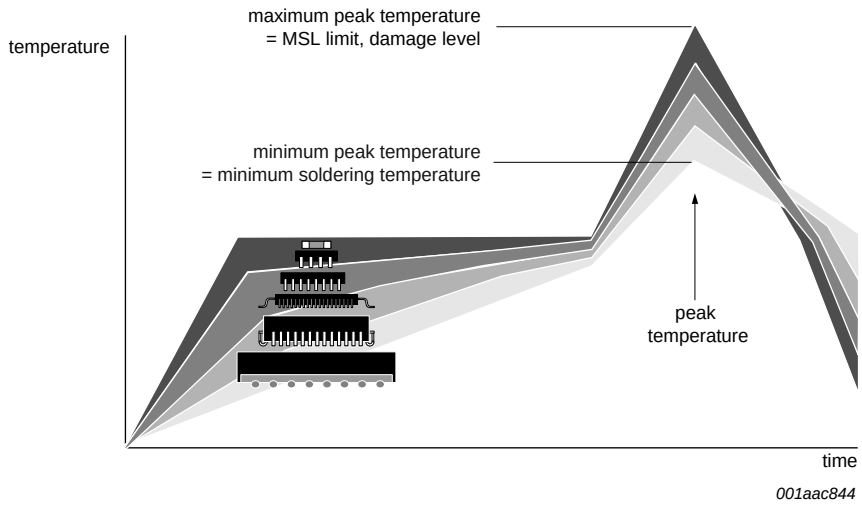
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 12) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14.

Table 14. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 12.



MSL: Moisture Sensitivity Level

Fig 12. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

16.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

16.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

16.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

16.3.4 Cleaning

Cleaning can be done after reflow soldering.

17. Abbreviations

Table 15. Abbreviations

Acronym	Description
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
MMC	MultiMedia Card
PCB	Printed-Circuit Board
RoHS	Restriction of Hazardous Substances
SD	Secure Digital
WLCSP	Wafer-Level Chip-Scale Package

18. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NVT4857UK v.2	20180606	Product data sheet	201805042I	NVT4857UK v.1.1
Modifications:	• Table 12 “Level translator dynamic characteristics”: – Updated typ and max values for Card side transition times t_r, t_f – Added Card input transition times t_r, t_f and associated Table note 3			
NVT4857UK v.1.1	20161213	Product data sheet	201612019I	NVT4857UK v.1
Modifications:	• Table 1 “Ordering information”: Corrected topside mark from “NV4857” to “N4857” to reflect the production marking; no impact to product functionality.			
NVT4857UK v.1	20151120	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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