

## ±15kV ESD, 5V, Full Fail-Safe, 1/8 Unit Load, RS-485/RS-422 Transceivers

The ISL8308xE are BiCMOS, ESD protected, 5V powered, single transceivers that meet both the RS-485 and RS-422 standards for balanced communication. Each driver output, and receiver input, is protected against ±15kV ESD strikes without latch-up, and unlike competitive products, this Intersil family is specified for 10% tolerance supplies (4.5V to 5.5V).

These devices have very low bus currents (+125μA/-75μA), so they present a true “1/8 unit load” to the RS-485 bus. This allows up to 256 transceivers on the network without violating the RS-485 specification’s 32 unit load maximum, and without using repeaters. For example, in a remote utility meter reading system, individual meter readings are routed to a concentrator via an RS-485 network, so the high allowed node count minimizes the number of repeaters required. Data for all meters is then read out from the concentrator via a single access port, or a wireless link.

Receiver (Rx) inputs feature a “Full Fail-Safe” design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or terminated but undriven.

The ISL83080E, ISL83082E, ISL83083E, ISL83084E, ISL83085E utilize slew rate limited drivers which reduce EMI, and minimize reflections from improperly terminated transmission lines, or unterminated stubs in multidrop and multipoint applications. Slew rate limited versions also include receiver input filtering to enhance noise immunity in the presence of slow input signals.

Hot Plug circuitry ensures that the Tx and Rx outputs remain in a high impedance state until the power supply has stabilized, and the Tx outputs are fully short circuit protected.

The ISL83080E, ISL83083E, ISL83084E, ISL83086E are configured for full duplex (separate Rx input and Tx output pins) applications. The half duplex versions multiplex the Rx inputs and Tx outputs to allow transceivers with output disable functions in 8 Ld packages.

## Features

- Pb-Free Available (RoHS Compliant)
- RS-485 I/O Pin ESD Protection . . . . . ±15kV HBM Class 3 ESD Protection (HBM) on all Pins. . . . . >7kV
- Tiny MSOP Packages Save 50% Board Space
- Full Fail-Safe (Open, Short, Terminated and Floating) Receivers
- Hot Plug Circuitry (ISL83080E, ISL83082E, ISL83083E, ISL83085E)
  - Tx and Rx Outputs Remain Three-state During Power-up/Power-down
- True 1/8 Unit Load Allows up to 256 Devices on the Bus
- Specified for Single 5V, 10% Tolerance, Supplies
- High Data Rates . . . . . up to 10Mbps
- Low Quiescent Supply Current . . . . . 530μA  
Ultra Low Shutdown Supply Current . . . . . 70nA
- -7V to +12V Common Mode Input Voltage Range
- Half and Full Duplex Pinouts
- Three-State Rx and Tx Outputs (Except ISL83084E)
- Current Limiting and Thermal Shutdown for driver Overload Protection

## Applications

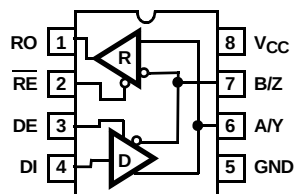
- Automated Utility Meter Reading Systems
- High Node Count Systems
- Factory Automation
- Field Bus Networks
- Security Camera Networks
- Building Environmental Control Systems
- Industrial/Process Control Networks

**TABLE 1. SUMMARY OF FEATURES**

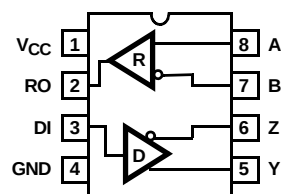
| PART NUMBER | HALF/FULL DUPLEX | DATA RATE (Mbps) | SLEW-RATE LIMITED? | HOT PLUG | #DEVICES ON BUS | Rx/Tx ENABLE? | QUIESCENT I <sub>CC</sub> (μA) | LOW POWER SHUTDOWN? | PIN COUNT |
|-------------|------------------|------------------|--------------------|----------|-----------------|---------------|--------------------------------|---------------------|-----------|
| ISL83080E   | Full             | 0.115            | Yes                | Yes      | 256             | Yes           | 530                            | Yes                 | 10, 14    |
| ISL83082E   | Half             | 0.115            | Yes                | Yes      | 256             | Yes           | 530                            | Yes                 | 8         |
| ISL83083E   | Full             | 0.5              | Yes                | Yes      | 256             | Yes           | 530                            | Yes                 | 10, 14    |
| ISL83084E   | Full             | 0.5              | Yes                | No       | 256             | No            | 530                            | No                  | 8         |
| ISL83085E   | Half             | 0.5              | Yes                | Yes      | 256             | Yes           | 530                            | Yes                 | 8         |
| ISL83086E   | Full             | 10               | No                 | No       | 256             | Yes           | 530                            | Yes                 | 10, 14    |
| ISL83088E   | Half             | 10               | No                 | No       | 256             | Yes           | 530                            | Yes                 | 8         |

## Pinouts

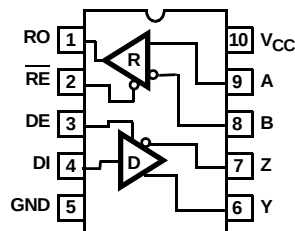
**ISL83082E, ISL83085E, ISL83088E**  
(8 LD MSOP, SOIC)  
TOP VIEW



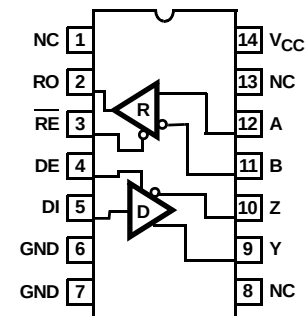
**ISL83084E**  
(8 LD SOIC)  
TOP VIEW



**ISL83080E, ISL83083E, ISL83086E**  
(10 LD MSOP)  
TOP VIEW



**ISL83080E, ISL83083E, ISL83086E**  
(14 LD SOIC)  
TOP VIEW



## Ordering Information

| PART NUMBER (Note 1)  | PART MARKING | TEMP. RANGE (°C) | PACKAGE              | PKG. DWG. # |
|-----------------------|--------------|------------------|----------------------|-------------|
| ISL83080EIB           | 83080EIB     | -40 to +85       | 14 Ld SOIC           | M14.15      |
| ISL83080EIBZ (Note 2) | 83080EIBZ    | -40 to +85       | 14 Ld SOIC (Pb-free) | M14.15      |
| ISL83080EIUZ (Note 2) | 3080Z        | -40 to +85       | 10 Ld MSOP (Pb-free) | M10.118     |
| ISL83082EIB           | 83082 EIB    | -40 to +85       | 8 Ld SOIC            | M8.15       |
| ISL83082EIBZ (Note 2) | 83082 EIBZ   | -40 to +85       | 8 Ld SOIC (Pb-free)  | M8.15       |
| ISL83082EIU           | 3082E        | -40 to +85       | 8 Ld MSOP            | M8.118      |
| ISL83082EIUZ (Note 2) | 3082Z        | -40 to +85       | 8 Ld MSOP (Pb-free)  | M8.118      |
| ISL83083EIB           | 83083EIB     | -40 to +85       | 14 Ld SOIC           | M14.15      |
| ISL83083EIBZ (Note 2) | 83083EIBZ    | -40 to +85       | 14 Ld SOIC (Pb-free) | M14.15      |
| ISL83083EIUZ (Note 2) | 3083Z        | -40 to +85       | 10 Ld MSOP (Pb-free) | M10.118     |
| ISL83084EIBZ (Note 2) | 83084 EIBZ   | -40 to +85       | 8 Ld SOIC (Pb-free)  | M8.15       |
| ISL83085EIB           | 83085 EIB    | -40 to +85       | 8 Ld SOIC            | M8.15       |
| ISL83085EIBZ (Note 2) | 83085 EIBZ   | -40 to +85       | 8 Ld SOIC (Pb-free)  | M8.15       |
| ISL83085EIU           | 3085E        | -40 to +85       | 8 Ld MSOP            | M8.118      |
| ISL83085EIUZ (Note 2) | 3085Z        | -40 to +85       | 8 Ld MSOP (Pb-free)  | M8.118      |
| ISL83086EIB           | 83086EIB     | -40 to +85       | 14 Ld SOIC           | M14.15      |
| ISL83086EIBZ (Note 2) | 83086EIBZ    | -40 to +85       | 14 Ld SOIC (Pb-free) | M14.15      |
| ISL83086EIUZ (Note 2) | 3086Z        | -40 to +85       | 10 Ld MSOP (Pb-free) | M10.118     |
| ISL83088EIB           | 83088 EIB    | -40 to +85       | 8 Ld SOIC            | M8.15       |
| ISL83088EIBZ (Note 2) | 83088 EIBZ   | -40 to +85       | 8 Ld SOIC (Pb-free)  | M8.15       |

## Ordering Information (Continued)

| PART NUMBER (Note 1)  | PART MARKING | TEMP. RANGE (°C) | PACKAGE             | PKG. DWG. # |
|-----------------------|--------------|------------------|---------------------|-------------|
| ISL83088EIU           | 3088E        | -40 to +85       | 8 Ld MSOP           | M8.118      |
| ISL83088EIUZ (Note 2) | 3088Z        | -40 to +85       | 8 Ld MSOP (Pb-free) | M8.118      |

### NOTES:

1. Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Truth Tables

| TRANSMITTING    |    |    |          |         |
|-----------------|----|----|----------|---------|
| INPUTS          |    |    | OUTPUTS  |         |
| $\overline{RE}$ | DE | DI | Z        | Y       |
| X               | 1  | 1  | 0        | 1       |
| X               | 1  | 0  | 1        | 0       |
| 0               | 0  | X  | High-Z   | High-Z  |
| 1               | 0  | X  | High-Z * | High-Z* |

NOTE: \*Shutdown Mode (See Notes 10 and 13).

| RECEIVING       |                   |                   |                        |         |
|-----------------|-------------------|-------------------|------------------------|---------|
| INPUTS          |                   |                   |                        | OUTPUT  |
| $\overline{RE}$ | DE<br>Half Duplex | DE<br>Full Duplex | A-B                    | RO      |
| 0               | 0                 | X                 | $\geq -0.05V$          | 1       |
| 0               | 0                 | X                 | $\leq -0.2V$           | 0       |
| 0               | 0                 | X                 | Inputs<br>Open/Shorted | 1       |
| 1               | 0                 | 0                 | X                      | High-Z* |
| 1               | 1                 | 1                 | X                      | High-Z  |

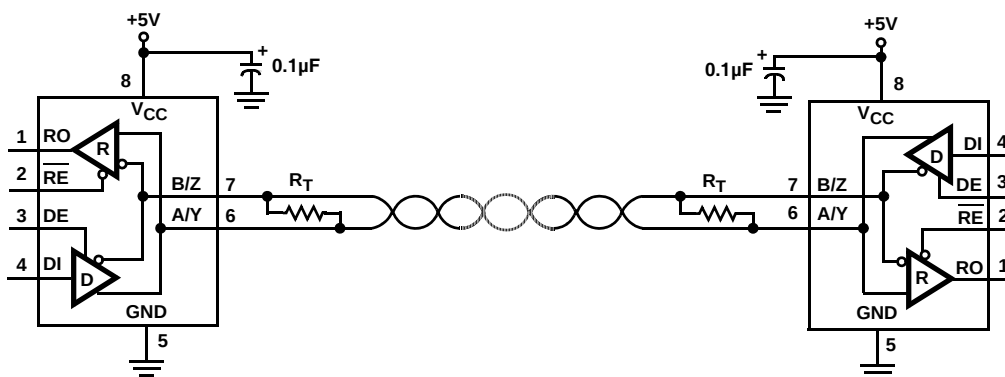
NOTE: \*Shutdown Mode (See Notes 10 and 13).

## Pin Descriptions

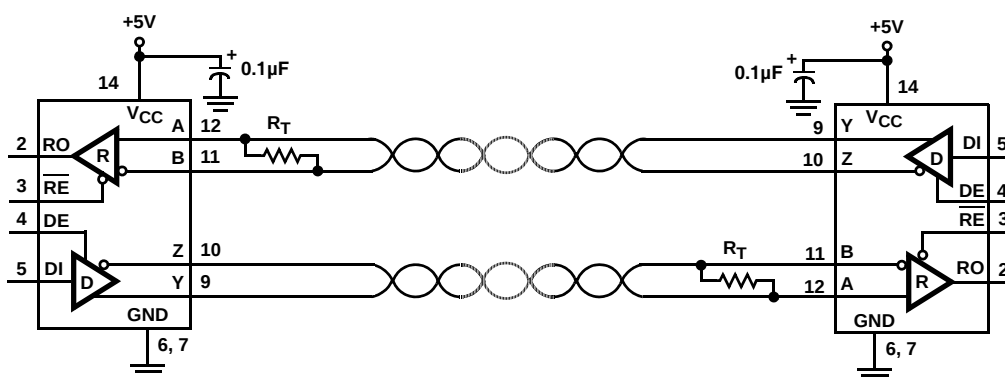
| PIN             | FUNCTION                                                                                                                                                             |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RO              | Receiver output: If A - B $\geq$ -50mV, RO is high; If A - B $\leq$ -200mV, RO is low; RO = High if A and B are unconnected (floating) or shorted.                   |
| $\overline{RE}$ | Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.                                                |
| DE              | Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low.                                          |
| DI              | Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.                                      |
| GND             | Ground connection.                                                                                                                                                   |
| A/Y             | $\pm 15kV$ HBM ESD Protected RS-485/RS-422 level, noninverting receiver input and noninverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1. |
| B/Z             | $\pm 15kV$ HBM ESD Protected RS-485/RS-422 level, Inverting receiver input and inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.       |
| A               | $\pm 15kV$ HBM ESD Protected RS-485/RS-422 level, noninverting receiver input.                                                                                       |
| B               | $\pm 15kV$ HBM ESD Protected RS-485/RS-422 level, inverting receiver input.                                                                                          |
| Y               | $\pm 15kV$ HBM ESD Protected RS-485/RS-422 level, noninverting driver output.                                                                                        |
| Z               | $\pm 15kV$ HBM ESD Protected RS-485/RS-422 level, inverting driver output.                                                                                           |
| V <sub>CC</sub> | System power supply input (4.5V to 5.5V).                                                                                                                            |
| NC              | No Connection.                                                                                                                                                       |

## Typical Operating Circuit

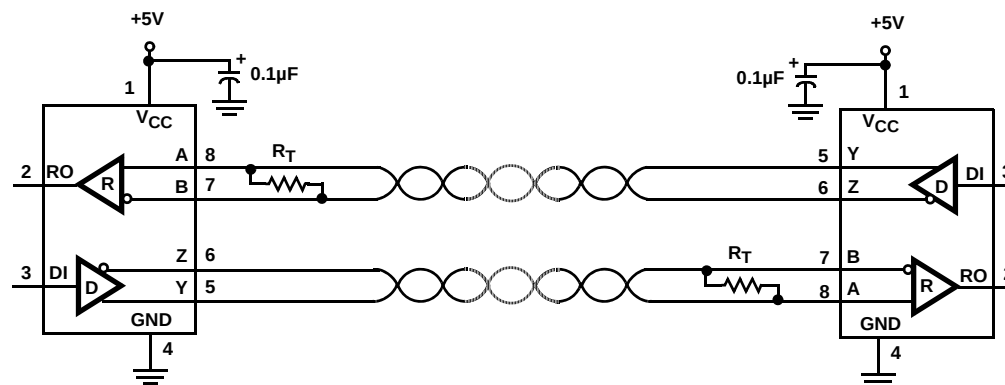
ISL83082E, ISL83085E, ISL83088E



ISL83080E, ISL83083E, ISL83086E



ISL83084E



## Absolute Maximum Ratings

|                                                    |                                   |
|----------------------------------------------------|-----------------------------------|
| V <sub>CC</sub> to Ground                          | 7V                                |
| Input Voltages                                     |                                   |
| DI, DE, RE                                         | -0.3V to (V <sub>CC</sub> + 0.3V) |
| Input/Output Voltages                              |                                   |
| A, B, Y, Z                                         | -9V to +13V                       |
| A, B, Y, Z (Transient Pulse Through 100Ω, Note 14) | ±75V                              |
| RO                                                 | -0.3V to (V <sub>CC</sub> + 0.3V) |
| Short Circuit Duration                             |                                   |
| Y, Z                                               | Continuous                        |
| ESD Rating                                         | See Specification Table           |

## Thermal Information

|                                                                                                                 |                        |
|-----------------------------------------------------------------------------------------------------------------|------------------------|
| Thermal Resistance (Typical, Note 3)                                                                            | θ <sub>JA</sub> (°C/W) |
| 8 Ld SOIC Package                                                                                               | 105                    |
| 8 Ld MSOP Package                                                                                               | 140                    |
| 10 Ld MSOP Package                                                                                              | 190                    |
| 14 Ld SOIC Package                                                                                              | 128                    |
| Maximum Junction Temperature (Plastic Package)                                                                  | +150°C                 |
| Maximum Storage Temperature Range                                                                               | -65°C to +150°C        |
| Pb-free reflow profile                                                                                          | see link below         |
| <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a> |                        |

## Operating Conditions

|                   |                |
|-------------------|----------------|
| Temperature Range | -40°C to +85°C |
|-------------------|----------------|

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

- θ<sub>JA</sub> is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

**Electrical Specifications** Test Conditions: V<sub>CC</sub> = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = +25°C (Note 5).

| PARAMETER                                                                                   | SYMBOL            | TEST CONDITIONS                                                                            |                       | TEMP<br>(°C) | MIN<br>(Note 4) | TYP  | MAX<br>(Note 4) | UNITS |
|---------------------------------------------------------------------------------------------|-------------------|--------------------------------------------------------------------------------------------|-----------------------|--------------|-----------------|------|-----------------|-------|
| DC CHARACTERISTICS                                                                          |                   |                                                                                            |                       |              |                 |      |                 |       |
| Driver Differential V <sub>OUT</sub> (no load)                                              | V <sub>OD1</sub>  |                                                                                            |                       | Full         | -               | -    | V <sub>CC</sub> | V     |
| Driver Differential V <sub>OUT</sub> (with load)                                            | V <sub>OD2</sub>  | R <sub>L</sub> = 100Ω (RS-422) (Figure 1A)                                                 |                       | Full         | 2               | 2.9  | -               | V     |
|                                                                                             |                   | R <sub>L</sub> = 54Ω (RS-485) (Figure 1A)                                                  |                       | Full         | 1.5             | 2.4  | V <sub>CC</sub> | V     |
|                                                                                             |                   | R <sub>L</sub> = 60Ω, -7V ≤ V <sub>CM</sub> ≤ 12V (Figure 1B)                              |                       | Full         | 1.5             | 2.6  | -               | V     |
| Change in Magnitude of Driver Differential V <sub>OUT</sub> for Complementary Output States | ΔV <sub>OD</sub>  | R <sub>L</sub> = 54Ω or 100Ω (Figure 1A)                                                   |                       | Full         | -               | 0.01 | 0.2             | V     |
| Driver Common-Mode V <sub>OUT</sub>                                                         | V <sub>OC</sub>   | R <sub>L</sub> = 54Ω or 100Ω (Figure 1A)                                                   |                       | Full         | -               | 2.85 | 3               | V     |
| Change in Magnitude of Driver Common-Mode V <sub>OUT</sub> for Complementary Output States  | ΔV <sub>OC</sub>  | R <sub>L</sub> = 54Ω or 100Ω (Figure 1A)                                                   |                       | Full         | -               | 0.01 | 0.1             | V     |
| Logic Input High Voltage                                                                    | V <sub>IH</sub>   | DE, DI, $\overline{\text{RE}}$                                                             |                       | Full         | 2               | -    | -               | V     |
| Logic Input Low Voltage                                                                     | V <sub>IL</sub>   | DE, DI, $\overline{\text{RE}}$                                                             |                       | Full         | -               | -    | 0.8             | V     |
| DI Input Hysteresis Voltage                                                                 | V <sub>HYS</sub>  |                                                                                            |                       | 25           | -               | 100  | -               | mV    |
| Logic Input Current                                                                         | I <sub>IN1</sub>  | DE, DI, $\overline{\text{RE}}$                                                             |                       | Full         | -2              | -    | 2               | μA    |
| Input Current (A, B)                                                                        | I <sub>IN2</sub>  | DE = 0V, V <sub>CC</sub> = 0V or 5.5V                                                      | V <sub>IN</sub> = 12V | Full         | -               | 70   | 125             | μA    |
|                                                                                             |                   |                                                                                            | V <sub>IN</sub> = -7V | Full         | -75             | 55   | -               | μA    |
| Output Leakage Current (Y, Z) (Full Duplex Versions Only)                                   | I <sub>IN3</sub>  | $\overline{\text{RE}}$ = 0V, DE = 0V, V <sub>CC</sub> = 0V or 5.5V (Note 13)               | V <sub>IN</sub> = 12V | Full         | -               | 7    | 125             | μA    |
|                                                                                             |                   |                                                                                            | V <sub>IN</sub> = -7V | Full         | -75             | 11   | -               | μA    |
| Output Leakage Current (Y, Z) in Shutdown Mode (Full Duplex)                                | I <sub>IN3</sub>  | $\overline{\text{RE}}$ = V <sub>CC</sub> , DE = 0V, V <sub>CC</sub> = 0V or 5.5V (Note 13) | V <sub>IN</sub> = 12V | Full         | -               | 0    | 20              | μA    |
|                                                                                             |                   |                                                                                            | V <sub>IN</sub> = -7V | Full         | -20             | 9    | -               | μA    |
| Driver Short-Circuit Current, V <sub>O</sub> = High or Low                                  | I <sub>OSD1</sub> | DE = V <sub>CC</sub> , -7V ≤ V <sub>Y</sub> or V <sub>Z</sub> ≤ 12V (Note 7)               |                       | Full         | -               | -    | ±250            | mA    |

**Electrical Specifications** Test Conditions:  $V_{CC} = 4.5V$  to  $5.5V$ ; Unless Otherwise Specified. Typicals are at  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$  (Note 5). **(Continued)**

| PARAMETER                                                                            | SYMBOL                              | TEST CONDITIONS                                                                                                                              | TEMP<br>(°C) | MIN<br>(Note 4)     | TYP    | MAX<br>(Note 4) | UNITS |
|--------------------------------------------------------------------------------------|-------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|--------------|---------------------|--------|-----------------|-------|
| Receiver Differential Threshold Voltage                                              | V <sub>TH</sub>                     | -7V ≤ V <sub>CM</sub> ≤ 12V                                                                                                                  | Full         | -200                | -90    | -50             | mV    |
| Receiver Input Hysteresis                                                            | ΔV <sub>TH</sub>                    | V <sub>CM</sub> = 0V                                                                                                                         | 25           | -                   | 20     | -               | mV    |
| Receiver Output High Voltage                                                         | V <sub>OH</sub>                     | I <sub>O</sub> = -4mA, V <sub>ID</sub> = -50mV                                                                                               | Full         | V <sub>CC</sub> - 1 | 4.6    | -               | V     |
| Receiver Output Low Voltage                                                          | V <sub>OL</sub>                     | I <sub>O</sub> = -4mA, V <sub>ID</sub> = -200mV                                                                                              | Full         | -                   | 0.2    | 0.4             | V     |
| Three-State (high impedance) Receiver Output Current                                 | I <sub>OZR</sub>                    | 0.4V ≤ V <sub>O</sub> ≤ 2.4V (Note 13)                                                                                                       | Full         | -1                  | 0.03   | 1               | μA    |
| Receiver Input Resistance                                                            | R <sub>IN</sub>                     | -7V ≤ V <sub>CM</sub> ≤ 12V                                                                                                                  | Full         | 96                  | 160    | -               | kΩ    |
| Receiver Short-Circuit Current                                                       | I <sub>OSR</sub>                    | 0V ≤ V <sub>O</sub> ≤ V <sub>CC</sub>                                                                                                        | Full         | ±7                  | -      | ±85             | mA    |
| SUPPLY CURRENT                                                                       |                                     |                                                                                                                                              |              |                     |        |                 |       |
| No-Load Supply Current (Note 6)                                                      | I <sub>CC</sub>                     | Half Duplex Versions, DE = V <sub>CC</sub> , $\overline{RE}$ = X, DI = 0V or V <sub>CC</sub>                                                 | Full         | -                   | 560    | 700             | μA    |
|                                                                                      |                                     | All Versions, DE = 0V, $\overline{RE}$ = 0V, or Full Duplex Versions, DE = V <sub>CC</sub> , $\overline{RE}$ = X. DI = 0V or V <sub>CC</sub> | Full         | -                   | 530    | 650             | μA    |
| Shutdown Supply Current                                                              | I <sub>SHDN</sub>                   | DE = 0V, $\overline{RE}$ = V <sub>CC</sub> , DI = 0V or V <sub>CC</sub> (Note 13)                                                            | Full         | -                   | 0.07   | 2               | μA    |
| ESD PERFORMANCE                                                                      |                                     |                                                                                                                                              |              |                     |        |                 |       |
| RS-485 Pins (A, Y, B, Z)                                                             |                                     | Human Body Model (HBM), Pin to GND                                                                                                           | 25           | -                   | ±15    | -               | kV    |
| All Other Pins                                                                       |                                     | HBM, per MIL-STD-883 Method 3015                                                                                                             | 25           | -                   | ±7     | -               | kV    |
|                                                                                      |                                     | Machine Model                                                                                                                                | 25           | -                   | > ±250 | -               | V     |
| DRIVER SWITCHING CHARACTERISTICS (115kbps Versions; ISL83080E, ISL83082E)            |                                     |                                                                                                                                              |              |                     |        |                 |       |
| Driver Differential Output Delay                                                     | t <sub>PLH</sub> , t <sub>PHL</sub> | R <sub>DIFF</sub> = 54Ω, C <sub>L</sub> = 100pF (Figure 2)                                                                                   | Full         | 500                 | 780    | 1300            | ns    |
| Driver Differential Output Skew                                                      | t <sub>SKEW</sub>                   | R <sub>DIFF</sub> = 54Ω, C <sub>L</sub> = 100pF (Figure 2)                                                                                   | Full         | -                   | 40     | 100             | ns    |
| Driver Differential Rise or Fall Time                                                | t <sub>R</sub> , t <sub>F</sub>     | R <sub>DIFF</sub> = 54Ω, C <sub>L</sub> = 100pF (Figure 2)                                                                                   | Full         | 667                 | 1000   | 1500            | ns    |
| Maximum Data Rate                                                                    | f <sub>MAX</sub>                    | C <sub>D</sub> = 820pF (Figure 4) (Note 15)                                                                                                  | Full         | 115                 | 666    | -               | kbps  |
| Driver Enable to Output High                                                         | t <sub>ZH</sub>                     | R <sub>L</sub> = 500Ω, C <sub>L</sub> = 100pF, SW = GND (Figure 3), (Note 8)                                                                 | Full         | -                   | 278    | 1500            | ns    |
| Driver Enable to Output Low                                                          | t <sub>ZL</sub>                     | R <sub>L</sub> = 500Ω, C <sub>L</sub> = 100pF, SW = V <sub>CC</sub> (Figure 3) (Note 8)                                                      | Full         | -                   | 35     | 1500            | ns    |
| Driver Disable from Output Low                                                       | t <sub>LZ</sub>                     | R <sub>L</sub> = 500Ω, C <sub>L</sub> = 15pF, SW = V <sub>CC</sub> (Figure 3)                                                                | Full         | -                   | 67     | 100             | ns    |
| Driver Disable from Output High                                                      | t <sub>HZ</sub>                     | R <sub>L</sub> = 500Ω, C <sub>L</sub> = 15pF, SW = GND (Figure 3)                                                                            | Full         | -                   | 38     | 100             | ns    |
| Time to Shutdown                                                                     | t <sub>SHDN</sub>                   | (Note 10)                                                                                                                                    | Full         | 60                  | 160    | 600             | ns    |
| Driver Enable from Shutdown to Output High                                           | t <sub>ZH(SHDN)</sub>               | R <sub>L</sub> = 500Ω, C <sub>L</sub> = 100pF, SW = GND (Figure 3) (Notes 10, 11)                                                            | Full         | -                   | 400    | 2000            | ns    |
| Driver Enable from Shutdown to Output Low                                            | t <sub>ZL(SHDN)</sub>               | R <sub>L</sub> = 500Ω, C <sub>L</sub> = 100pF, SW = V <sub>CC</sub> (Figure 3) (Notes 10, 11)                                                | Full         | -                   | 155    | 2000            | ns    |
| DRIVER SWITCHING CHARACTERISTICS (500kbps Versions; ISL83083E, ISL83084E, ISL83085E) |                                     |                                                                                                                                              |              |                     |        |                 |       |
| Driver Differential Output Delay                                                     | t <sub>PLH</sub> , t <sub>PHL</sub> | R <sub>DIFF</sub> = 54Ω, C <sub>L</sub> = 100pF (Figure 2)                                                                                   | Full         | 250                 | 360    | 1000            | ns    |
| Driver Differential Output Skew                                                      | t <sub>SKEW</sub>                   | R <sub>DIFF</sub> = 54Ω, C <sub>L</sub> = 100pF (Figure 2)                                                                                   | Full         | -                   | 20     | 100             | ns    |
| Driver Differential Rise or Fall Time                                                | t <sub>R</sub> , t <sub>F</sub>     | R <sub>DIFF</sub> = 54Ω, C <sub>L</sub> = 100pF (Figure 2)                                                                                   | Full         | 200                 | 475    | 750             | ns    |

**Electrical Specifications** Test Conditions:  $V_{CC} = 4.5V$  to  $5.5V$ ; Unless Otherwise Specified. Typicals are at  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$  (Note 5). **(Continued)**

| PARAMETER                                                                                          | SYMBOL                | TEST CONDITIONS                                                                  | TEMP<br>(°C) | MIN<br>(Note 4) | TYP  | MAX<br>(Note 4) | UNITS |
|----------------------------------------------------------------------------------------------------|-----------------------|----------------------------------------------------------------------------------|--------------|-----------------|------|-----------------|-------|
| Maximum Data Rate                                                                                  | $f_{MAX}$             | $C_D = 820pF$ (Figure 4) (Note 15)                                               | Full         | 500             | 1000 | -               | kbps  |
| Driver Enable to Output High                                                                       | $t_{ZH}$              | $R_L = 500\Omega$ , $C_L = 100pF$ , SW = GND (Figure 3), (Notes 8, 13)           | Full         | -               | 137  | 1000            | ns    |
| Driver Enable to Output Low                                                                        | $t_{ZL}$              | $R_L = 500\Omega$ , $C_L = 100pF$ , SW = $V_{CC}$ (Figure 3), (Notes 8, 13)      | Full         | -               | 35   | 1000            | ns    |
| Driver Disable from Output Low                                                                     | $t_{LZ}$              | $R_L = 500\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 3), (Note 13)           | Full         | -               | 65   | 100             | ns    |
| Driver Disable from Output High                                                                    | $t_{HZ}$              | $R_L = 500\Omega$ , $C_L = 15pF$ , SW = GND (Figure 3), (Note 13)                | Full         | -               | 38   | 100             | ns    |
| Time to Shutdown                                                                                   | $t_{SHDN}$            | (Note 10)                                                                        | Full         | 60              | 160  | 600             | ns    |
| Driver Enable from Shutdown to Output High                                                         | $t_{ZH}(SHDN)$        | $R_L = 500\Omega$ , $C_L = 100pF$ , SW = GND (Figure 3), (Notes 10, 11, 13)      | Full         | -               | 260  | 1500            | ns    |
| Driver Enable from Shutdown to Output Low                                                          | $t_{ZL}(SHDN)$        | $R_L = 500\Omega$ , $C_L = 100pF$ , SW = $V_{CC}$ (Figure 3), (Notes 10, 11, 13) | Full         | -               | 155  | 1500            | ns    |
| <b>DRIVER SWITCHING CHARACTERISTICS (10Mbps Versions; ISL83086E, ISL83088E)</b>                    |                       |                                                                                  |              |                 |      |                 |       |
| Driver Differential Output Delay                                                                   | $t_{PLH}$ , $t_{PHL}$ | $R_{DIFF} = 54\Omega$ , $C_L = 100pF$ (Figure 2)                                 | Full         | -               | 20   | 60              | ns    |
| Driver Differential Output Skew                                                                    | $t_{SKEW}$            | $R_{DIFF} = 54\Omega$ , $C_L = 100pF$ (Figure 2)                                 | Full         | -               | 1    | 10              | ns    |
| Driver Differential Rise or Fall Time                                                              | $t_R$ , $t_F$         | $R_{DIFF} = 54\Omega$ , $C_L = 100pF$ (Figure 2)                                 | Full         | -               | 13   | 25              | ns    |
| Maximum Data Rate                                                                                  | $f_{MAX}$             | $C_D = 470pF$ (Figure 4) (Note 15)                                               | Full         | 10              | 15   | -               | Mbps  |
| Driver Enable to Output High                                                                       | $t_{ZH}$              | $R_L = 500\Omega$ , $C_L = 100pF$ , SW = GND (Figure 3), (Note 8)                | Full         | -               | 35   | 150             | ns    |
| Driver Enable to Output Low                                                                        | $t_{ZL}$              | $R_L = 500\Omega$ , $C_L = 100pF$ , SW = $V_{CC}$ (Figure 3), (Note 8)           | Full         | -               | 30   | 150             | ns    |
| Driver Disable from Output Low                                                                     | $t_{LZ}$              | $R_L = 500\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 3)                      | Full         | -               | 66   | 100             | ns    |
| Driver Disable from Output High                                                                    | $t_{HZ}$              | $R_L = 500\Omega$ , $C_L = 15pF$ , SW = GND (Figure 3)                           | Full         | -               | 38   | 100             | ns    |
| Time to Shutdown                                                                                   | $t_{SHDN}$            | (Note 10)                                                                        | Full         | 60              | 160  | 600             | ns    |
| Driver Enable from Shutdown to Output High                                                         | $t_{ZH}(SHDN)$        | $R_L = 500\Omega$ , $C_L = 100pF$ , SW = GND (Figure 3), (Notes 10, 11)          | Full         | -               | 115  | 250             | ns    |
| Driver Enable from Shutdown to Output Low                                                          | $t_{ZL}(SHDN)$        | $R_L = 500\Omega$ , $C_L = 100pF$ , SW = $V_{CC}$ (Figure 3), (Notes 10, 11)     | Full         | -               | 84   | 250             | ns    |
| <b>RECEIVER SWITCHING CHARACTERISTICS (115kbps and 500kbps Versions; ISL83080E THRU ISL83085E)</b> |                       |                                                                                  |              |                 |      |                 |       |
| Maximum Data Rate                                                                                  | $f_{MAX}$             | (Figure 5) (Note 15)                                                             | Full         | 0.5             | 10   | -               | Mbps  |
| Receiver Input to Output Delay                                                                     | $t_{PLH}$ , $t_{PHL}$ | (Figure 5)                                                                       | Full         | -               | 100  | 150             | ns    |
| Receiver Skew   $t_{PLH} - t_{PHL}$                                                                | $t_{SKD}$             | (Figure 5)                                                                       | Full         | -               | 7    | 10              | ns    |
| Receiver Enable to Output Low                                                                      | $t_{ZL}$              | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 6), (Notes 9, 13)        | Full         | -               | 10   | 50              | ns    |
| Receiver Enable to Output High                                                                     | $t_{ZH}$              | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = GND (Figure 6), (Notes 9, 13)             | Full         | -               | 10   | 50              | ns    |
| Receiver Disable from Output Low                                                                   | $t_{LZ}$              | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 6), (Note 13)            | Full         | -               | 10   | 50              | ns    |
| Receiver Disable from Output High                                                                  | $t_{HZ}$              | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = GND (Figure 6), (Note 13)                 | Full         | -               | 10   | 50              | ns    |

**Electrical Specifications** Test Conditions:  $V_{CC} = 4.5V$  to  $5.5V$ ; Unless Otherwise Specified. Typical values are at  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$  (Note 5). **(Continued)**

| PARAMETER                                                                         | SYMBOL                | TEST CONDITIONS                                                                | TEMP<br>(°C) | MIN<br>(Note 4) | TYP | MAX<br>(Note 4) | UNITS |
|-----------------------------------------------------------------------------------|-----------------------|--------------------------------------------------------------------------------|--------------|-----------------|-----|-----------------|-------|
| Time to Shutdown                                                                  | $t_{SHDN}$            | (Notes 10, 13)                                                                 | Full         | 60              | 160 | 600             | ns    |
| Receiver Enable from Shutdown to Output High                                      | $t_{ZH(SHDN)}$        | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = GND (Figure 6), (Notes 10, 12, 13)      | Full         | -               | 150 | 2000            | ns    |
| Receiver Enable from Shutdown to Output Low                                       | $t_{ZL(SHDN)}$        | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 6), (Notes 10, 12, 13) | Full         | -               | 150 | 2000            | ns    |
| <b>RECEIVER SWITCHING CHARACTERISTICS (10Mbps Versions; ISL83086E, ISL83088E)</b> |                       |                                                                                |              |                 |     |                 |       |
| Maximum Data Rate                                                                 | $f_{MAX}$             | (Figure 5) (Note 15)                                                           | Full         | 10              | 15  | -               | Mbps  |
| Receiver Input to Output Delay                                                    | $t_{PLH}$ , $t_{PHL}$ | (Figure 5)                                                                     | Full         | -               | 70  | 125             | ns    |
| Receiver Skew   $t_{PLH} - t_{PHL}$                                               | $t_{SKD}$             | (Figure 5)                                                                     | Full         | -               | 0   | 10              | ns    |
| Receiver Enable to Output Low                                                     | $t_{ZL}$              | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 6) (Note 9)            | Full         | -               | 10  | 30              | ns    |
| Receiver Enable to Output High                                                    | $t_{ZH}$              | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = GND (Figure 6) (Note 9)                 | Full         | -               | 10  | 30              | ns    |
| Receiver Disable from Output Low                                                  | $t_{LZ}$              | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 6)                     | Full         | -               | 10  | 30              | ns    |
| Receiver Disable from Output High                                                 | $t_{HZ}$              | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = GND (Figure 6)                          | Full         | -               | 10  | 30              | ns    |
| Time to Shutdown                                                                  | $t_{SHDN}$            | (Note 10)                                                                      | Full         | 60              | 160 | 600             | ns    |
| Receiver Enable from Shutdown to Output High                                      | $t_{ZH(SHDN)}$        | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = GND (Figure 6) (Notes 10, 12)           | Full         | -               | 150 | 2000            | ns    |
| Receiver Enable from Shutdown to Output Low                                       | $t_{ZL(SHDN)}$        | $R_L = 1k\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 6) (Notes 10, 12)      | Full         | -               | 150 | 2000            | ns    |

**NOTES:**

- Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ C$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.
- All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
- Supply current specification is valid for loaded drivers when  $DE = 0V$ .
- Applies to peak current. See "Typical Performance Curves" beginning on page 12 for more information.
- Keep  $\overline{RE} = 0$  to prevent the device from entering SHDN.
- The  $\overline{RE}$  signal high time must be short enough (typically  $<100ns$ ) to prevent the device from entering SHDN.
- Transceivers are put into shutdown by bringing  $\overline{RE}$  high and  $DE$  low. If the inputs are in this state for less than  $60ns$ , the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least  $600ns$ , the parts are guaranteed to have entered shutdown. See "Low Power Shutdown Mode" on page 12.
- Keep  $\overline{RE} = V_{CC}$ , and set the  $DE$  signal low time  $>600ns$  to ensure that the device enters SHDN.
- Set the  $\overline{RE}$  signal high time  $>600ns$  to ensure that the device enters SHDN.
- Does not apply to the ISL83084E.
- Tested according to TIA/EIA-485-A, section 4.2.6 ( $\pm 75V$  for  $15\mu s$  at a 1% duty cycle).
- Limits established by characterization and are not production tested.

## Test Circuits and Waveforms

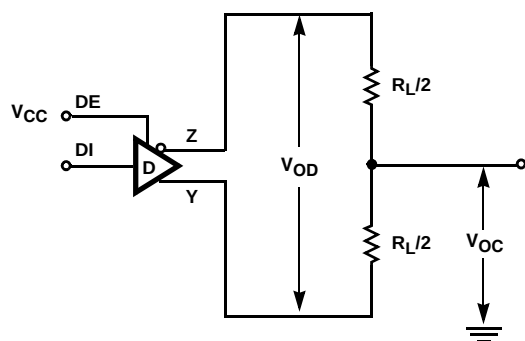


FIGURE 1A.  $V_{OD}$  AND  $V_{OC}$

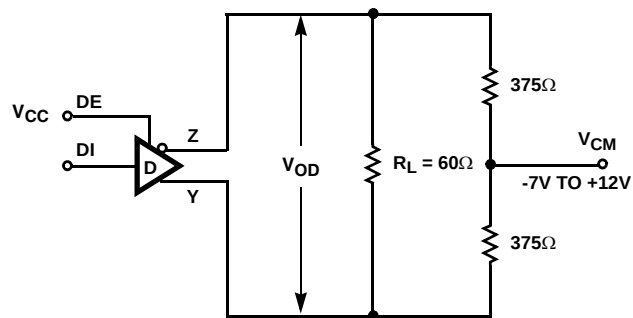


FIGURE 1B.  $V_{OD}$  WITH COMMON MODE LOAD

FIGURE 1. DC DRIVER TEST CIRCUITS

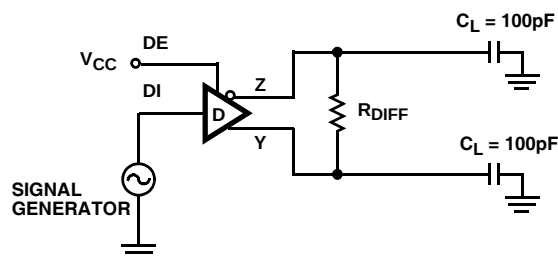


FIGURE 2A. TEST CIRCUIT

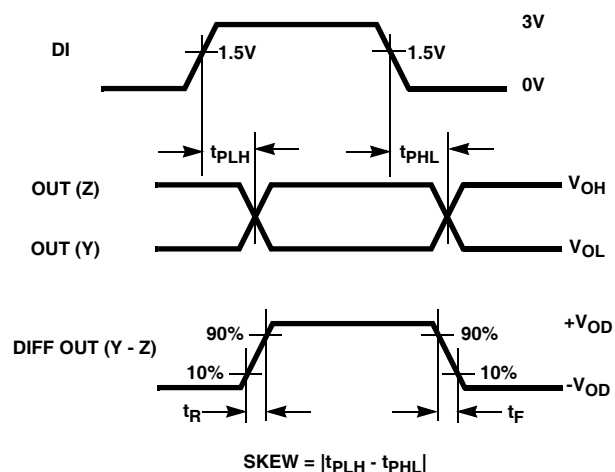
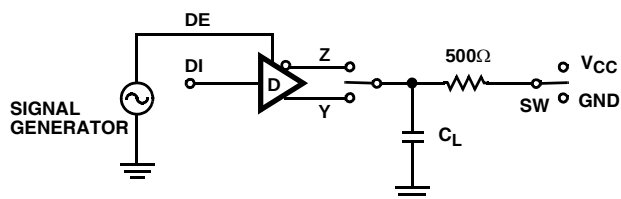


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



| PARAMETER      | OUTPUT | $\overline{RE}$ | DI  | SW       | $C_L$ (pF) |
|----------------|--------|-----------------|-----|----------|------------|
| $t_{HZ}$       | Y/Z    | X               | 1/0 | GND      | 15         |
| $t_{LZ}$       | Y/Z    | X               | 0/1 | $V_{CC}$ | 15         |
| $t_{ZH}$       | Y/Z    | 0 (Note 8)      | 1/0 | GND      | 100        |
| $t_{ZL}$       | Y/Z    | 0 (Note 8)      | 0/1 | $V_{CC}$ | 100        |
| $t_{ZH(SHDN)}$ | Y/Z    | 1 (Note 11)     | 1/0 | GND      | 100        |
| $t_{ZL(SHDN)}$ | Y/Z    | 1 (Note 11)     | 0/1 | $V_{CC}$ | 100        |

FIGURE 3A. TEST CIRCUIT

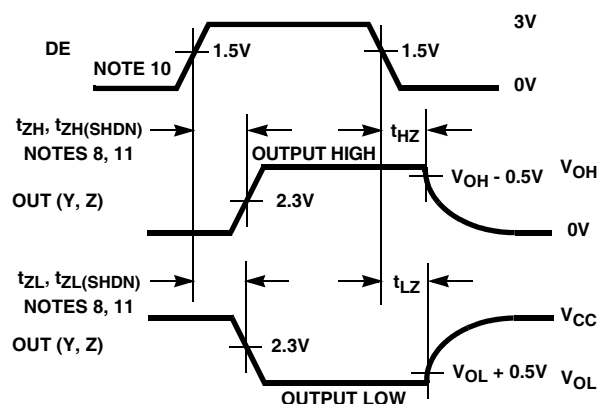


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES (DOES NOT APPLY TO THE ISL83084E)

## Test Circuits and Waveforms (Continued)

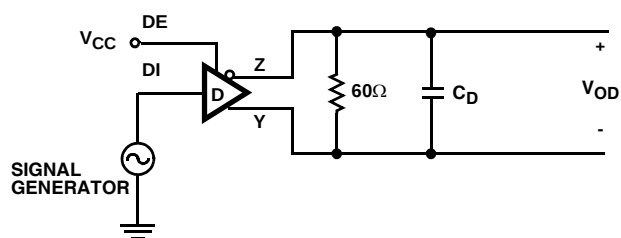


FIGURE 4A. TEST CIRCUIT

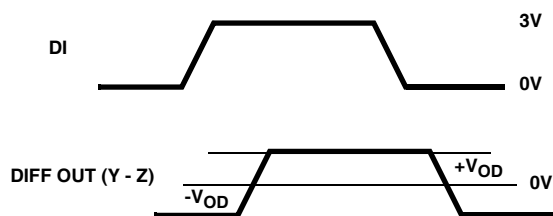


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. DRIVER DATA RATE

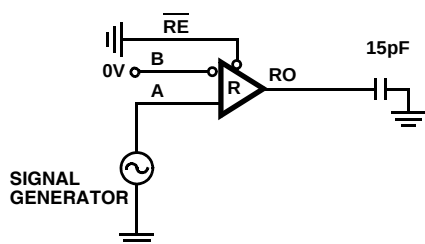


FIGURE 5A. TEST CIRCUIT

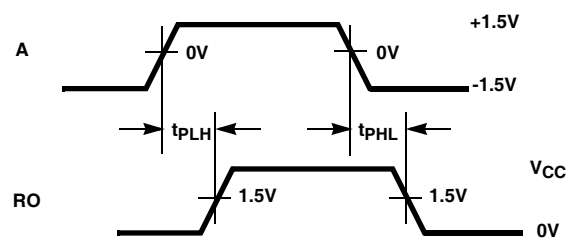


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER PROPAGATION DELAY AND DATA RATE

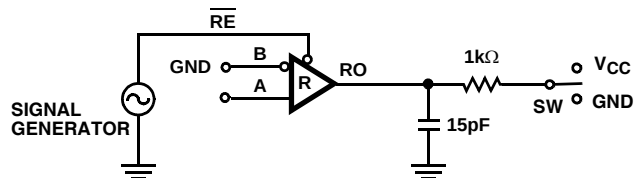


FIGURE 6A. TEST CIRCUIT

| PARAMETER                | DE | A     | SW       |
|--------------------------|----|-------|----------|
| $t_{HZ}$                 | 0  | +1.5V | GND      |
| $t_{LZ}$                 | 0  | -1.5V | $V_{CC}$ |
| $t_{ZH}$ (Note 9)        | 0  | +1.5V | GND      |
| $t_{ZL}$ (Note 9)        | 0  | -1.5V | $V_{CC}$ |
| $t_{ZH}(SHDN)$ (Note 12) | 0  | +1.5V | GND      |
| $t_{ZL}(SHDN)$ (Note 12) | 0  | -1.5V | $V_{CC}$ |

FIGURE 6. RECEIVER ENABLE AND DISABLE TIMES (DOES NOT APPLY TO THE ISL83084E)

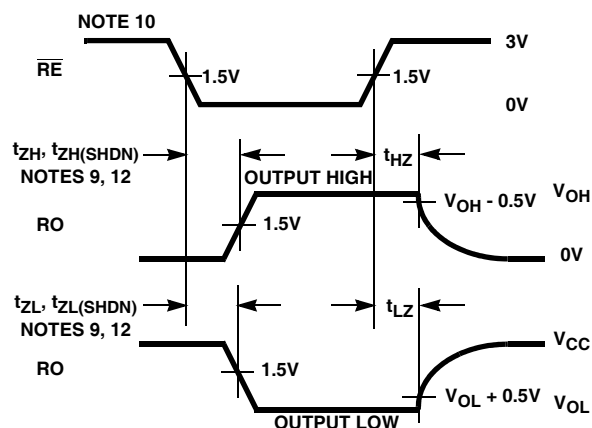


FIGURE 6B. MEASUREMENT POINTS

## Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only

one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended common mode range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

### Receiver Features

These devices utilize a differential input receiver for maximum noise immunity and common mode rejection. Input sensitivity is  $\pm 200\text{mV}$ , as required by the RS-422 and RS-485 specifications.

Receiver input resistance of  $96\text{k}\Omega$  surpasses the RS-422 specification of  $4\text{k}\Omega$ , and is eight times the RS-485 "Unit Load (UL)" requirement of  $12\text{k}\Omega$  minimum. Thus, these products are known as "one-eighth UL" transceivers, and there can be up to 256 of these devices on a network while still complying with the RS-485 loading specification.

Receiver inputs function with common mode voltages as great as  $\pm 7\text{V}$  outside the power supplies (i.e., +12V and -7V), making them ideal for long networks where induced voltages are a realistic concern.

All the receivers include a "full fail-safe" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating) or shorted.

Receivers easily meet the data rates supported by the corresponding driver, and all receiver outputs are three-statable via the active low  $\overline{\text{RE}}$  input (except for the ISL83084E).

### Driver Features

The RS-485/RS-422 driver is a differential output device that delivers at least 1.5V across a  $54\Omega$  load (RS-485), and at least 2V across a  $100\Omega$  load (RS-422). The drivers feature low propagation delay skew to maximize bit width, and to minimize EMI.

All drivers are three-statable via the active high DE input (except for the ISL83084E).

The 115kbps and 500kbps driver outputs are slew rate limited to minimize EMI, and to minimize reflections in unterminated or improperly terminated networks. Outputs of the ISL83086E, ISL83088E drivers are not limited, so faster output transition times allow data rates of at least 10Mbps.

### Hot Plug Function

When a piece of equipment powers up, there is a period of time where the processor or ASIC driving the RS-485 control lines (DE,  $\overline{\text{RE}}$ ) is unable to ensure that the RS-485 Tx and Rx outputs are kept disabled. If the equipment is connected to the bus, a driver activating prematurely during power-up may crash the bus. To avoid this scenario, the ISL83080, ISL83082, ISL83083, ISL83085 versions incorporate a "Hot Plug" function. Circuitry monitoring  $V_{\text{CC}}$  ensures that, during

power-up and power-down, the Tx and Rx outputs remain disabled, regardless of the state of DE and  $\overline{\text{RE}}$ , if  $V_{\text{CC}}$  is less than  $\sim 3.4\text{V}$ . This gives the processor/ASIC a chance to stabilize and drive the RS-485 control lines to the proper states.

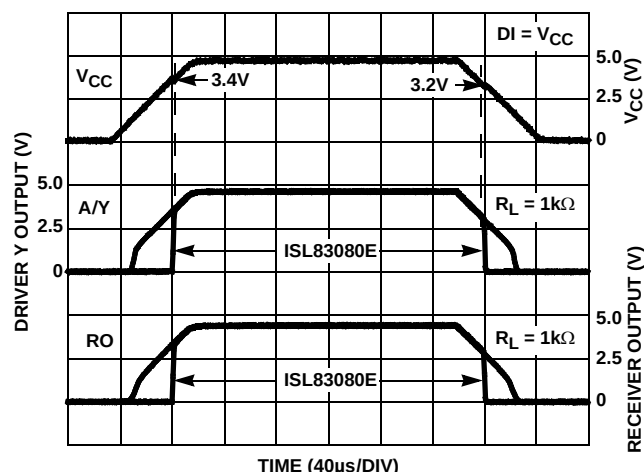


FIGURE 7. HOT PLUG PERFORMANCE (ISL83080E) vs DEVICE WITHOUT HOT PLUG CIRCUITRY (ISL83086E)

### ESD Protection

All pins on these devices include class 3 Human Body Model (HBM) ESD protection structures, but the RS-485 pins (driver outputs and receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of  $\pm 15\text{kV}$  HBM. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and without degrading the RS-485 common mode range of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (e.g., transient suppression diodes), and the associated, undesirable capacitive load they present.

### Data Rate, Cables, and Terminations

RS-485/RS-422 are intended for network lengths up to 4000', but the maximum system data rate decreases as the transmission length increases. Devices operating at 10Mbps are limited to lengths less than 100', while the 115kbps versions can operate at full data rates with lengths of several 1000'.

Twisted pair is the cable of choice for RS-485/RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative (when using the 10Mbps devices) to minimize reflections. Short networks using the

115kbps versions need not be terminated, but, terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

### Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst case bus contentions undamaged. These devices meet this requirement via driver output short circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate short circuit current limiting circuitry which ensures that the output current never exceeds the RS-485 specification, even at the common mode voltage range extremes. Additionally, these devices utilize a foldback circuit which reduces the short circuit current, and thus the power dissipation, whenever the contending voltage exceeds either supply.

In the event of a major short circuit condition, devices also include a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about +15°C. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

### Low Power Shutdown Mode

These CMOS transceivers all use a fraction of the power required by their bipolar counterparts, but they also include a shutdown feature (except for the ISL83084E) that reduces the already low quiescent  $I_{CC}$  to a 70nA trickle. These devices enter shutdown whenever the receiver and driver are **simultaneously** disabled ( $\overline{RE} = V_{CC}$  and  $\overline{DE} = GND$ ) for a period of at least 600ns. Disabling both the driver and the receiver for less than 60ns guarantees that the transceiver will not enter shutdown.

Note that receiver and driver enable times increase when the transceiver enables from shutdown. Refer to Notes 8 thru 12, at the end of the "Electrical Specification Table" on page 8, for more information.

### Typical Performance Curves $V_{CC} = 5V$ , $T_A = +25^\circ C$ ; Unless Otherwise Specified

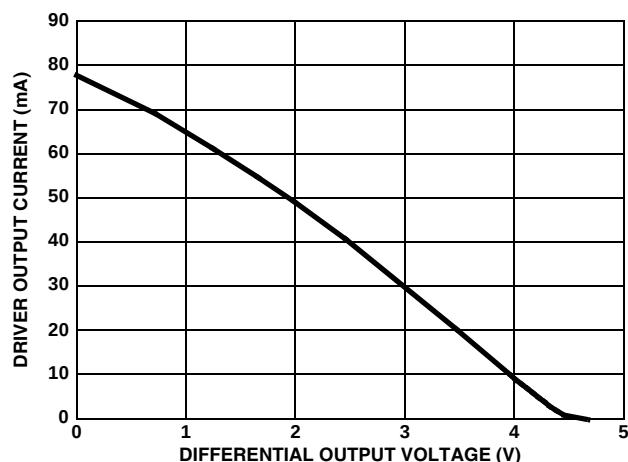


FIGURE 8. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

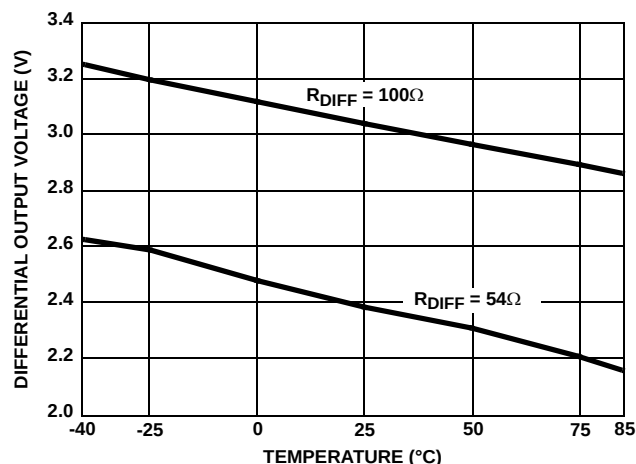


FIGURE 9. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

**Typical Performance Curves**  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$ ; Unless Otherwise Specified (Continued)

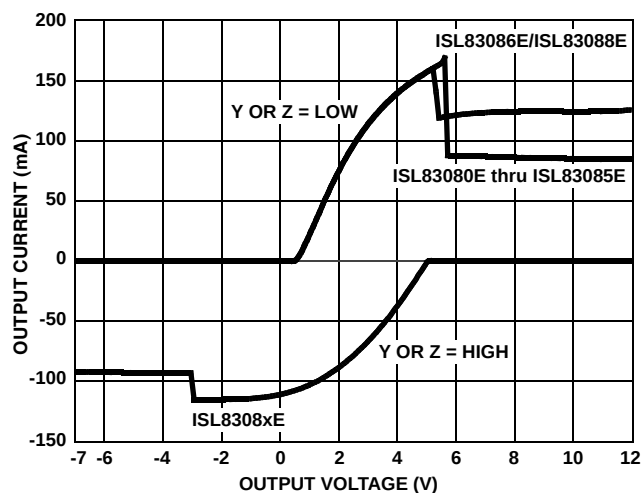


FIGURE 10. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

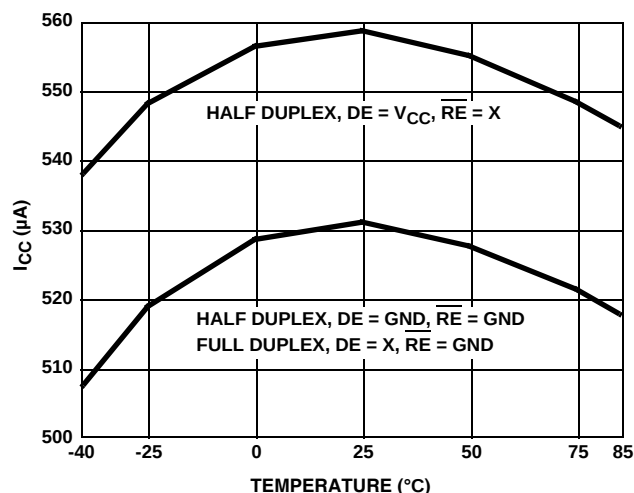


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE

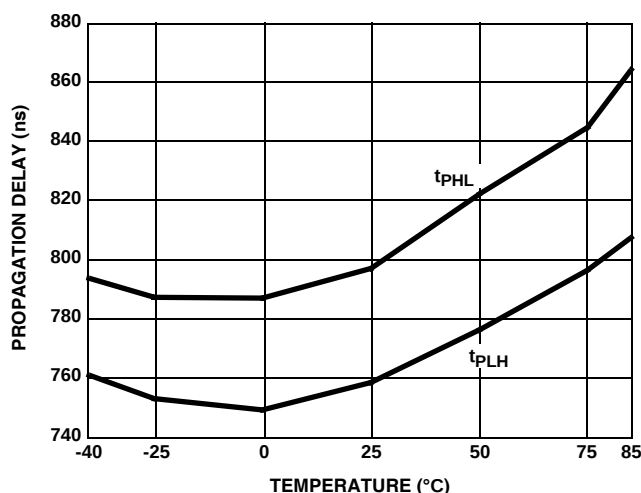


FIGURE 12. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL83080E, ISL83082E)

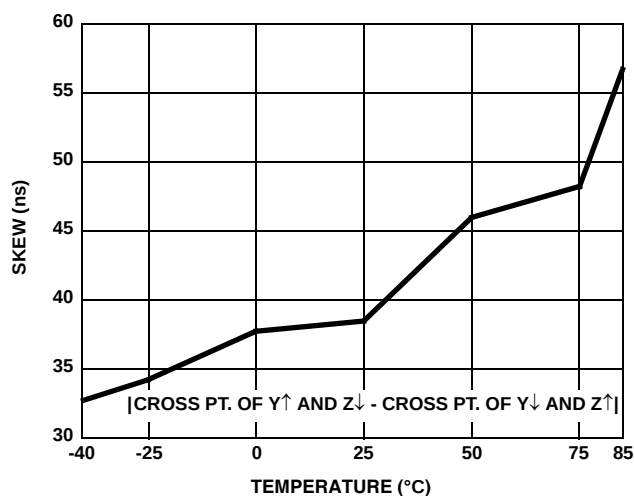


FIGURE 13. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL83080E, ISL83082E)

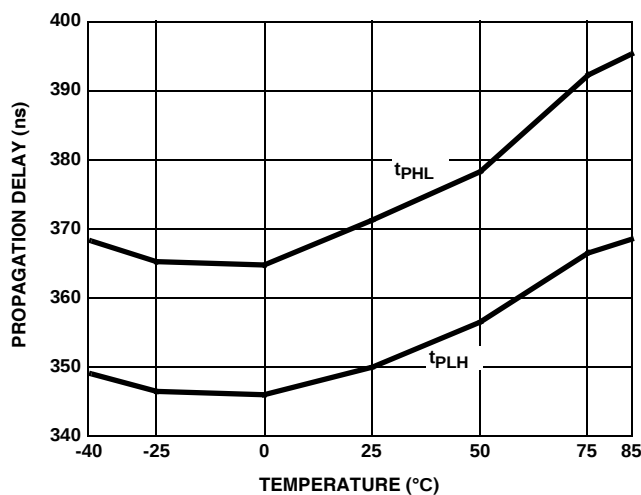


FIGURE 14. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL83083E, ISL83084E, ISL83085E)

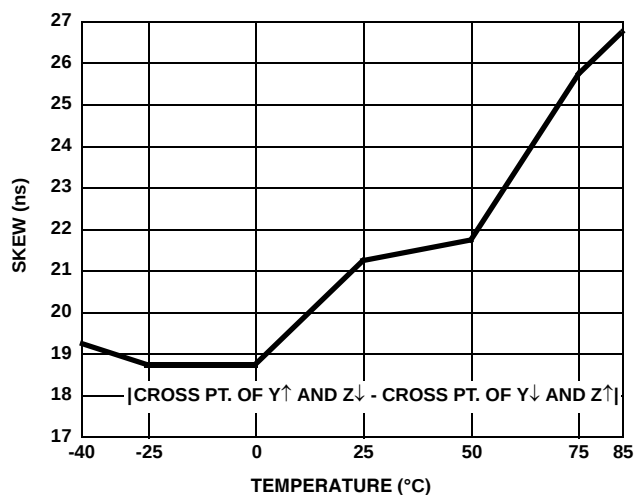


FIGURE 15. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL83083E, ISL83084E, ISL83085E)

**Typical Performance Curves**  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$ ; Unless Otherwise Specified (Continued)

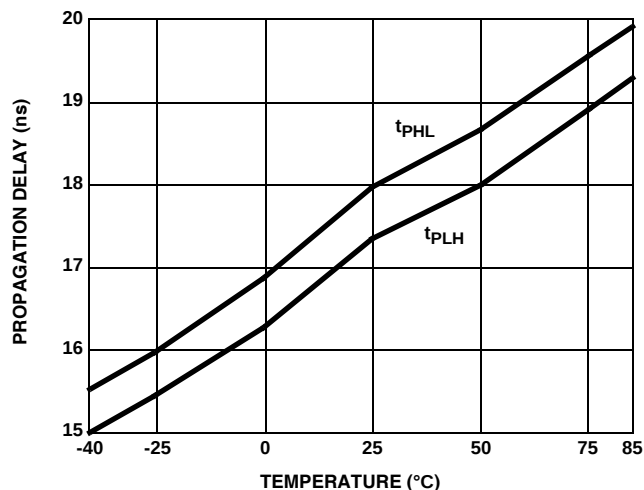


FIGURE 16. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL83086E, ISL83088E)

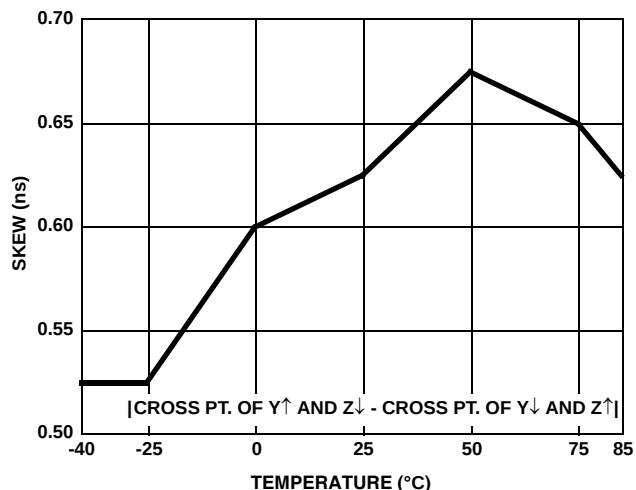


FIGURE 17. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL83086E, ISL83088E)

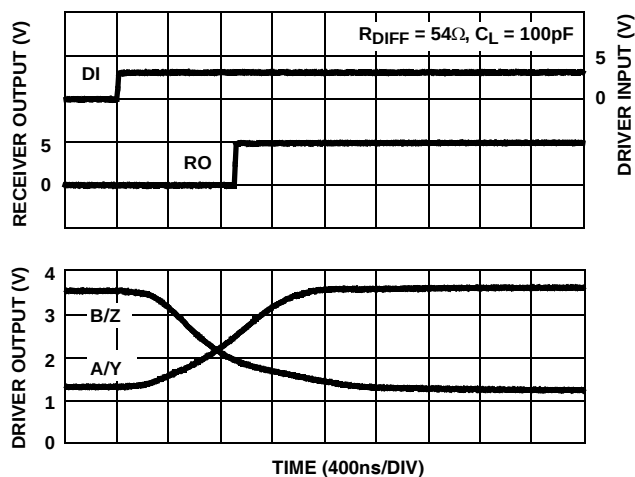


FIGURE 18. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL83080E, ISL83082E)

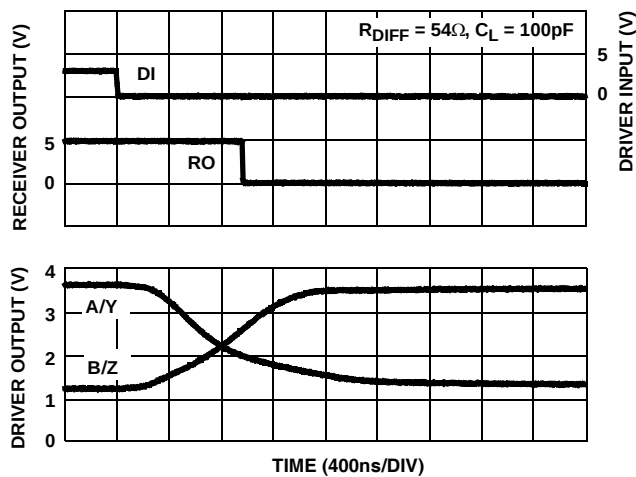


FIGURE 19. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL83080E, ISL83082E)

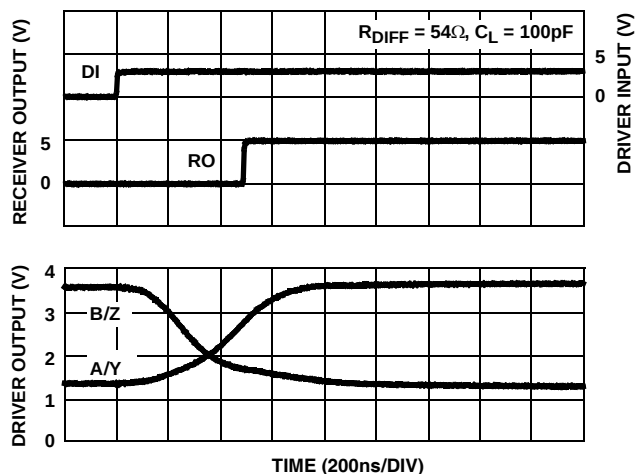


FIGURE 20. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL83083E, ISL83084E, ISL83085E)

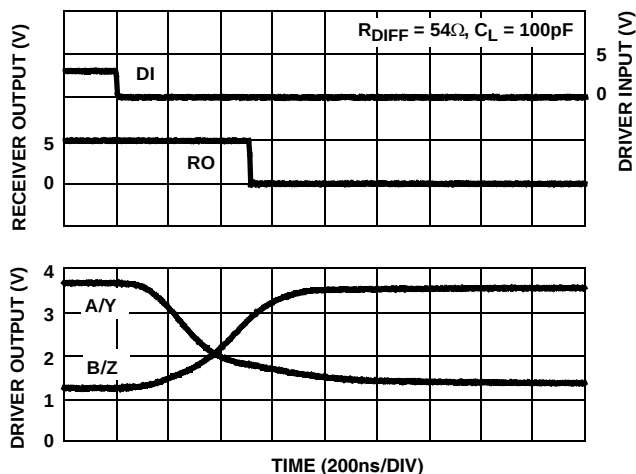


FIGURE 21. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL83083E, ISL83084E, ISL83085E)

**Typical Performance Curves**  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$ ; Unless Otherwise Specified (Continued)

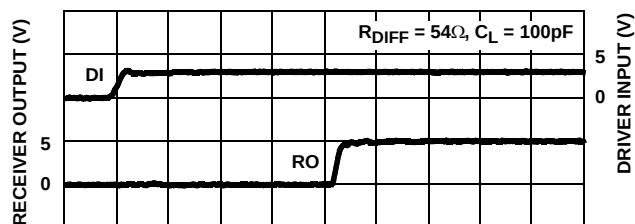


FIGURE 22. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL83086E, ISL83088E)

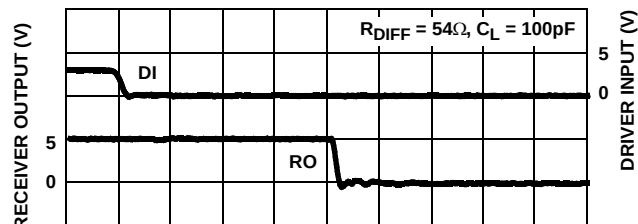


FIGURE 23. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL83086E, ISL83088E)

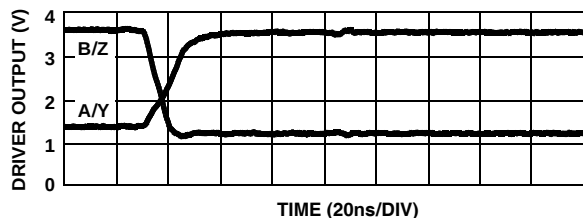


FIGURE 24. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

**Die Characteristics**

SUBSTRATE POTENTIAL (POWERED UP):

GND

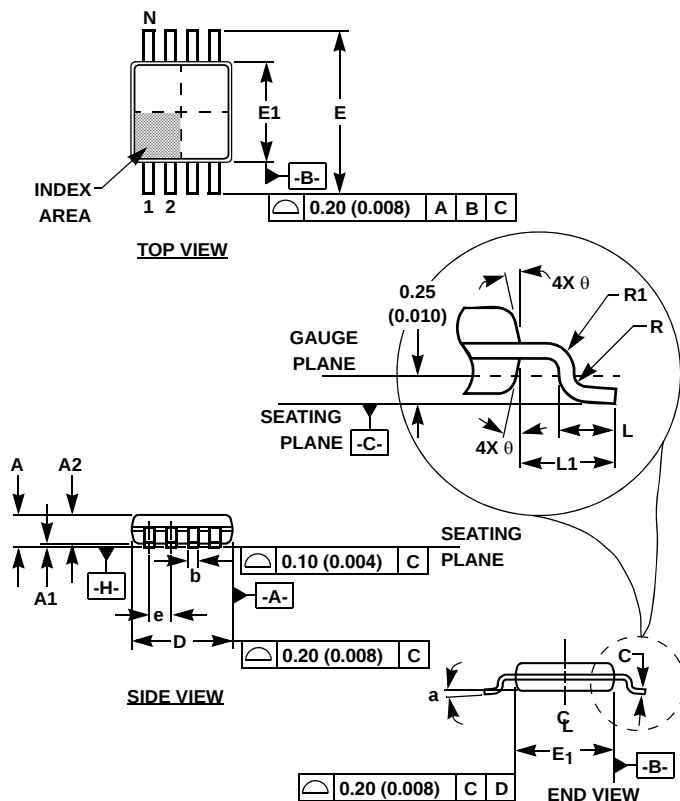
TRANSISTOR COUNT:

525

PROCESS:

Si Gate BiCMOS

# Mini Small Outline Plastic Packages (MSOP)



## M8.118 (JEDEC MO-187AA) 8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

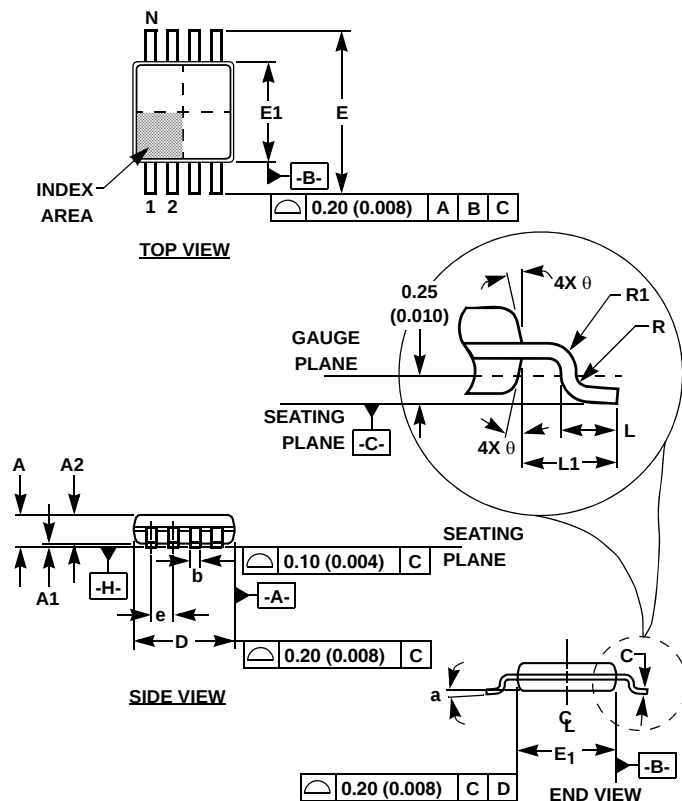
| SYMBOL | INCHES    |       | MILLIMETERS |      | NOTES |
|--------|-----------|-------|-------------|------|-------|
|        | MIN       | MAX   | MIN         | MAX  |       |
| A      | 0.037     | 0.043 | 0.94        | 1.10 | -     |
| A1     | 0.002     | 0.006 | 0.05        | 0.15 | -     |
| A2     | 0.030     | 0.037 | 0.75        | 0.95 | -     |
| b      | 0.010     | 0.014 | 0.25        | 0.36 | 9     |
| c      | 0.004     | 0.008 | 0.09        | 0.20 | -     |
| D      | 0.116     | 0.120 | 2.95        | 3.05 | 3     |
| E1     | 0.116     | 0.120 | 2.95        | 3.05 | 4     |
| e      | 0.026 BSC |       | 0.65 BSC    |      | -     |
| E      | 0.187     | 0.199 | 4.75        | 5.05 | -     |
| L      | 0.016     | 0.028 | 0.40        | 0.70 | 6     |
| L1     | 0.037 REF |       | 0.95 REF    |      | -     |
| N      | 8         |       | 8           |      | 7     |
| R      | 0.003     | -     | 0.07        | -    | -     |
| R1     | 0.003     | -     | 0.07        | -    | -     |
| 0      | 5°        | 15°   | 5°          | 15°  | -     |
| α      | 0°        | 6°    | 0°          | 6°   | -     |

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### NOTES:

- These package dimensions are within allowable dimensions of JEDEC MO-187BA.
- Dimensioning and tolerancing per ANSI Y14.5M-1994.
- Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane. [-H-] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
- Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
- "L" is the length of terminal for soldering to a substrate.
- "N" is the number of terminal positions.
- Terminal numbers are shown for reference only.
- Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
- Datums [-A-] and [-B-] to be determined at Datum plane [-H-].
- Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

## Mini Small Outline Plastic Packages (MSOP)



### M10.118 (JEDEC MO-187BA)

#### 10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

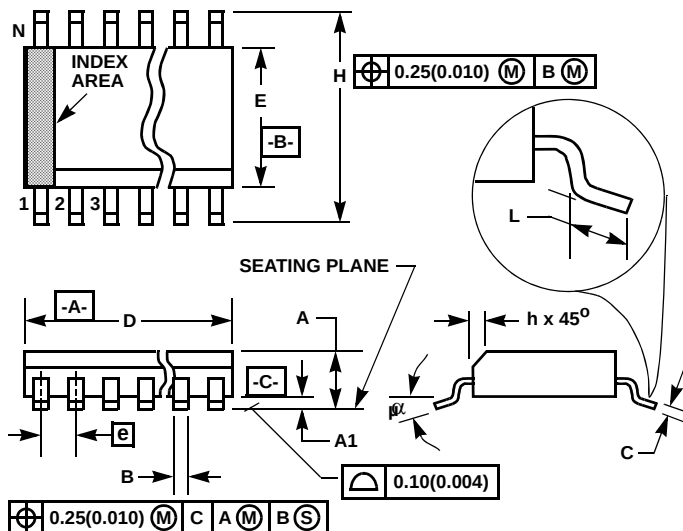
| SYMBOL | INCHES    |       | MILLIMETERS |      | NOTES |
|--------|-----------|-------|-------------|------|-------|
|        | MIN       | MAX   | MIN         | MAX  |       |
| A      | 0.037     | 0.043 | 0.94        | 1.10 | -     |
| A1     | 0.002     | 0.006 | 0.05        | 0.15 | -     |
| A2     | 0.030     | 0.037 | 0.75        | 0.95 | -     |
| b      | 0.007     | 0.011 | 0.18        | 0.27 | 9     |
| c      | 0.004     | 0.008 | 0.09        | 0.20 | -     |
| D      | 0.116     | 0.120 | 2.95        | 3.05 | 3     |
| E1     | 0.116     | 0.120 | 2.95        | 3.05 | 4     |
| e      | 0.020 BSC |       | 0.50 BSC    |      | -     |
| E      | 0.187     | 0.199 | 4.75        | 5.05 | -     |
| L      | 0.016     | 0.028 | 0.40        | 0.70 | 6     |
| L1     | 0.037 REF |       | 0.95 REF    |      | -     |
| N      | 10        |       | 10          |      | 7     |
| R      | 0.003     | -     | 0.07        | -    | -     |
| R1     | 0.003     | -     | 0.07        | -    | -     |
| θ      | 5°        | 15°   | 5°          | 15°  | -     |
| α      | 0°        | 6°    | 0°          | 6°   | -     |

Rev. 0 12/02

#### NOTES:

- These package dimensions are within allowable dimensions of JEDEC MO-187BA.
- Dimensioning and tolerancing per ANSI Y14.5M-1994.
- Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane. **-H-** Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
- Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
- "L" is the length of terminal for soldering to a substrate.
- "N" is the number of terminal positions.
- Terminal numbers are shown for reference only.
- Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
- Datums **-A-** and **-B-** to be determined at Datum plane **-H-**.
- Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

## Small Outline Plastic Packages (SOIC)



### NOTES:

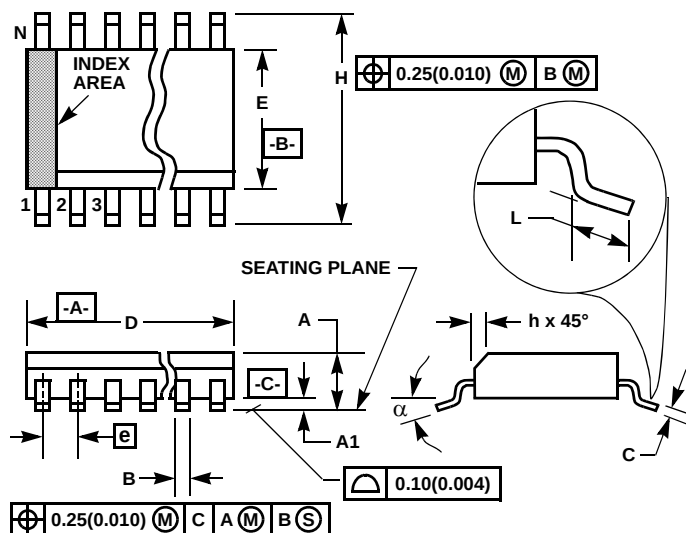
1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

### M14.15 (JEDEC MS-012-AB ISSUE C) 14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES    |        | MILLIMETERS |      | NOTES |
|--------|-----------|--------|-------------|------|-------|
|        | MIN       | MAX    | MIN         | MAX  |       |
| A      | 0.0532    | 0.0688 | 1.35        | 1.75 | -     |
| A1     | 0.0040    | 0.0098 | 0.10        | 0.25 | -     |
| B      | 0.013     | 0.020  | 0.33        | 0.51 | 9     |
| C      | 0.0075    | 0.0098 | 0.19        | 0.25 | -     |
| D      | 0.3367    | 0.3444 | 8.55        | 8.75 | 3     |
| E      | 0.1497    | 0.1574 | 3.80        | 4.00 | 4     |
| e      | 0.050 BSC |        | 1.27 BSC    |      | -     |
| H      | 0.2284    | 0.2440 | 5.80        | 6.20 | -     |
| h      | 0.0099    | 0.0196 | 0.25        | 0.50 | 5     |
| L      | 0.016     | 0.050  | 0.40        | 1.27 | 6     |
| N      | 14        |        | 14          |      | 7     |
| α      | 0°        | 8°     | 0°          | 8°   | -     |

Rev. 0 12/93

## Small Outline Plastic Packages (SOIC)



### NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

### M8.15 (JEDEC MS-012-AA ISSUE C)

#### 8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES    |        | MILLIMETERS |      | NOTES |
|--------|-----------|--------|-------------|------|-------|
|        | MIN       | MAX    | MIN         | MAX  |       |
| A      | 0.0532    | 0.0688 | 1.35        | 1.75 | -     |
| A1     | 0.0040    | 0.0098 | 0.10        | 0.25 | -     |
| B      | 0.013     | 0.020  | 0.33        | 0.51 | 9     |
| C      | 0.0075    | 0.0098 | 0.19        | 0.25 | -     |
| D      | 0.1890    | 0.1968 | 4.80        | 5.00 | 3     |
| E      | 0.1497    | 0.1574 | 3.80        | 4.00 | 4     |
| e      | 0.050 BSC |        | 1.27 BSC    |      | -     |
| H      | 0.2284    | 0.2440 | 5.80        | 6.20 | -     |
| h      | 0.0099    | 0.0196 | 0.25        | 0.50 | 5     |
| L      | 0.016     | 0.050  | 0.40        | 1.27 | 6     |
| N      | 8         |        | 8           |      | 7     |
| α      | 0°        | 8°     | 0°          | 8°   | -     |

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